An Infineon Technologies Company

IRHYS9A7234CM, IRHYB9A7234CM

PD-97886B

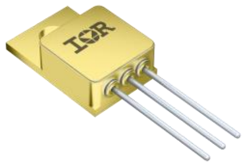
Radiation Hardened Power MOSFET
250V, 17A, N-channel, R9 Superjunction Technology

Features

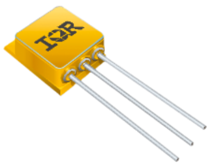
- Low $R_{DS(on)}$
- Fast switching
- Single event effect (SEE) hardened
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Electrically isolated case
- Ceramic eyelets (Low-Ohmic TO-257AA)
- ESD rating: class 2 per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}:** 250V
- **I_D :** 17A
- **$R_{DS(on), max}$:** 110mΩ
- **$Q_{G, max}$:** 34nC
- **REF:** MIL-PRF-19500/775



Low – Ohmic TO-257AA



Tabless TO-257AA

Applications

- DC-DC converter
- Motor drives
- Electric propulsion

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 88.6 MeV·cm^2/mg. Their combination of low $R_{DS(on)}$ and faster switching times reduces the power losses and increases power density in today's high speed switching applications such as DC-DC converters and motor controllers. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHYS9A7234CM	Low-Ohmic TO-257AA	COTS	100 krad(Si)
JANSR2N7649T3	Low-Ohmic TO-257AA	JANS	100 krad(Si)
IRHYS9A3234CM	Low-Ohmic TO-257AA	COTS	300 krad(Si)
JANSF2N7649T3	Low-Ohmic TO-257AA	JANS	300 krad(Si)
IRHYB9A7234CM	Tabless TO-257AA	COTS	100 krad(Si)
JANSR2N7649D5	Tabless TO-257AA	JANS	100 krad(Si)
IRHYB9A3234CM	Tabless TO-257AA	COTS	300 krad(Si)
JANSF2N7649D5	Tabless TO-257AA	JANS	300 krad(Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	17	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	10.5	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	68	A
P_D @ T_C = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	331	mJ
I_{AR}	Avalanche Current [1]	17	A
E_{AR}	Repetitive Avalanche Energy [1]	17	mJ
dv/dt	Peak Diode Reverse Recovery [3]	13	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063in./1.6mm from case for 10s)	
	Weight	4.3 (Typical)	g

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[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = 150V, starting T_J = 25°C, L = 6.0mH, Peak I_L = 10.5A, V_{GS} = 20V

[3] $I_{SD} \leq 17A$, di/dt ≤ 1100A/µs, $V_{DD} \leq 250V$, $T_J \leq 150°C$

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_j = 25°C$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	$V_{GS} = 0V$, $I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/°C	Reference to 25°C, $I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	110	mΩ	$V_{GS} = 12V$, $I_{D2} = 10.5A$ [1]
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} \geq V_{GS}$, $I_D = 1mA$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-9.5	—	mV/°C	
Gfs	Forward Transconductance	10	—	—	S	$V_{DS} = 15V$, $I_{D2} = 10.5A$ [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	µA	$V_{DS} = 200V$, $V_{GS} = 0V$
		—	—	10		$V_{DS} = 200V$, $V_{GS} = 0V$, $T_J = 125°C$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_G	Total Gate Charge	—	—	34	nC	$I_{D1} = 17A$ $V_{DS} = 125V$ $V_{GS} = 12V$
Q_{GS}	Gate-to-Source Charge	—	—	13		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	13		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	$I_{D1} = 17A$ ** $V_{DD} = 125V$ $R_G = 7.5\Omega$ $V_{GS} = 12V$
t_r	Rise Time	—	—	25		
$t_{d(off)}$	Turn-Off Delay Time	—	—	50		
t_f	Fall Time	—	—	25		
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C_{iss}	Input Capacitance	—	1510	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	240	—		
C_{rss}	Reverse Transfer Capacitance	—	1.0	—		
R_G	Gate Resistance	—	1.0	—	Ω	$f = 1.0MHz$, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

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[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	68	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25°C, I_S = 17A, V_{GS} = 0V$ [2]
t_{rr}	Reverse Recovery Time	—	—	335	ns	$T_J = 25°C, I_F = 17A, V_{DD} \le 50V$ di/dt = 100A/µs [2]
Q_{rr}	Reverse Recovery Charge	—	—	3.6	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	80	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics - Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_j = 25°C$, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300krads (Si) [5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	V	$V_{GS} = 0V, I_D = 1mA$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	$V_{DS} \ge V_{GS}, I_D = 1mA$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	µA	$V_{DS} = 200V, V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [2]	—	110	mΩ	$V_{GS} = 12V, I_{D2} = 10.5A$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (Low-Ohmic TO-257AA) [2]	—	110	mΩ	$V_{GS} = 12V, I_{D2} = 10.5A$
V_{SD}	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0V, I_F = 17A$

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[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] Total Dose Irradiation with V_{GS} Bias. V_{GS}=12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = 200V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[5] Part numbers IRHYS9A7234CM (JANSR2N7649T3), IRHYS9A3234CM (JANSF2N7649T3), IRHYB9A7234CM (JANSR2N7649D5), and IRHYB9A3234CM (JANSF2N7649D5)

2.4.2 Single Event Effects – Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)			
			V_{GS} = 0V	V_{GS} = -1V	V_{GS} =- 5V	V_{GS} = -10V
35.7 ± 5%	486 ± 5%	59 ± 10%	250	250	250	250
58.5 ± 5%	865 ± 5%	69 ± 7.5%	250	250	250	250
88.6 ± 5%	1685 ± 5%	90 ± 5%	250	250	—	—

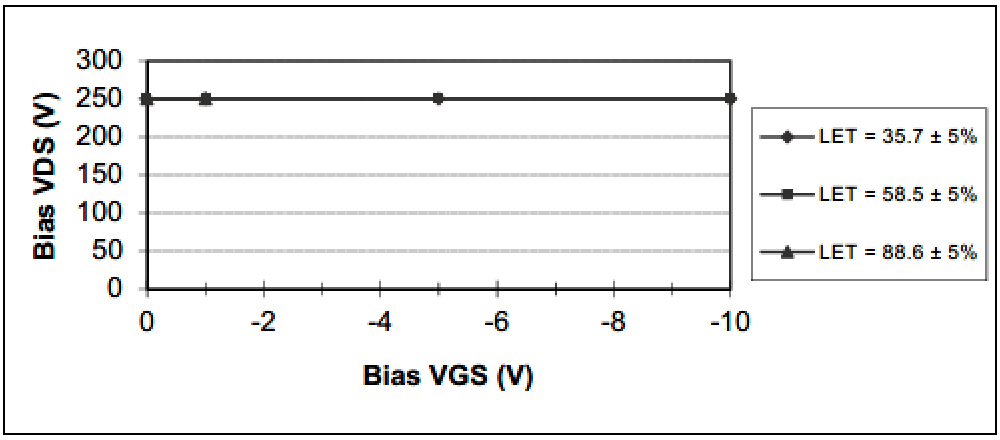


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

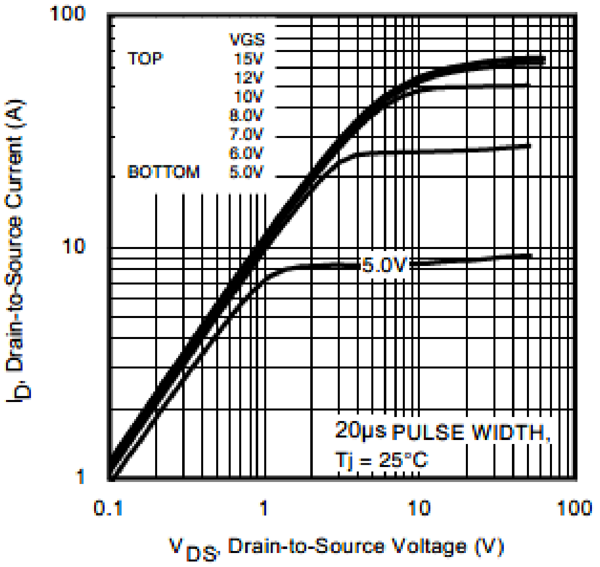


Figure 2 Typical Output Characteristics

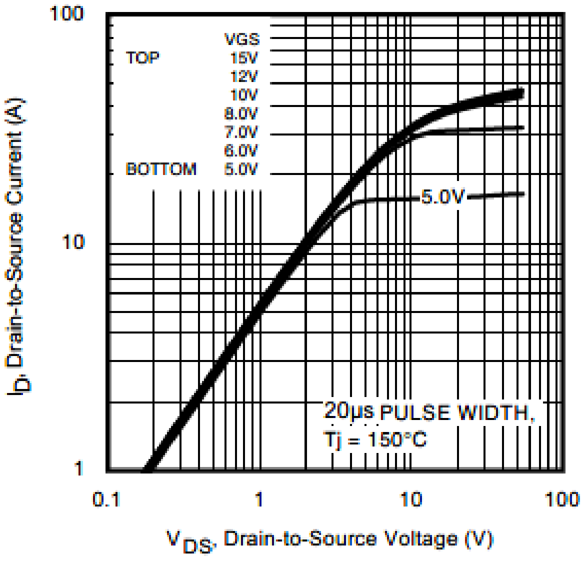


Figure 3 Typical Output Characteristics

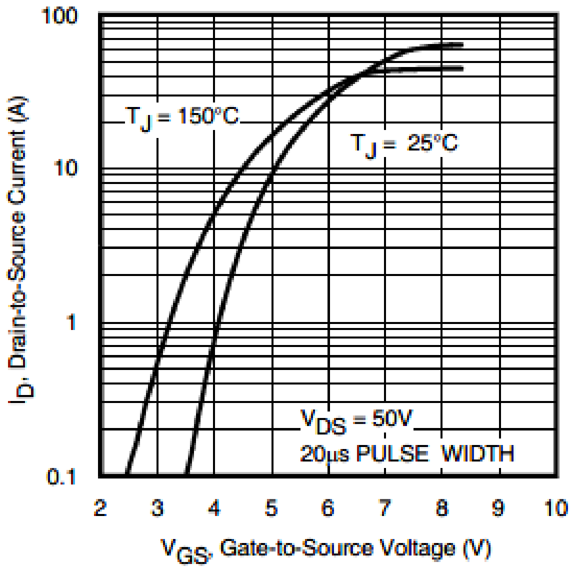


Figure 4 Typical Transfer Characteristics

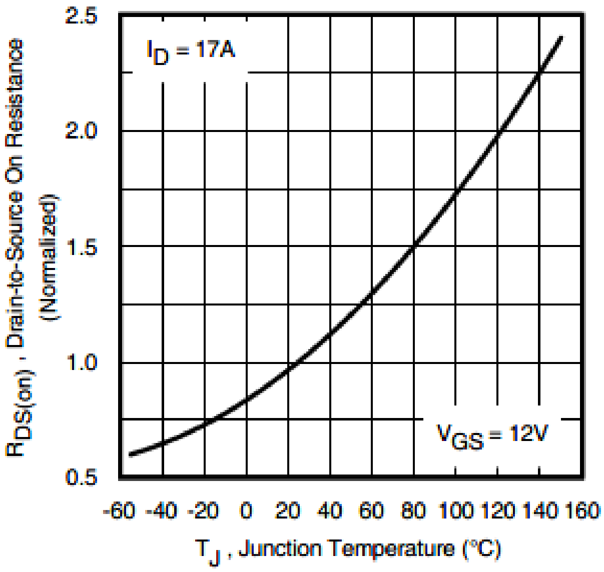


Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

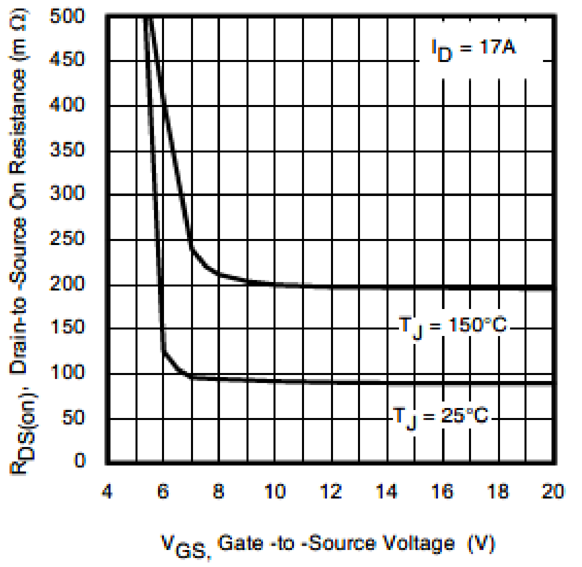


Figure 6 Typical On-Resistance Vs. Gate Voltage

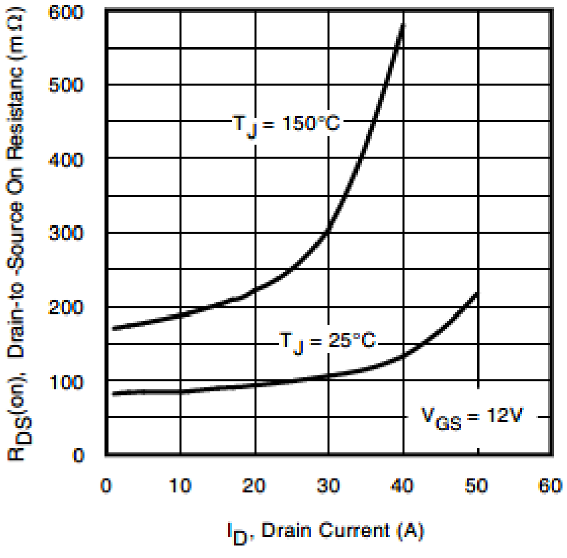


Figure 7 Typical On-Resistance Vs. Drain Current

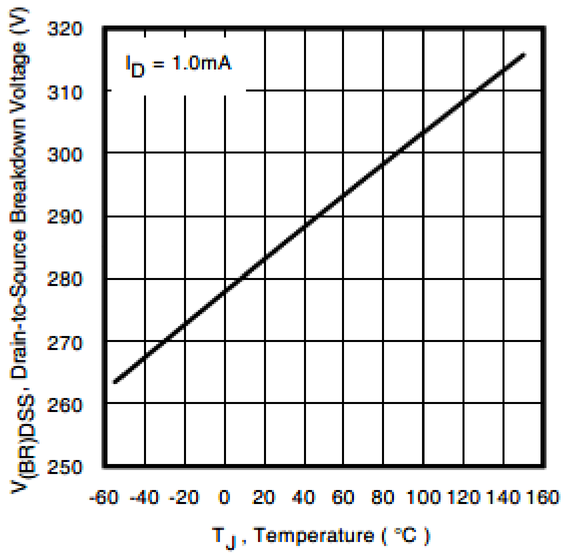


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

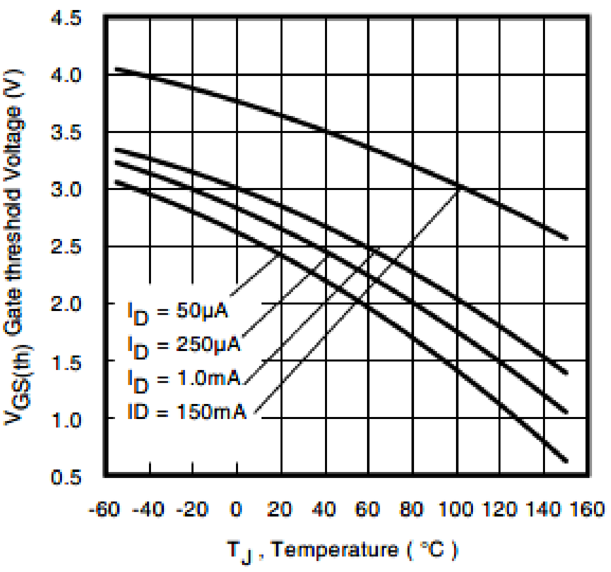


Figure 9 Typical Threshold Voltage Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

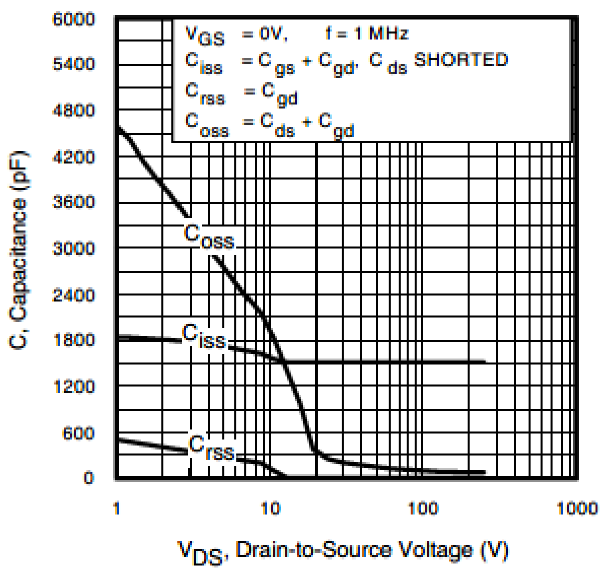


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

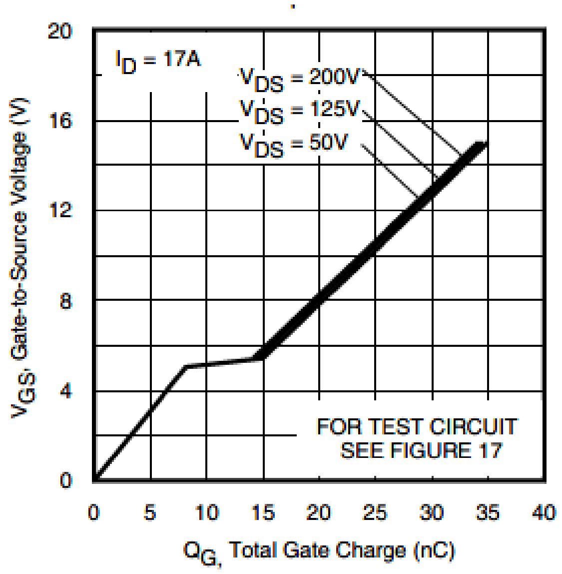


Figure 11 Typical Gate Charge Vs. Gate-to-Source Voltage

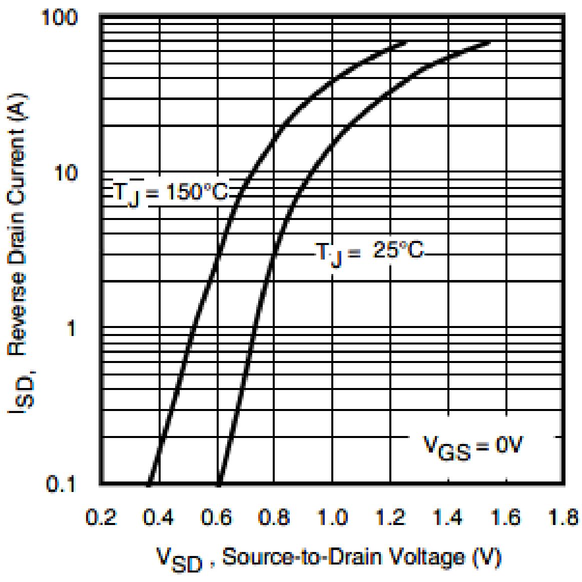


Figure 12 Typical Source-Drain Vs. Diode Forward Voltage

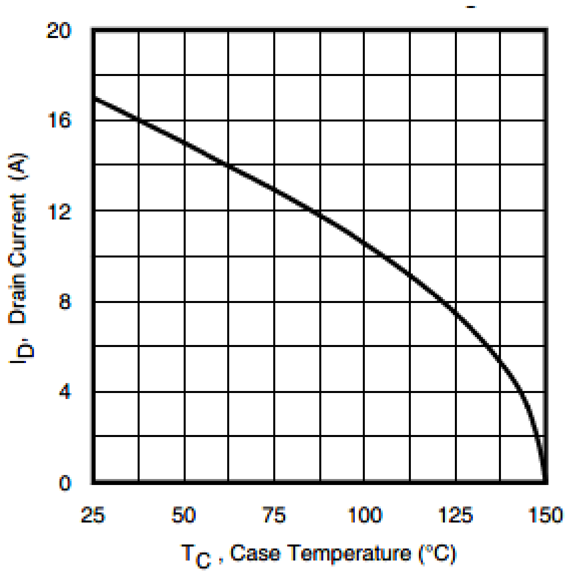


Figure 13 Maximum Drain Current Vs. Case Temperature

Electrical Characteristics Curves (Pre-irradiation)

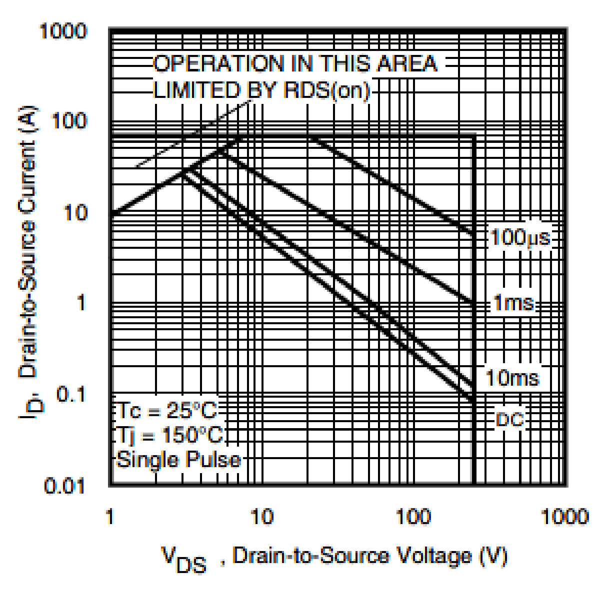


Figure 14 Maximum Safe Operating Area

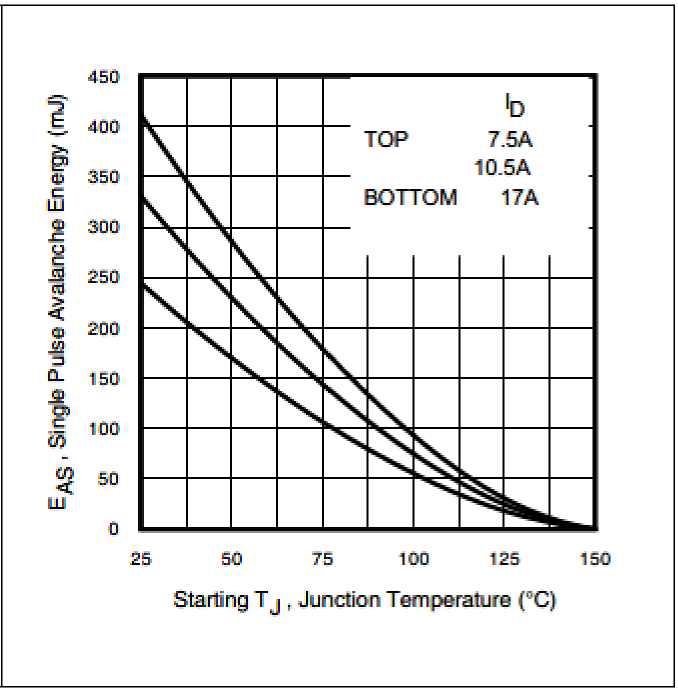


Figure 15 Maximum Effective Transient Thermal Impedance, Junction-to-Case

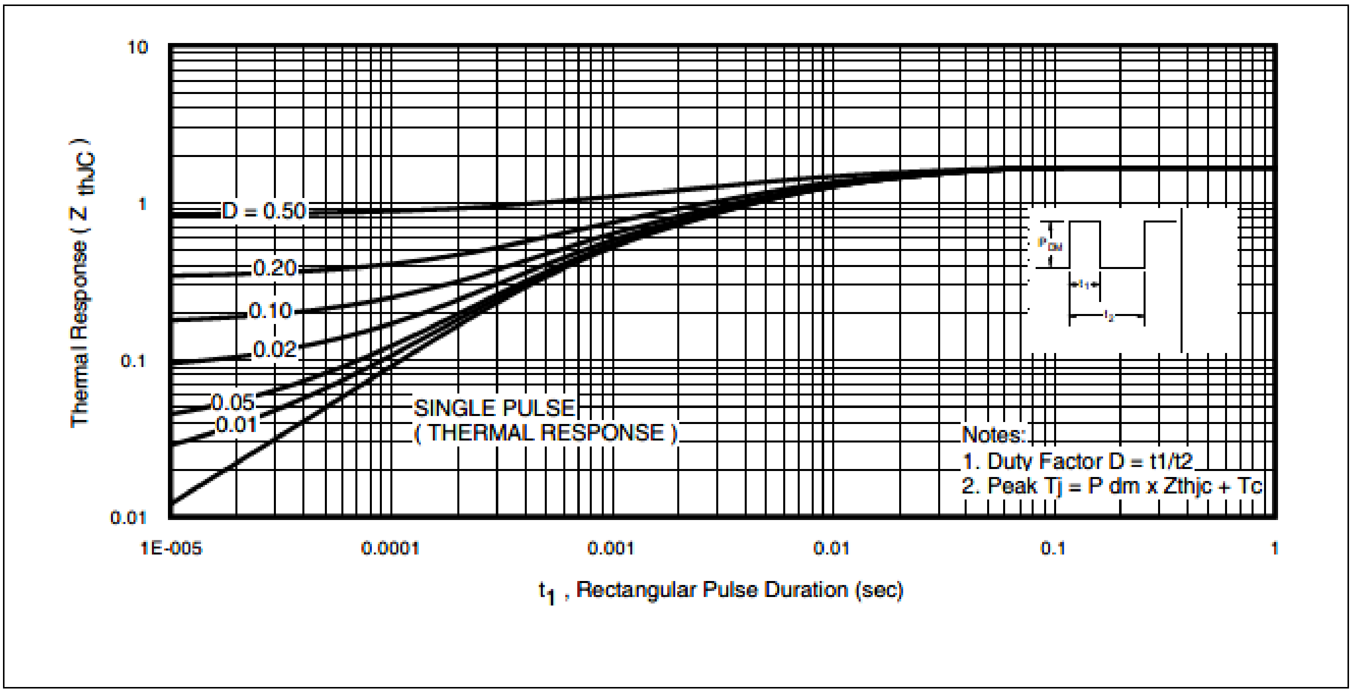


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

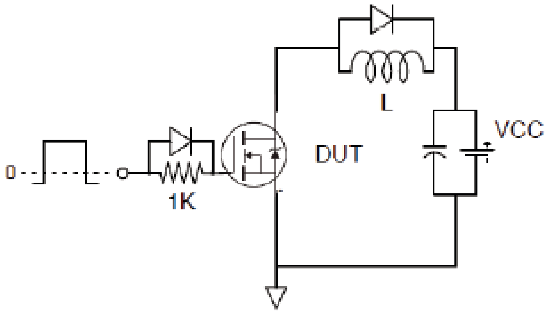


Figure 17 Gate Charge Test Circuit

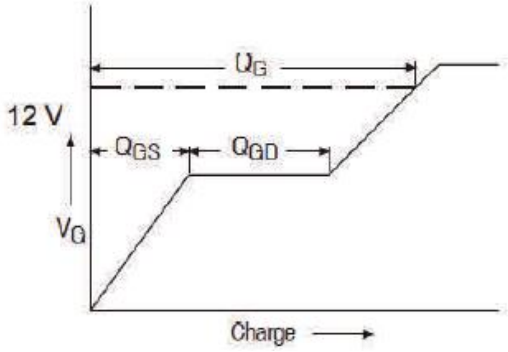


Figure 18 Gate Charge Waveform

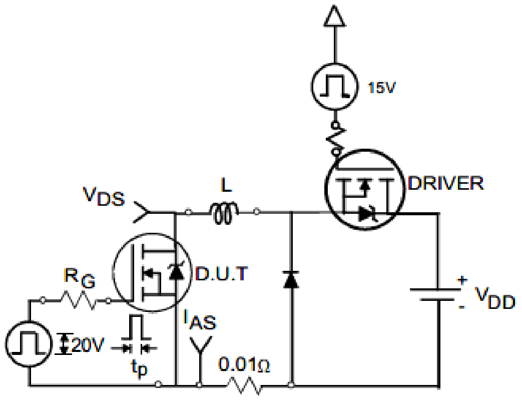


Figure 19 Unclamped Inductive Test Circuit

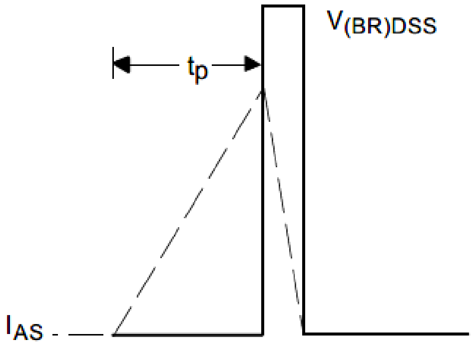


Figure 20 Unclamped Inductive Waveform

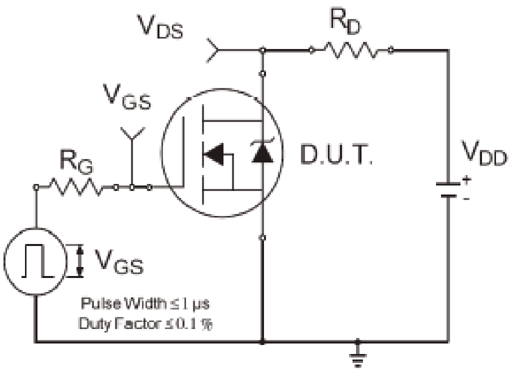


Figure 21 Switching Time Test Circuit

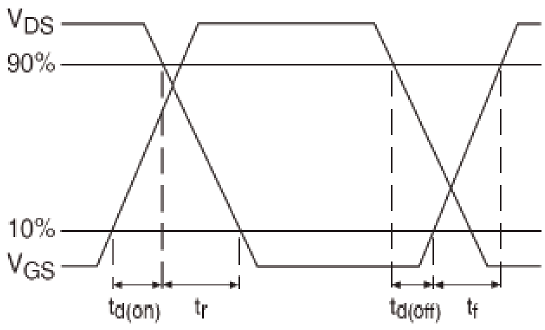
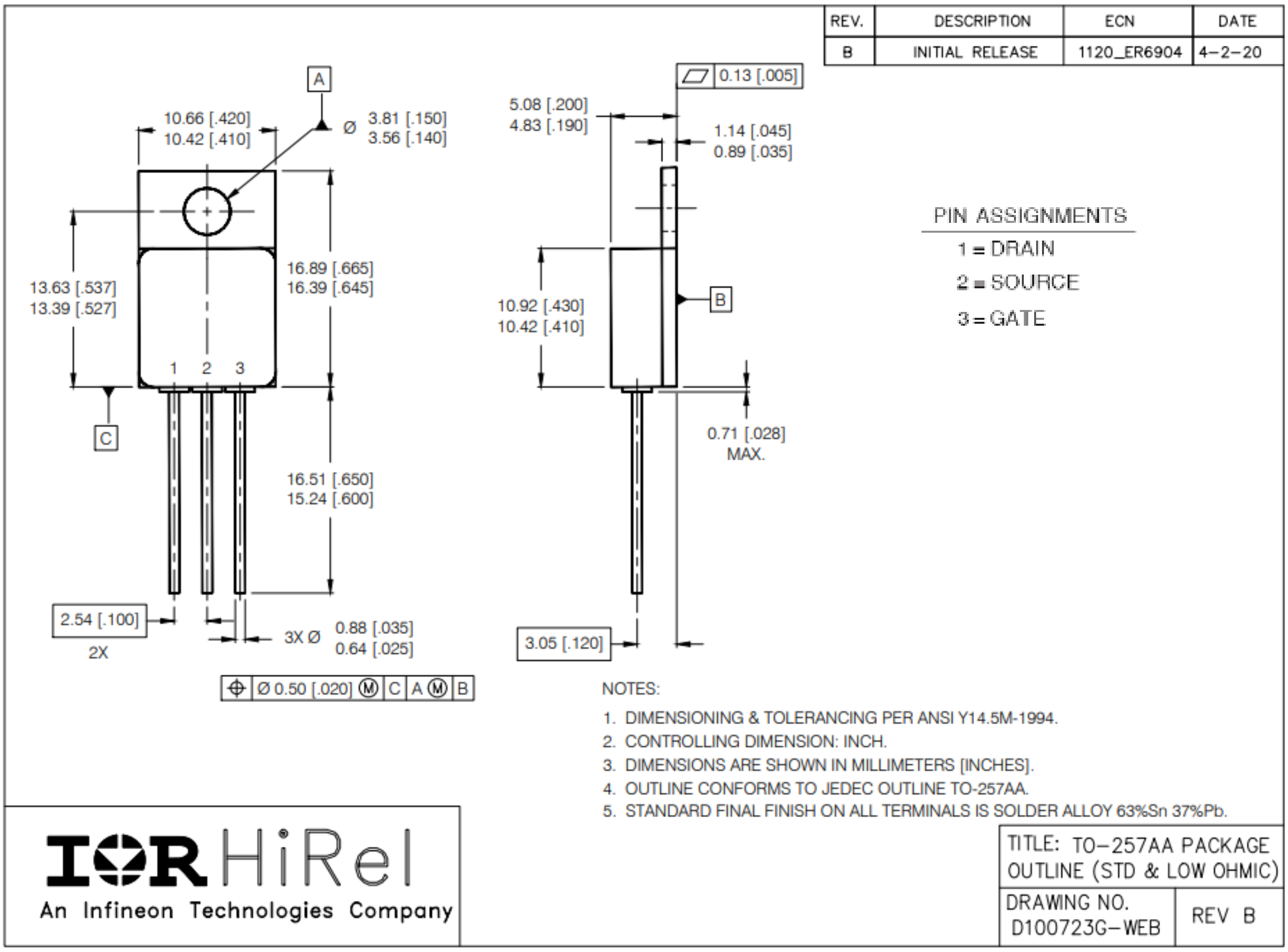


Figure 22 Switching Time Waveforms

5 Package Outline (Low-Ohmic TO-257AA)

Note: For the most updated package outline, please see the website: [TO-257AA]



REV.	DESCRIPTION	ECN	DATE
B	INITIAL RELEASE	1120_ER6904	4–2–20

PIN ASSIGNMENTS
1 = DRAIN
2 = SOURCE
3 = GATE

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.
5. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

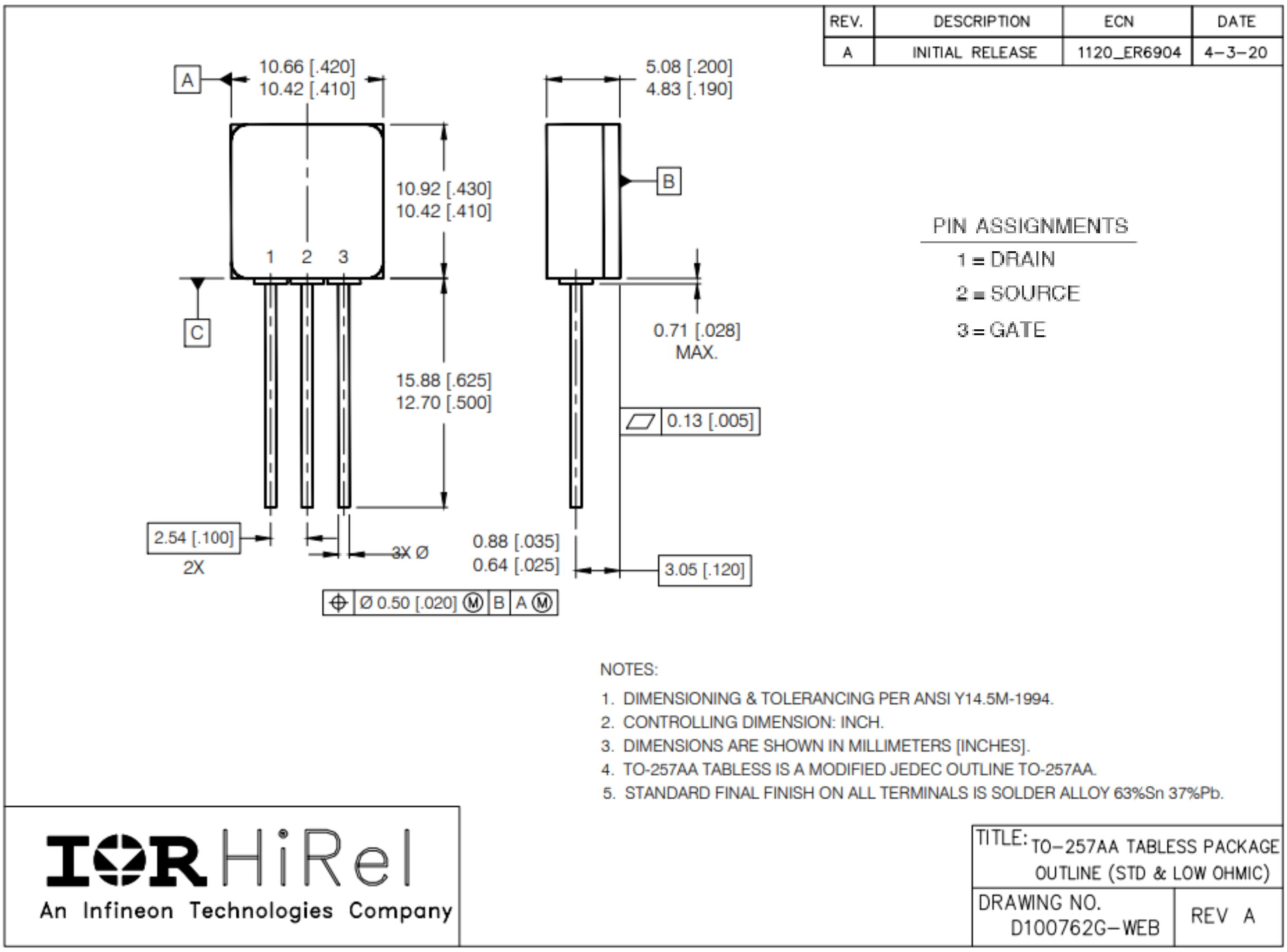
TITLE: TO–257AA PACKAGE OUTLINE (STD & LOW OHMIC)
DRAWING NO. D100723G–WEB
REV B

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

6 Package Outline (Tabless TO-257AA)

Note: For the most updated package outline, please see the website: [Tabless TO-257AA]



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Revision history

Document version	Date of release	Description of changes
	10/28/2019	Datasheet (PD-97886A)
Rev B	05/09/2022	Updated based on ECN-1120_09100

Edition 2022-05-09

Published by

International Rectifier HiRel Products, Inc.

An Infineon Technologies company

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Document reference

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