IRHNS9A97160 (JANSR2N7665U2A)

PD-97984A

Radiation Hardened Power MOSFET
Surface-Mount (SupIR-SMD™)
-100V, -91A, P-channel, R9 Superjunction Technology

Features

- Single event effect (SEE) hardened (up to LET of 91 MeV·cm²/mg)
- Low $R_{DS\,(on)}$
- Improved SOA for linear mode operation
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- Ceramic eyelets
- Light weight
- ESD rating: Class 3B per MIL-STD-750, Method 1020

Product Summary

- **B_{VDSS}:** -100V
- **I_D:** -91A
- **$R_{DS\,(on)\,max}$:** 17mΩ
- **$Q_{G\,max}$:** 230Nc
- **REF:** MIL-PRF-19500/791

SupIR-SMD™

Potential Applications

- DC-DC converter
- Motor drives
- Inrush current protection
- Power distribution

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. This family of p-channel MOSFETs are the first radiation hardened devices that are based on a superjunction technology. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 91 MeV·cm²/mg. Their combination of low $R_{DS\,(on)}$ and improved SOA allows for better performance in applications such as Solid-State Power Controllers (SSPC), DC-DC converters and motor drives. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNS9A97160	SupIR-SMD™	COTS	100 krad (Si)
JANSR2N7665U2A	SupIR-SMD™	JANS	100 krad (Si)
IRHNS9A93160	SupIR-SMD™	COTS	300 krad (Si)
JANSF2N7665U2A	SupIR-SMD™	JANS	300 krad (Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = -12V, T_C = 25°C	Continuous Drain Current	-91	A
I_{D2} @ V_{GS} = -12V, T_C = 100°C	Continuous Drain Current	-57	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	-364	A
P_D @ T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	4224	mJ
I_{AR}	Avalanche Current [1]	-57	A
E_{AR}	Repetitive Avalanche Energy [1]	25	mJ
dv/dt	Peak Diode Reverse Recovery [3]	10	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = -100V, starting T_J = 25°C, L = 2.6mH, Peak I_L = -57A, V_{GS} = -20V

[3] $I_{SD} \leq$ -91A, di/dt $\leq$ -400A/µs, $V_{DD} \leq$ -100V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS\ (on)}$	Static Drain-to-Source On-State Resistance	—	—	17	mΩ	V_{GS} = -12V, I_{D2} =- 57A [1]
$V_{GS\ (th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} \geq V_{GS}$, I_D = -5mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	5.7	—	mV/°C	
Gfs	Forward Transconductance	50	—	—	S	V_{DS} = -15V, I_{D2} = -57A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-10	µA	V_{DS} = -80V, V_{GS} = 0V
		—	—	-25		V_{DS} = -80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	230	nC	I_{D1} = -91A V_{DS} = -50V V_{GS} = -12V
Q_{GS}	Gate-to-Source Charge	—	—	65		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	47		
$t_{d(on)}$	Turn-On Delay Time	—	—	36	ns	I_{D1} = -91A ** V_{DD} = -50V R_G = 2.4Ω V_{GS} = -12V
t_r	Rise Time	—	—	100		
$t_{d(off)}$	Turn-Off Delay Time	—	—	176		
t_f	Fall Time	—	—	155		
$L_s + L_D$	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	12060	—	pF	V_{GS} = 0V V_{DS} = -25V ƒ = 100KHz
C_{oss}	Output Capacitance	—	2210	—		
C_{rss}	Reverse Transfer Capacitance	—	55	—		
R_G	Gate Resistance	—	3.1	—	Ω	ƒ = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-91	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	-364	A	
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	T_J = 25°C, I_S =- 91A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	134	201	ns	T_J = 25°C, I_F = -91A, V_{DD} ≤ -25V di/dt = -100A/µs
Q_{rr}	Reverse Recovery Charge	—	745	—	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.5	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PC Board (Soldered to 2" sq. inch copper clad board)	—	1.6	—	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300 krad (Si) [5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	V	$V_{DS} \geq V_{GS}$, I_D = -5.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	100		V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	µA	V_{DS} = -80V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [2]	—	18	mΩ	V_{GS} = -12V, I_{D2} = -57A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SupIR-SMD) [2]	—	17	mΩ	V_{GS} = -12V, I_{D2} =- 57A
V_{SD}	Diode Forward Voltage	—	-1.3	V	V_{GS} = 0V, I_F = -75A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = -12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = -80V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[5] Part numbers IRHNS9A97160 (JANSR2N7665U2A) and IRHNS9A93160 (JANSF2N7665U2A)

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 **Typical Single Event Effects Safe Operating Area**

LET ($MeV \cdot cm^2/mg$)	Energy (MeV)	Range (µm)	V_{DS} (V)			
			V_{GS} = 0V	V_{GS} = 3V	V_{GS} = 5V	V_{GS} = 10V
38.3 ± 5%	348 ± 5%	42.7 ± 7.5%	-100	-100	-100	-100
62.0 ± 10%	642 ± 10%	52.8 ± 5%	-100	-100	-100	—
91.0 ± 5%	1350 ± 7.5%	74.2 ± 5%	-100	-100	—	—

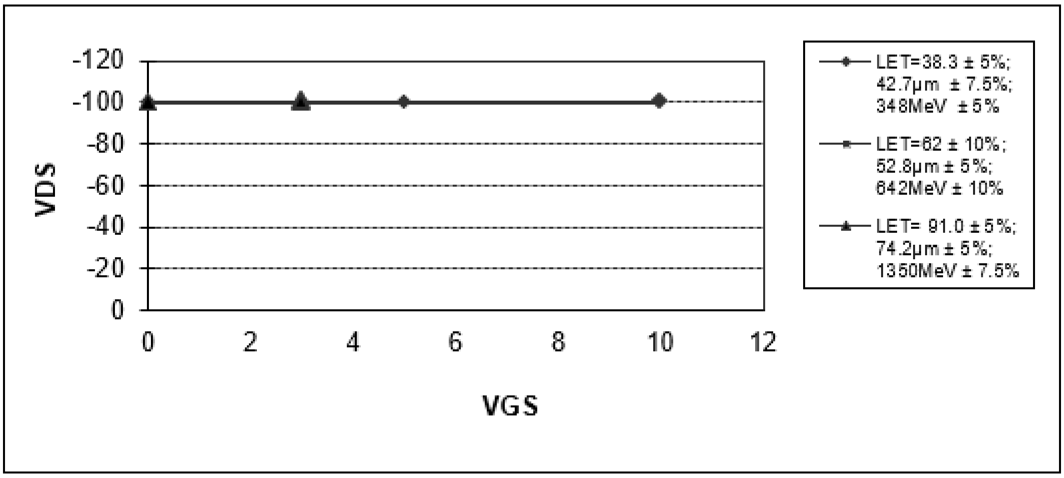


Figure 1 **Typical Single Event Effect, Safe Operating Area**

3 Electrical Characteristics Curves (Pre-irradiation)

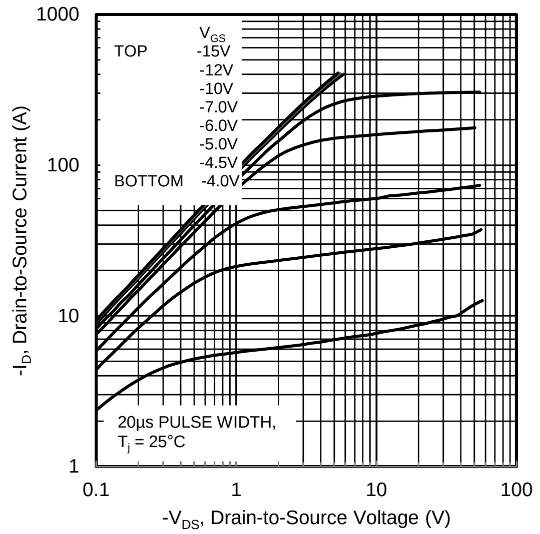


Figure 2 **Typical Output Characteristics**

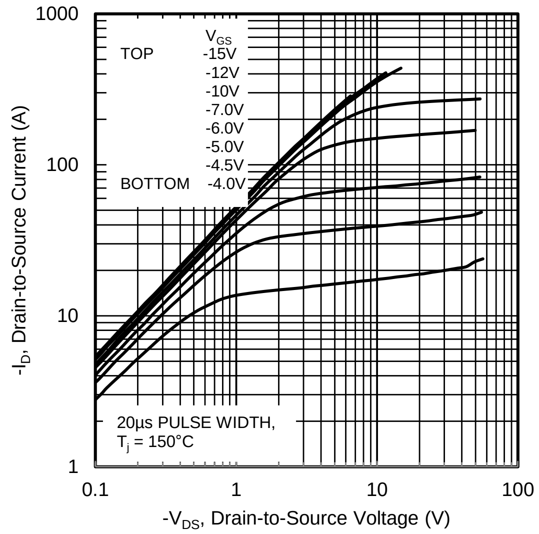


Figure 3 **Typical Output Characteristics**

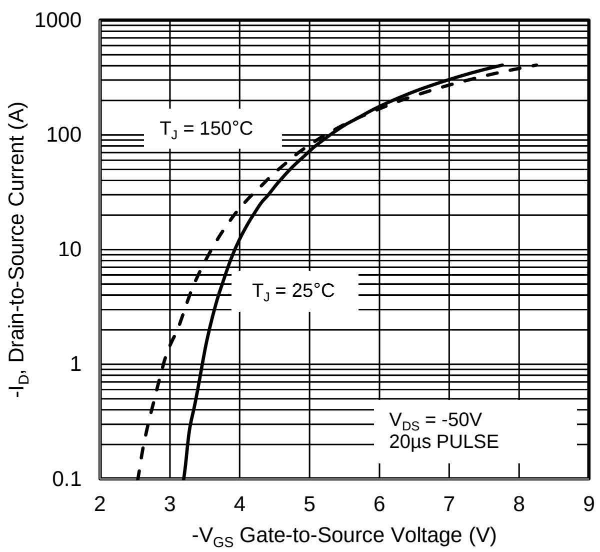


Figure 4 **Typical Transfer Characteristics**

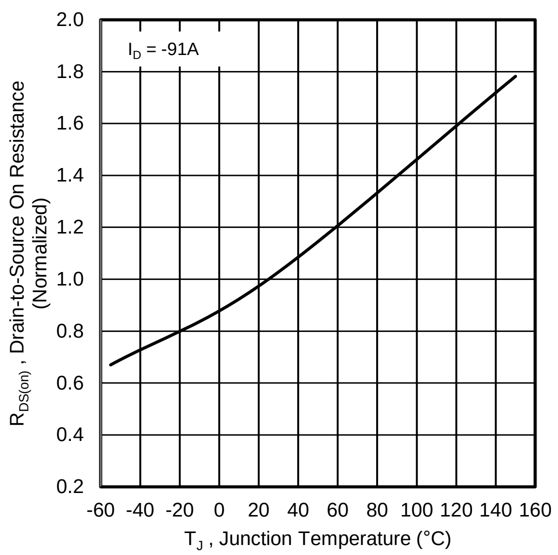


Figure 5 **Normalized On-Resistance Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

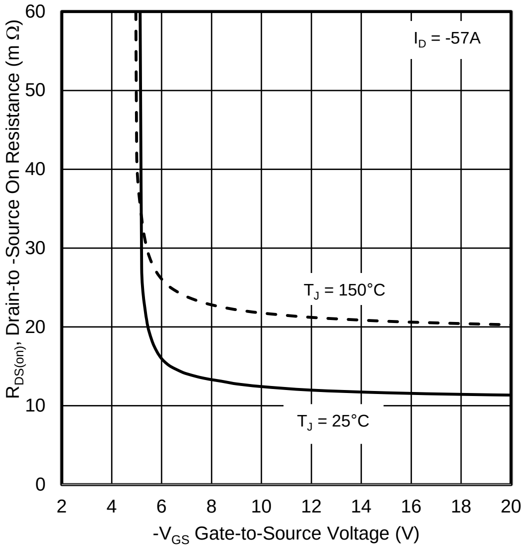


Figure 6 Typical On-Resistance Vs Gate Voltage

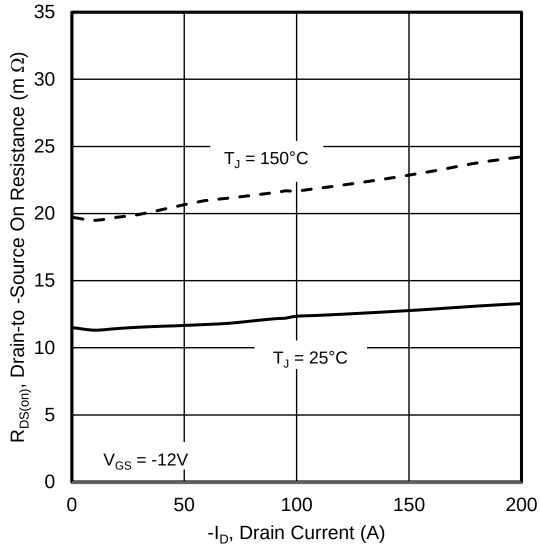


Figure 7 Typical On-Resistance Vs Drain Current

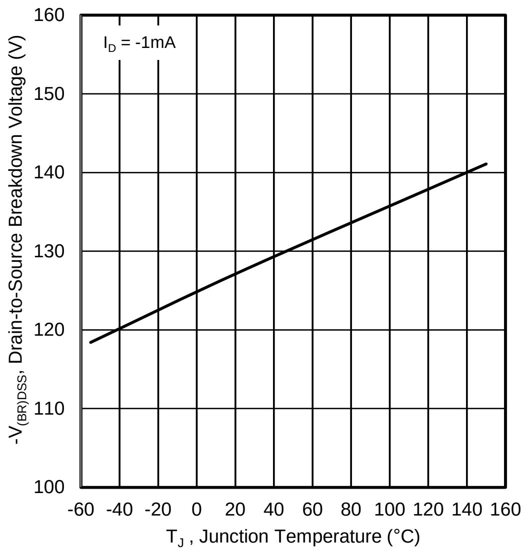


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

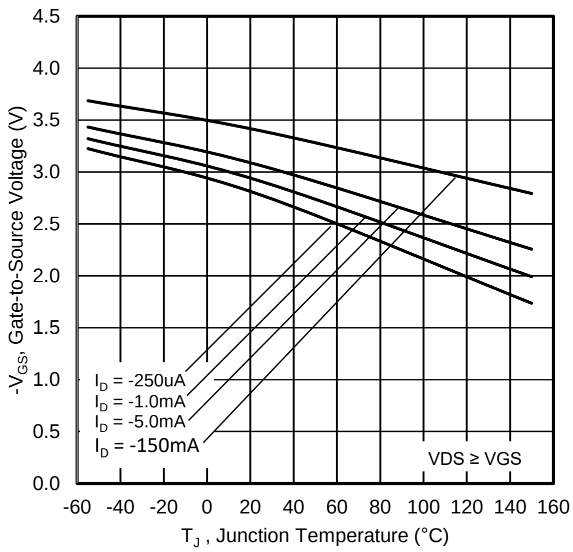


Figure 9 Typical Gate-to-Source Voltage Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

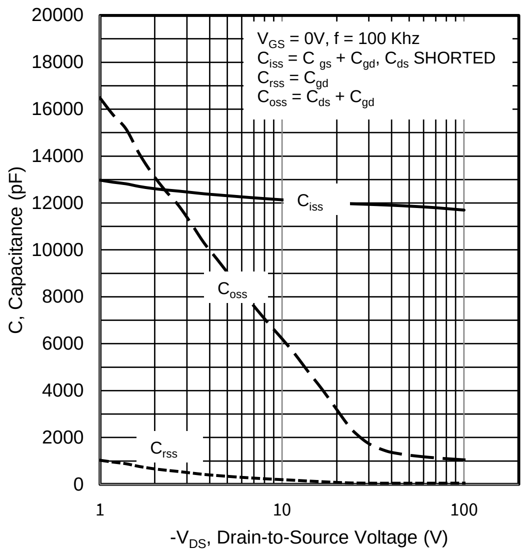


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

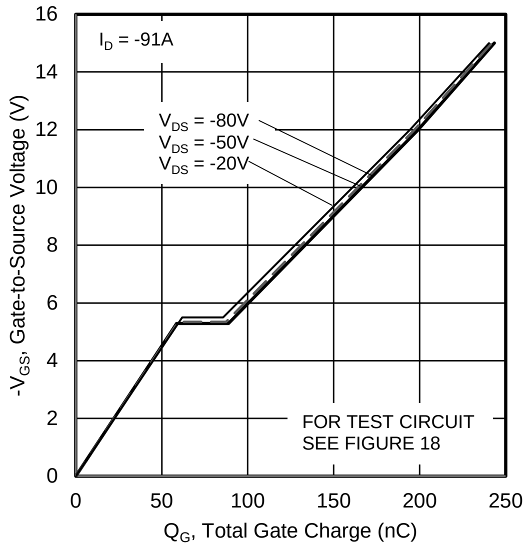


Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge

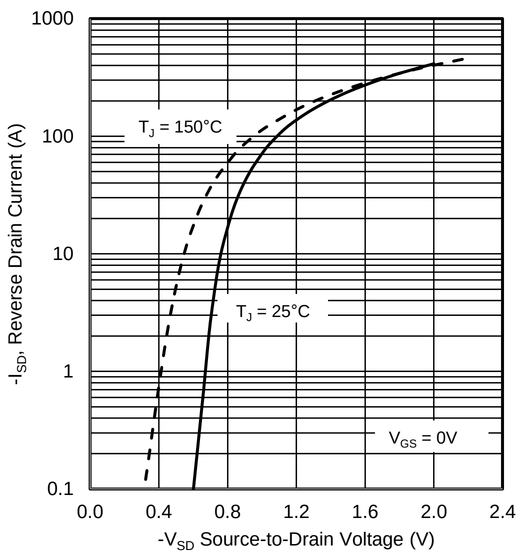


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

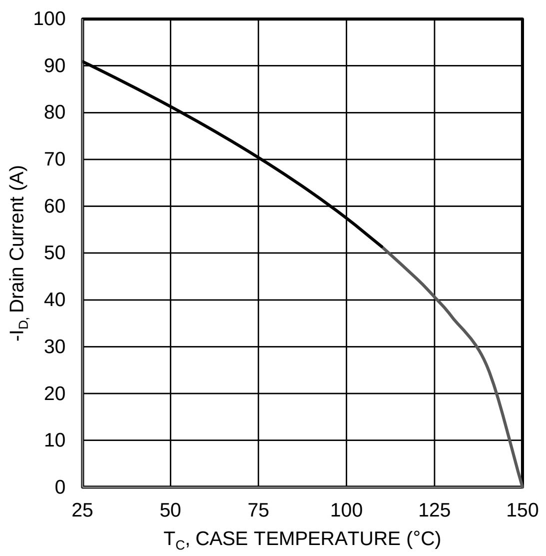
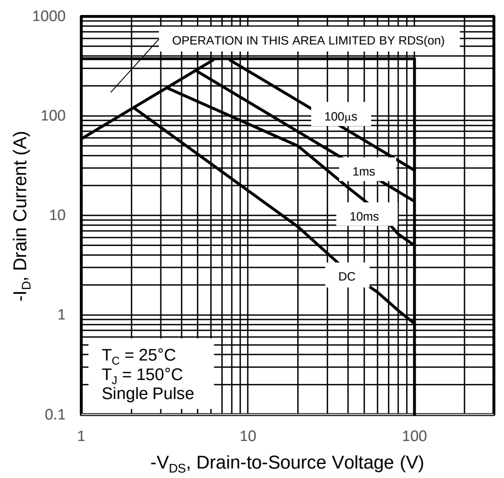


Figure 13 Maximum Drain Current Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)



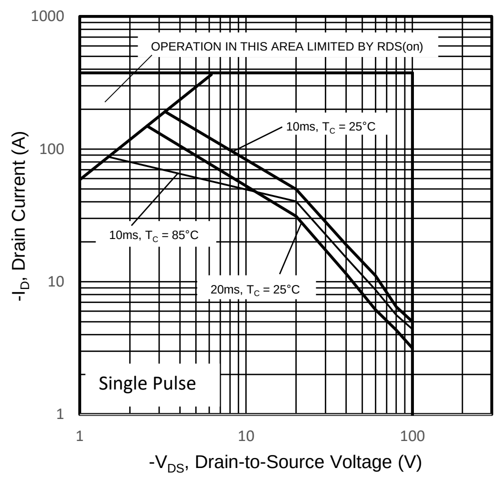


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Safe Operating Area

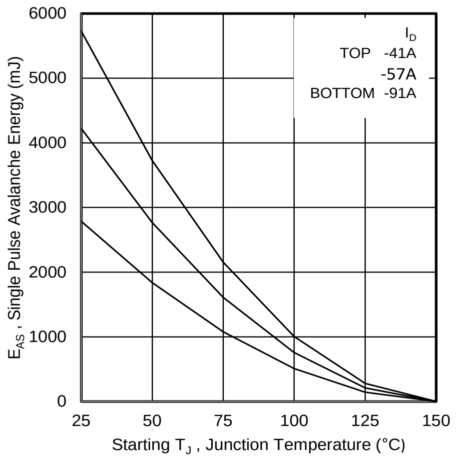


Figure 16 Maximum Avalanche Energy Vs. Junction Temperature

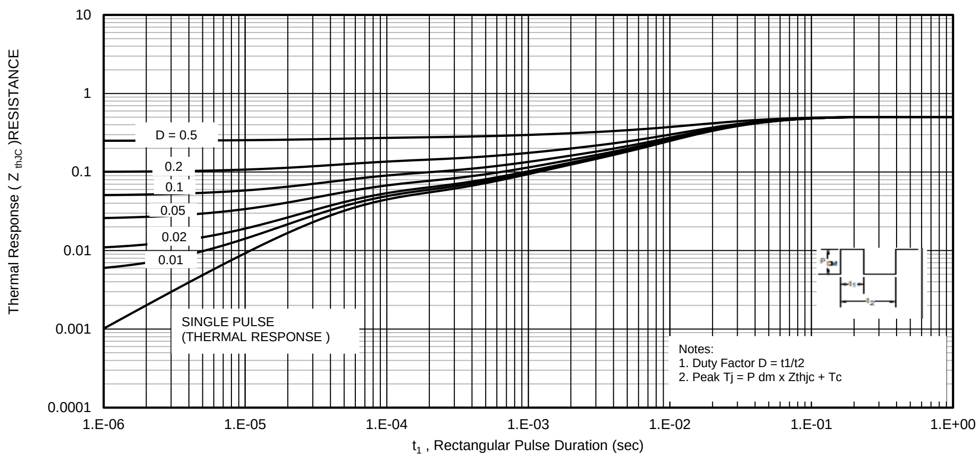


Figure 17 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

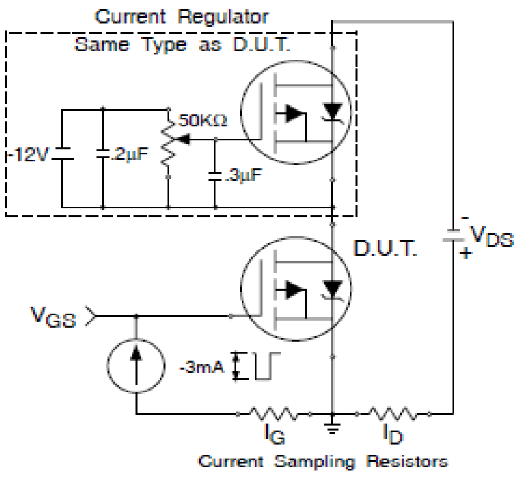


Figure 18 **Gate Charge Test Circuit**

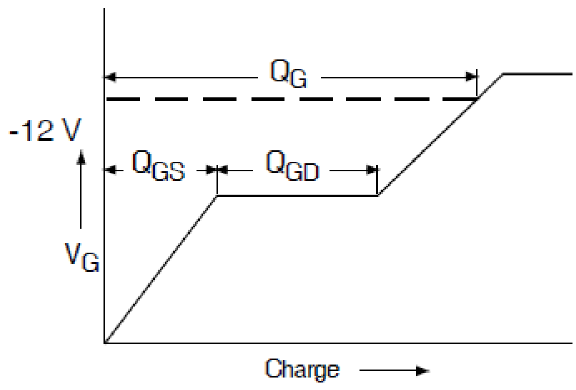


Figure 19 **Gate Charge Waveform**

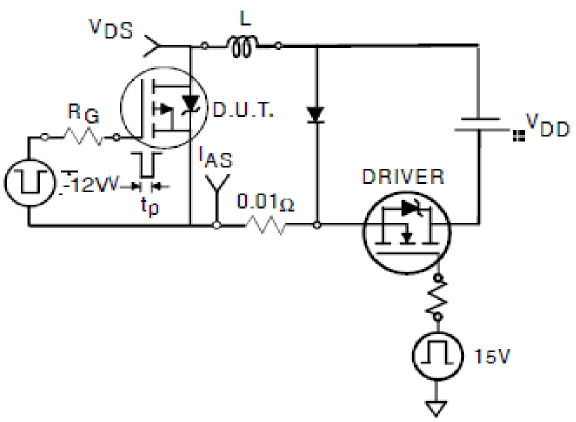


Figure 20 **Unclamped Inductive Test Circuit**

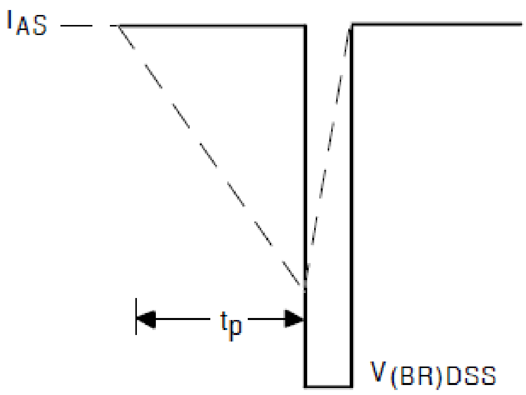


Figure 21 **Unclamped Inductive Waveform**

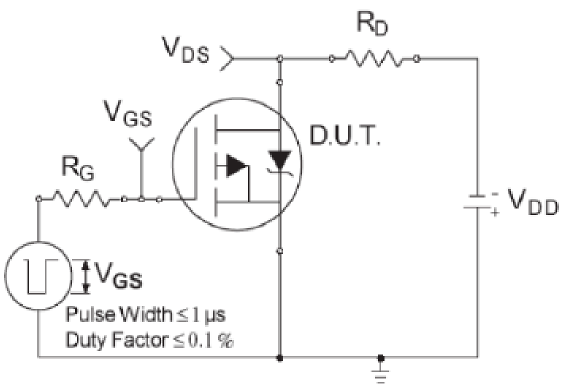


Figure 22 **Switching Time Test Circuit**

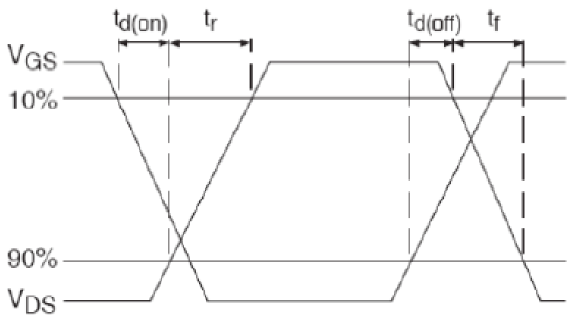
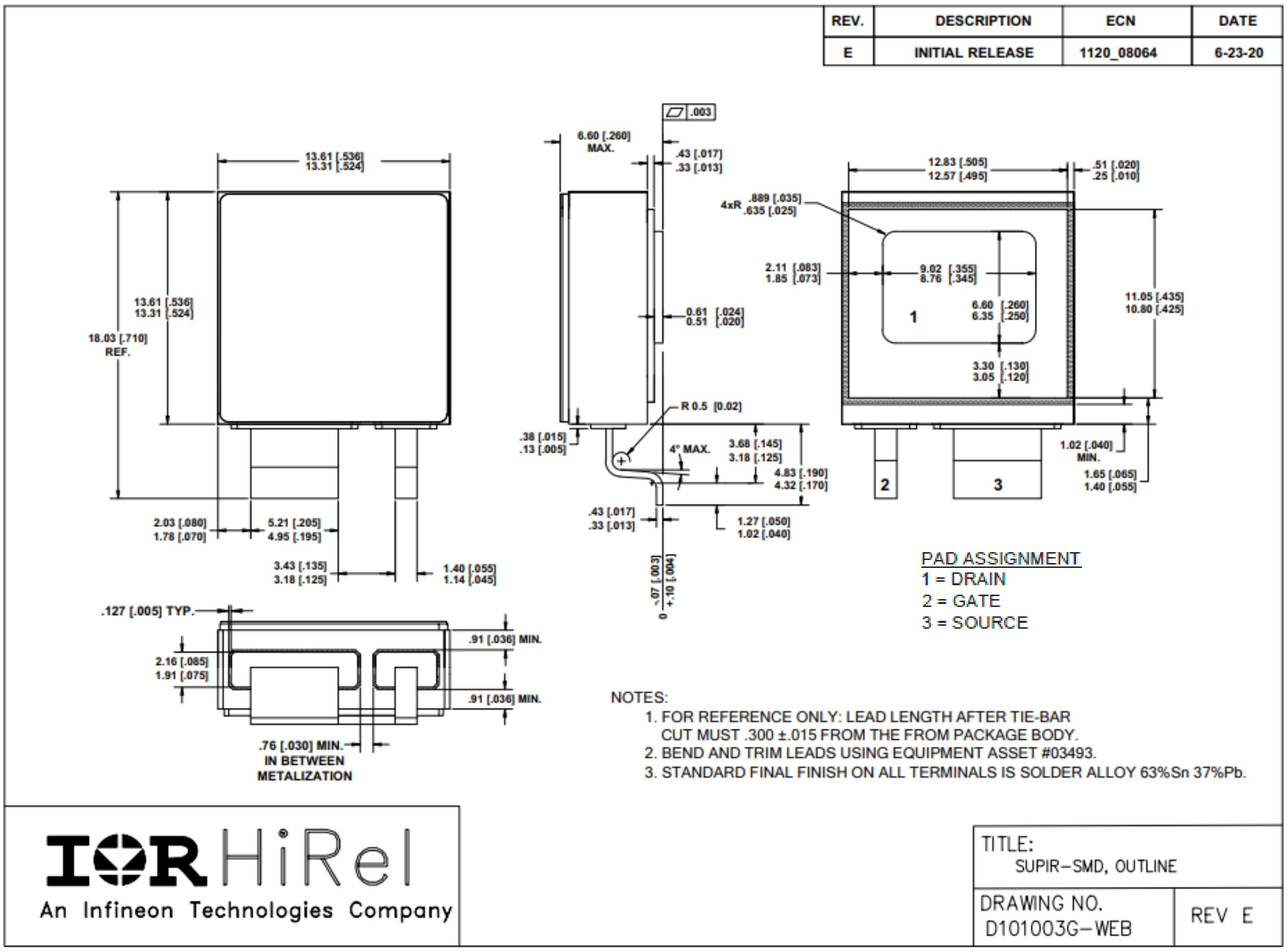


Figure 23 **Switching Time Waveforms**

5 Package Outline

Note: For the most updated package outline, please see the website: SupIR-SMD™



Revision history

Document version	Date of release	Description of changes
	03/21/2023	Preliminary datasheet with PPD number (PPD-97984)
Rev A	06/13/2023	Final datasheet with PD number (PD-97984A)

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