

IRHNS9A7160 (JANSR2N7653U2A)

PD-97930C

Radiation Hardened Power MOSFET Surface-Mount (SupIR-SMD™) 100V, 100A, N-channel, R9 Superjunction Technology

Features

- Single event effect (SEE) hardened (up to LET of 89.8 MeV·cm²/mg)
- Low R_{DS(on)}
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Direct-to-PCB attach
- Light weight
- ESD rating: class 3B per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 89.8 MeV·cm²/mg. Their combination of low R_{DS(on)} and fast switching times will allow for better performance in applications such as DC-DC converters or motor drives. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNS9A7160	SupIR-SMD™	COTS	100krad(Si)
JANSR2N7653U2A	SupIR-SMD™	JANS	100krad(Si)
IRHNS9A3160	SupIR-SMD™	COTS	300krad(Si)
JANSF2N7653U2A	SupIR-SMD™	JANS	300krad(Si)

Product Summary

- **Part number:** IRHNS9A7160 (JANSR2N7653U2A), IRHNS9A3160 (JANSF2N7653U2A)
- **REF:** MIL-PRF-19500/777
- **Radiation level:** 100 krad (Si), 300 krad (Si)
- **R_{DS(on), max}:** 6.5mΩ
- **I_D:** 100A*

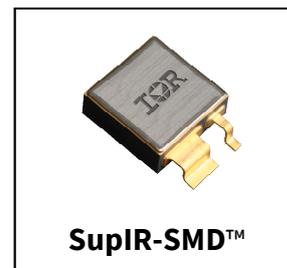


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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 12V, T_C = 25^\circ C$	Continuous Drain Current	100*	A
$I_{D2} @ V_{GS} = 12V, T_C = 100^\circ C$	Continuous Drain Current	93	A
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current ¹	400	A
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	3027	mJ
I_{AR}	Avalanche Current ¹	93	A
E_{AR}	Repetitive Avalanche Energy ¹	25	mJ
dv/dt	Peak Diode Reverse Recovery ³	24	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	

* Current is limited by package

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² $V_{DD} = 100V$, starting $T_J = 25^\circ C$, $L = 0.7mH$, Peak $I_L = 93A$, $V_{GS} = 20V$

³ $I_{SD} \leq 93A$, $di/dt \leq 2190A/\mu s$, $V_{DD} \leq 100V$, $T_J \leq 150^\circ C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	6.5	mΩ	V _{GS} = 12V, I _{D2} = 93A ¹
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} ≥ V _{GS} , I _D = 6.0mA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-8.1	—	mV/°C	
G _{fs}	Forward Transconductance	68	—	—	S	V _{DS} = 15V, I _{D2} = 93A ¹
I _{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	25		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	195	nC	I _{D1} = 100A
Q _{GS}	Gate-to-Source Charge	—	—	67		V _{DS} = 50V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	52		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time	—	—	41	ns	I _{D1} = 100A ^{**} V _{DD} = 50V R _G = 2.4Ω V _{GS} = 12V
t _r	Rise Time	—	—	101		
t _{d(off)}	Turn-Off Delay Time	—	—	98		
t _f	Fall Time	—	—	28		
L _s + L _D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C _{iss}	Input Capacitance	—	9808	—	pF	V _{GS} = 0V V _{DS} = 25V f = 100KHz
C _{oss}	Output Capacitance	—	2407	—		
C _{rss}	Reverse Transfer Capacitance	—	15	—		
R _G	Gate Resistance	—	1.1	—	Ω	f = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	100	A	
I_{SM}	Pulsed Source Current (Body Diode) ¹	—	—	400	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 100\text{A}$, $V_{GS} = 0\text{V}$ ²
t_{rr}	Reverse Recovery Time	—	168	252	ns	$T_J = 25^\circ\text{C}$, $I_F = 100\text{A}$, $V_{DD} \leq 25\text{V}$ $di/dt = -100\text{A}/\mu\text{s}$ ²
Q_{rr}	Reverse Recovery Charge	—	1331	—	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.50	$^\circ\text{C}/\text{W}$
$R_{\theta J-PCB}$	Junction-to-PC Board (Soldered to 2" sq.inch copper clad board)	—	1.6	—	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics - Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation^{3, 4}

Symbol	Parameter	Up to 300krads (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	V	$V_{GS} = 0\text{V}$, $I_D = 1\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	$V_{DS} \geq V_{GS}$, $I_D = 6.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -20\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	8.0	$\text{m}\Omega$	$V_{GS} = 12\text{V}$, $I_{D2} = 75\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SupIR-SMD) ²	—	6.5	$\text{m}\Omega$	$V_{GS} = 12\text{V}$, $I_{D2} = 93\text{A}$
V_{SD}	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0\text{V}$, $I_F = 75\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 12\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 80\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part numbers IRHNS9A7160 (JANSR2N7653U2A) and IRHNS9A3160 (JANSF2N7653U2A)

Device Characteristics

2.4.2 Single Event Effects – Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)			
			V _{GS} = 0V	V _{GS} = -1V	V _{GS} = -5V	V _{GS} = -10V
37 ± 5%	417 ± 7.5%	50 ± 7.5%	100	100	100	100
59.8 ± 5%	753 ± 7.5%	60 ± 7.5%	100	100	100	100
89.8 ± 5%	1515 ± 7.5%	82 ± 7.5%	100	100	—	—

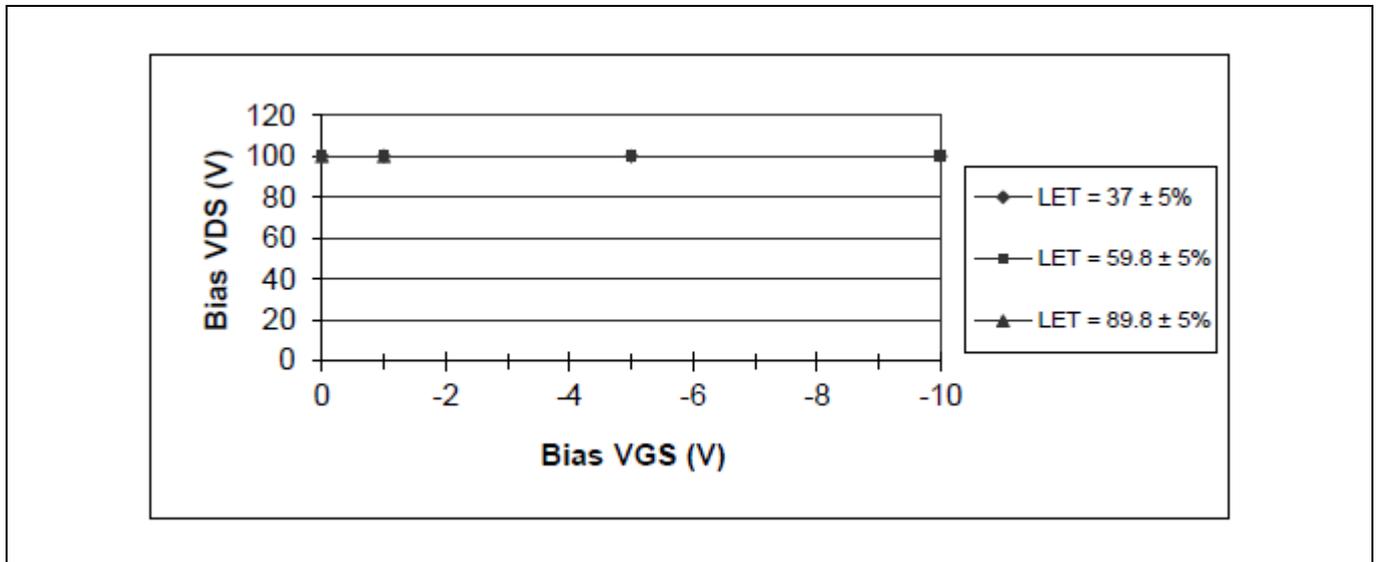


Figure 1 Typical Single Event Effect, Safe Operating Area

Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

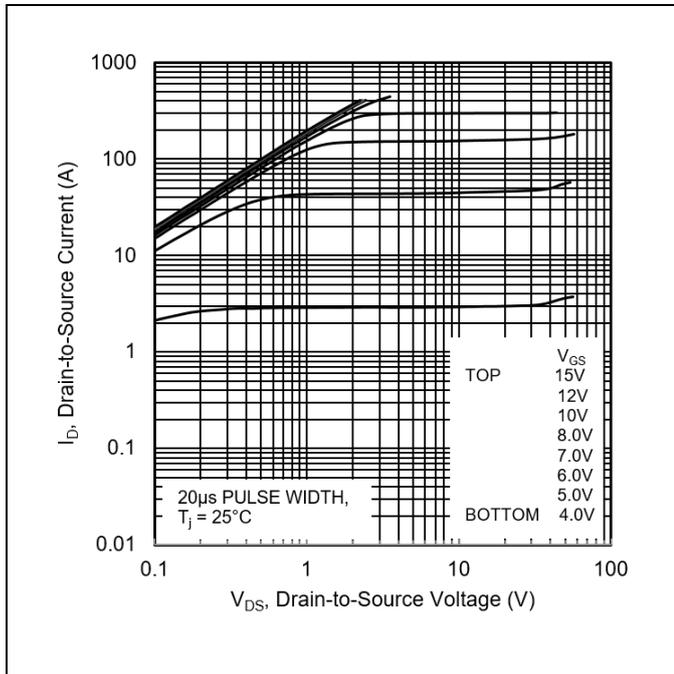


Figure 2 Typical Output Characteristics

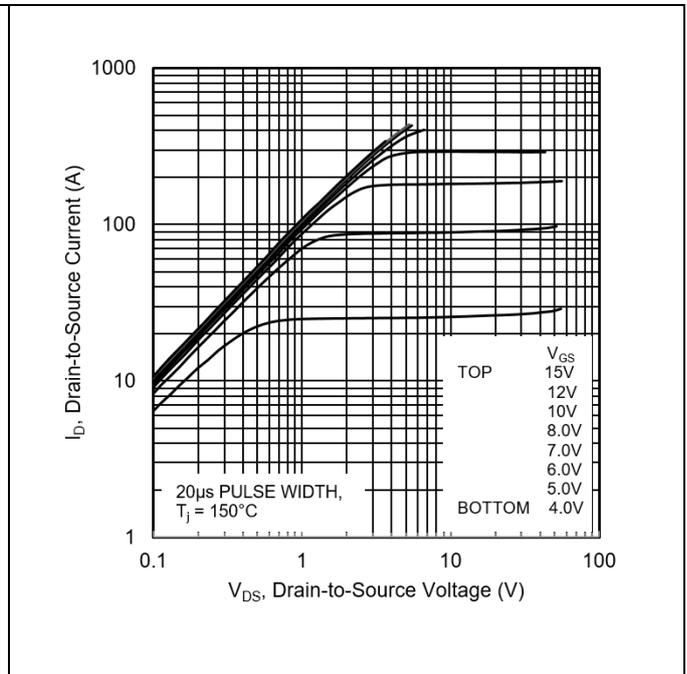


Figure 3 Typical Output Characteristics

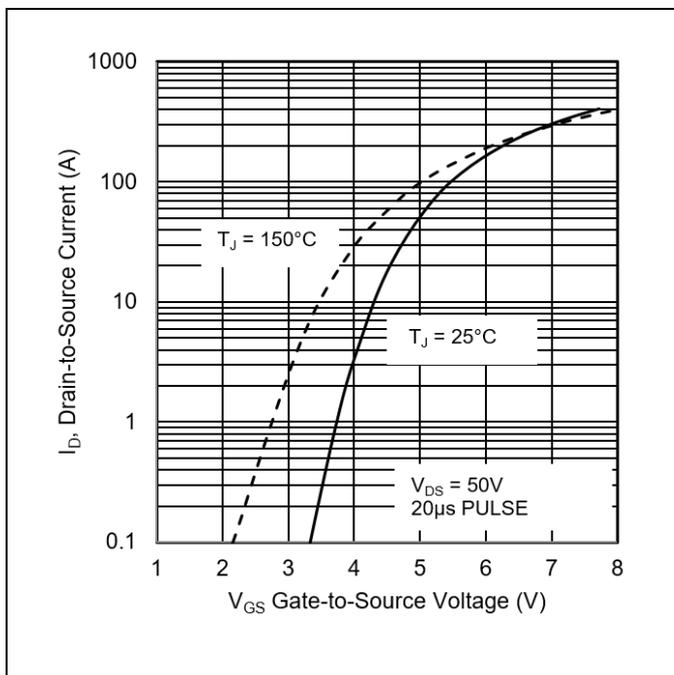


Figure 4 Typical Transfer Characteristics

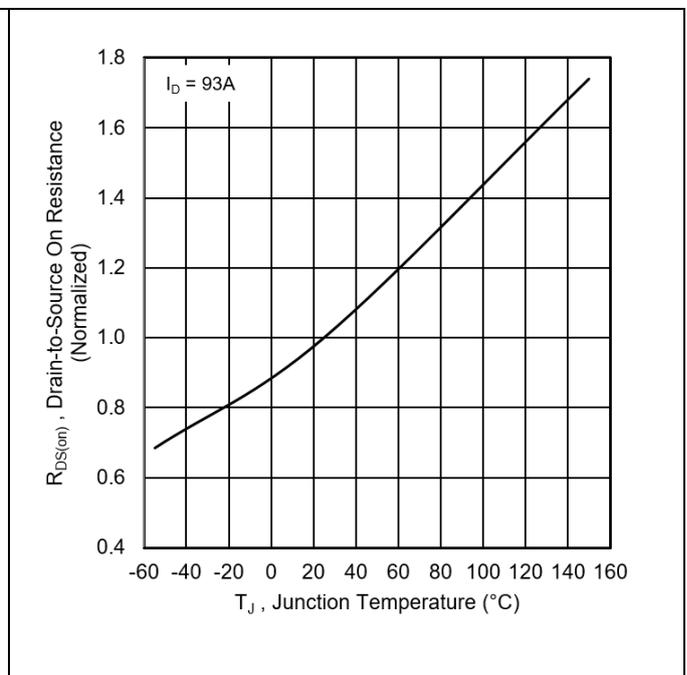


Figure 5 Normalized On-Resistance Vs. Temperature

IRHNS9A7160 (JANSR2N7653U2A)
Radiation Hardened Power MOSFET (SupIR-SMD™)
Electrical Characteristics Curves (Pre-irradiation)

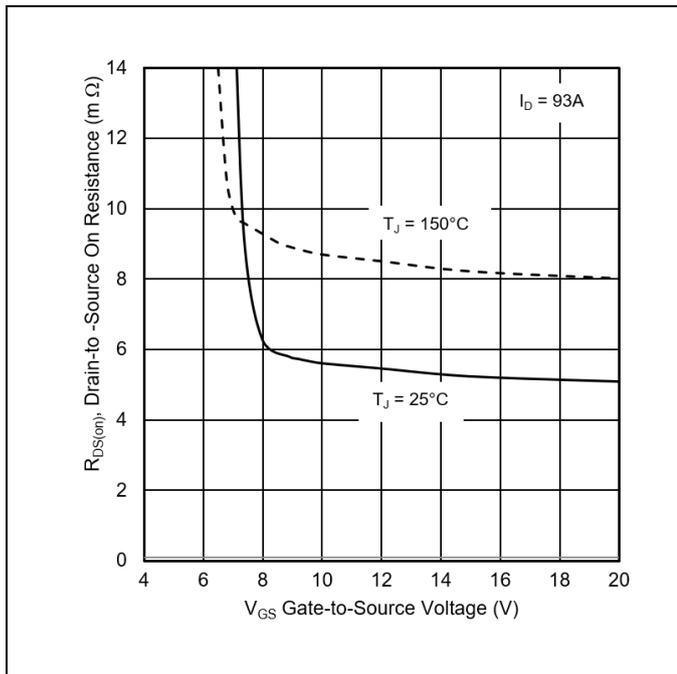


Figure 6 Typical On-Resistance Vs. Gate Voltage

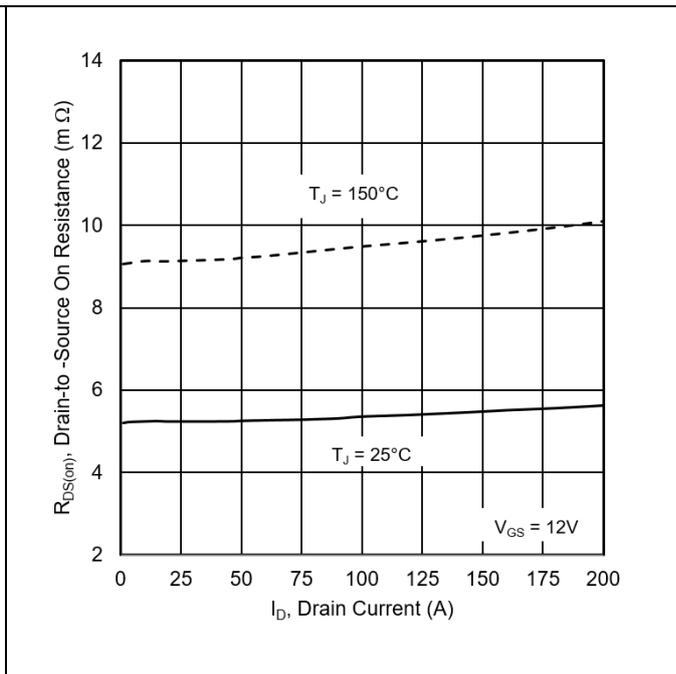


Figure 7 Typical On-Resistance Vs. Drain Current

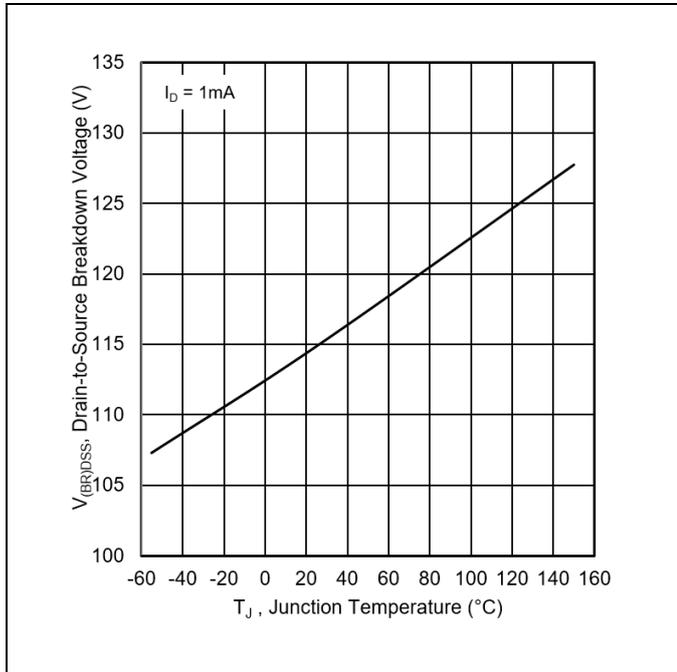


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

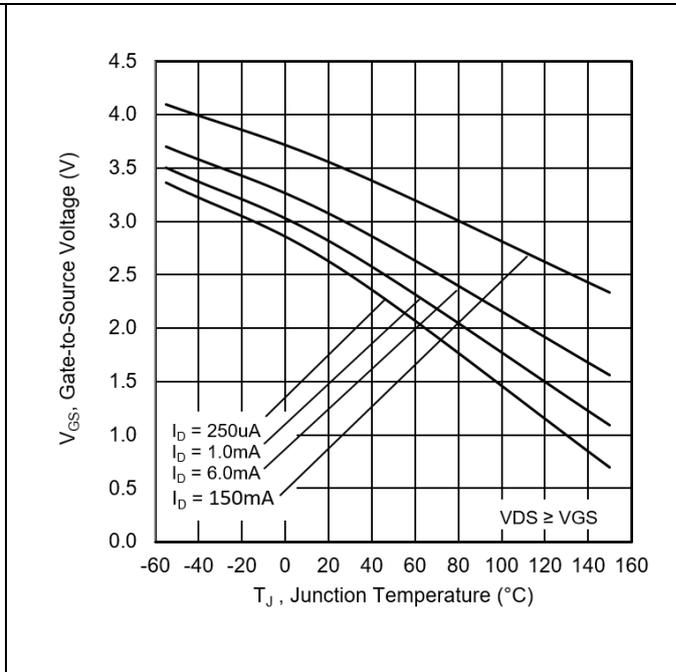


Figure 9 Typical Threshold Voltage Vs. Temperature

IRHNS9A7160 (JANSR2N7653U2A)
Radiation Hardened Power MOSFET (SupIR-SMD™)
Electrical Characteristics Curves (Pre-irradiation)

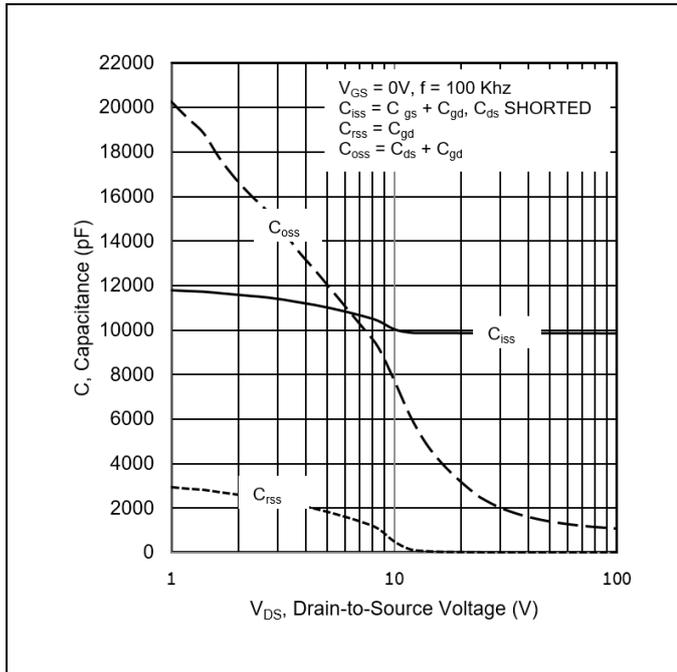


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

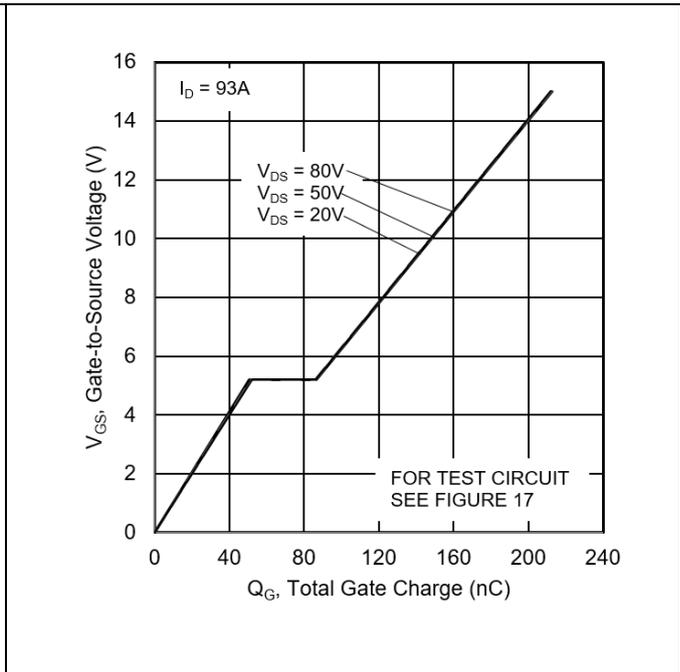


Figure 11 Typical Gate-to-Source Voltage Vs. Gate Charge

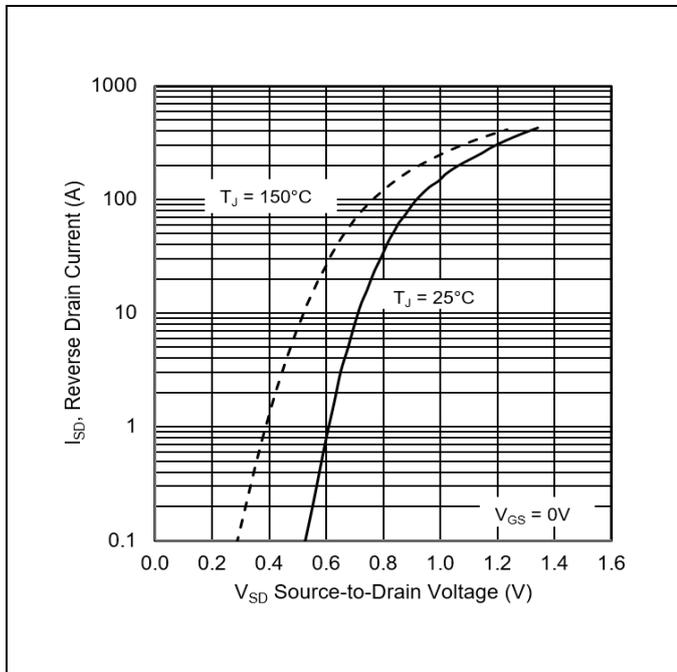


Figure 12 Typical Source-Drain Vs. Diode Forward Voltage

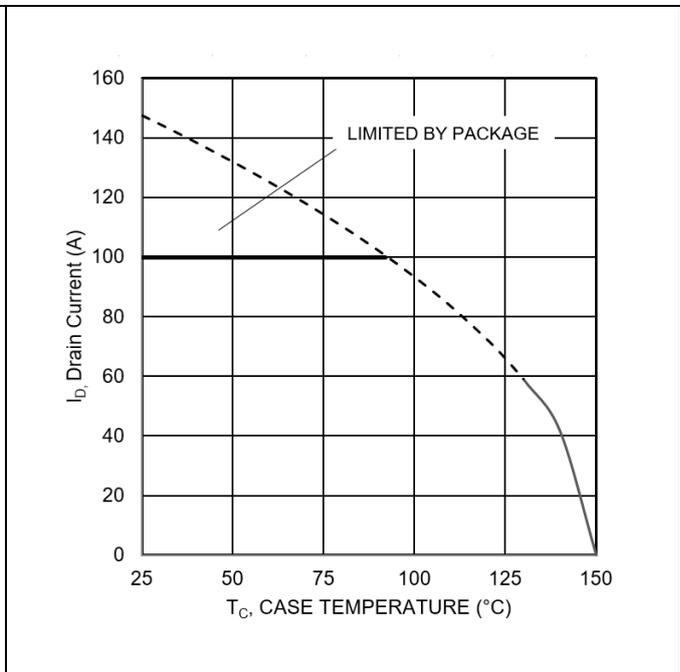


Figure 13 Maximum Drain Current Vs. Case Temperature

IRHNS9A7160 (JANSR2N7653U2A)
Radiation Hardened Power MOSFET (SupIR-SMD™)

Electrical Characteristics Curves (Pre-irradiation)

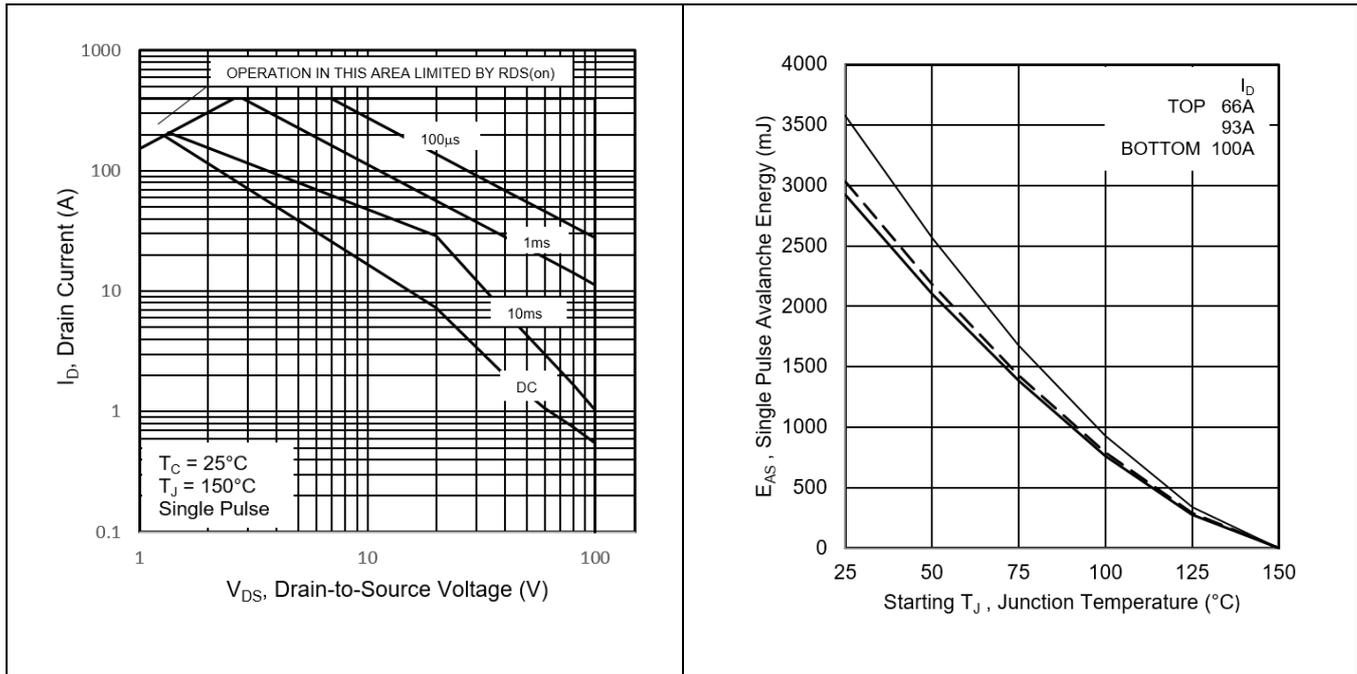


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Avalanche Energy Vs. Drain Current

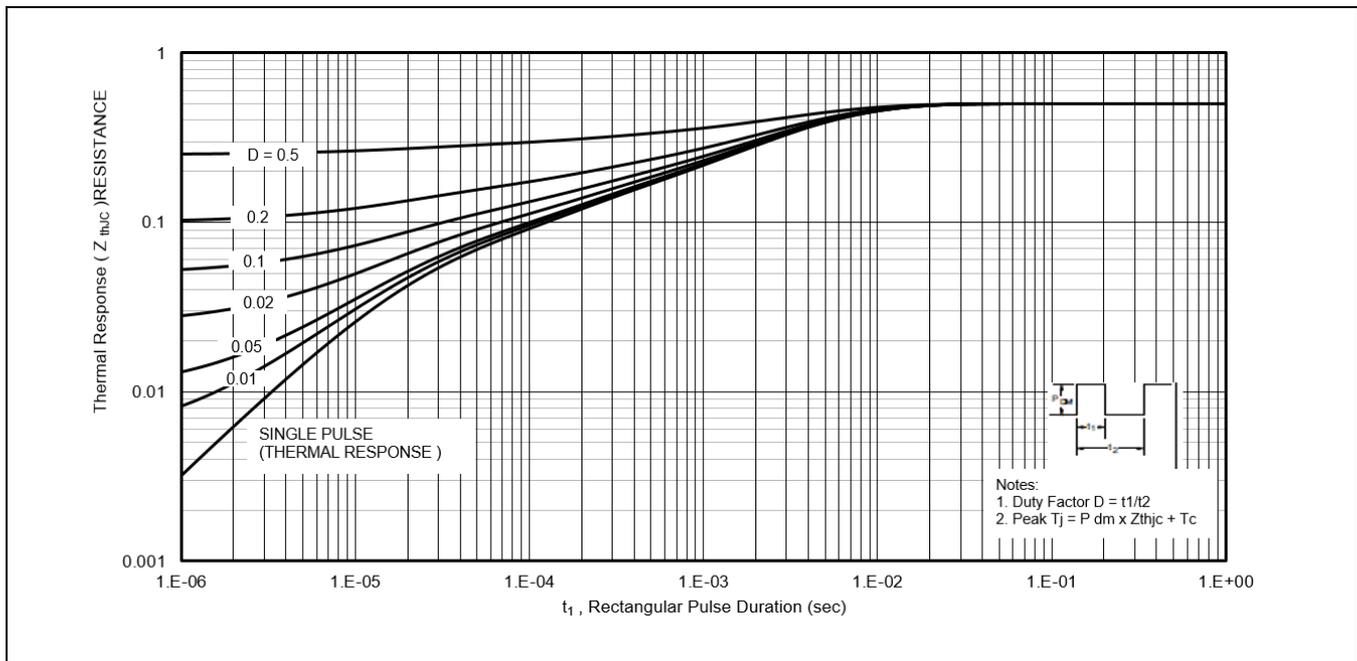


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRHNS9A7160 (JANSR2N7653U2A)
Radiation Hardened Power MOSFET (SupIR-SMD™)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

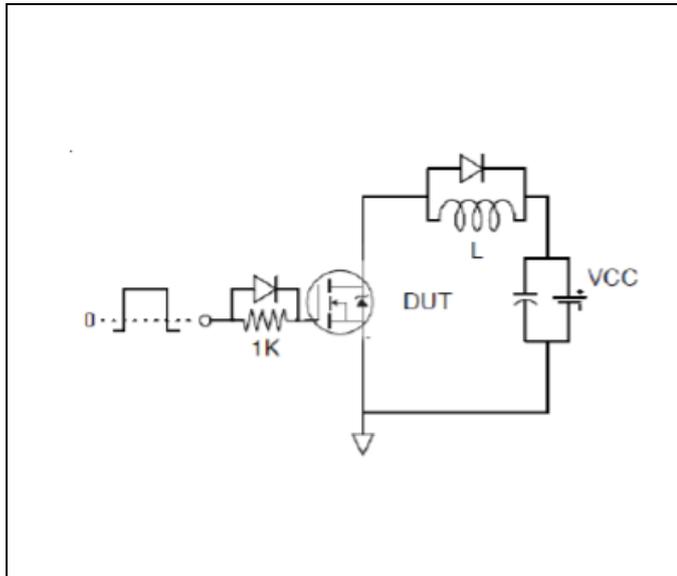


Figure 17 Gate Charge Test Circuit

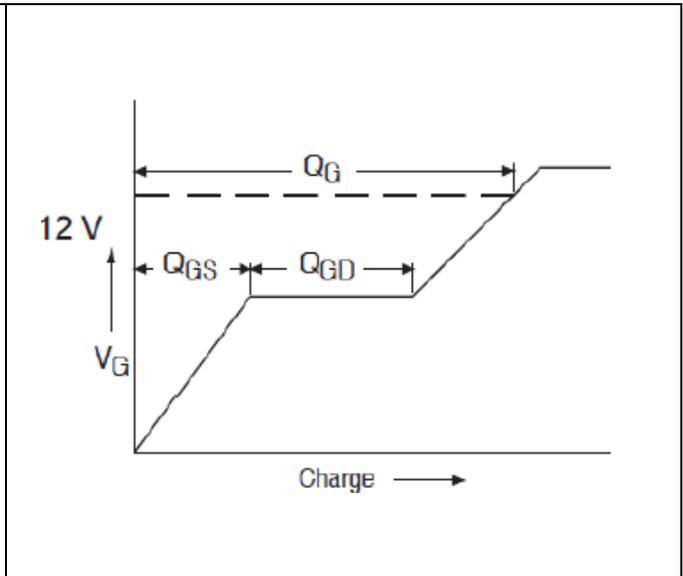


Figure 18 Gate Charge Waveform

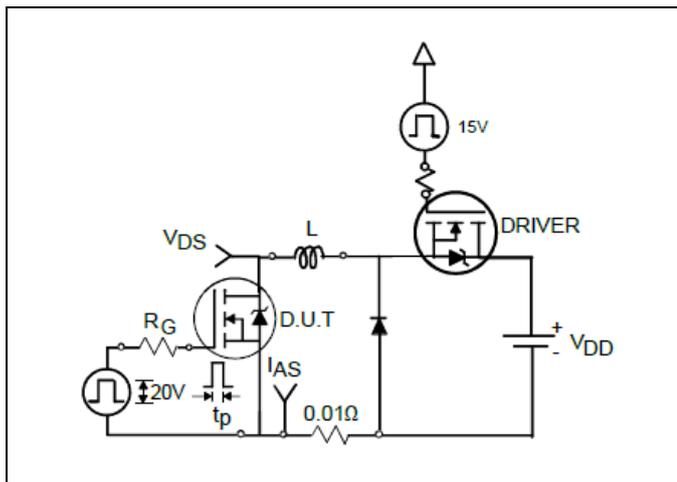


Figure 19 Unclamped Inductive Test Circuit

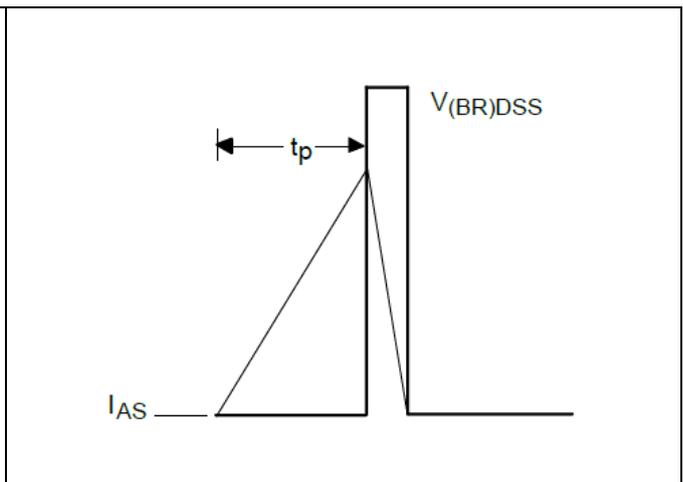


Figure 20 Unclamped Inductive Waveform

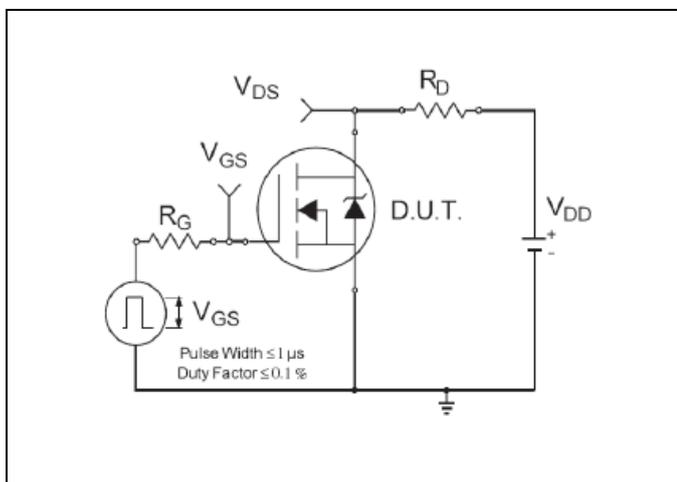


Figure 21 Switching Time Test Circuit

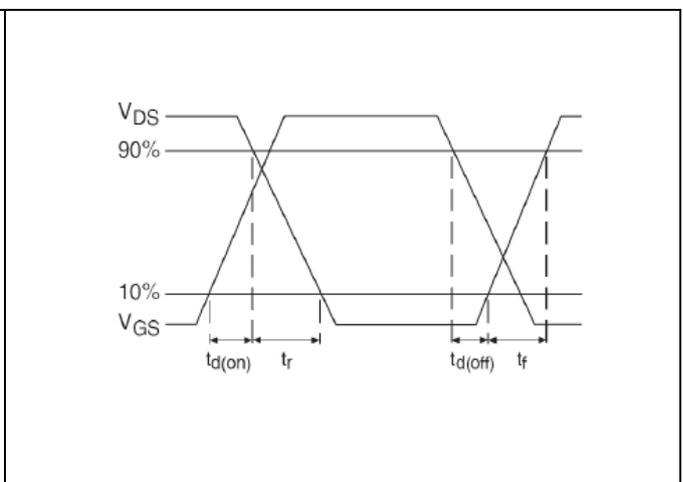


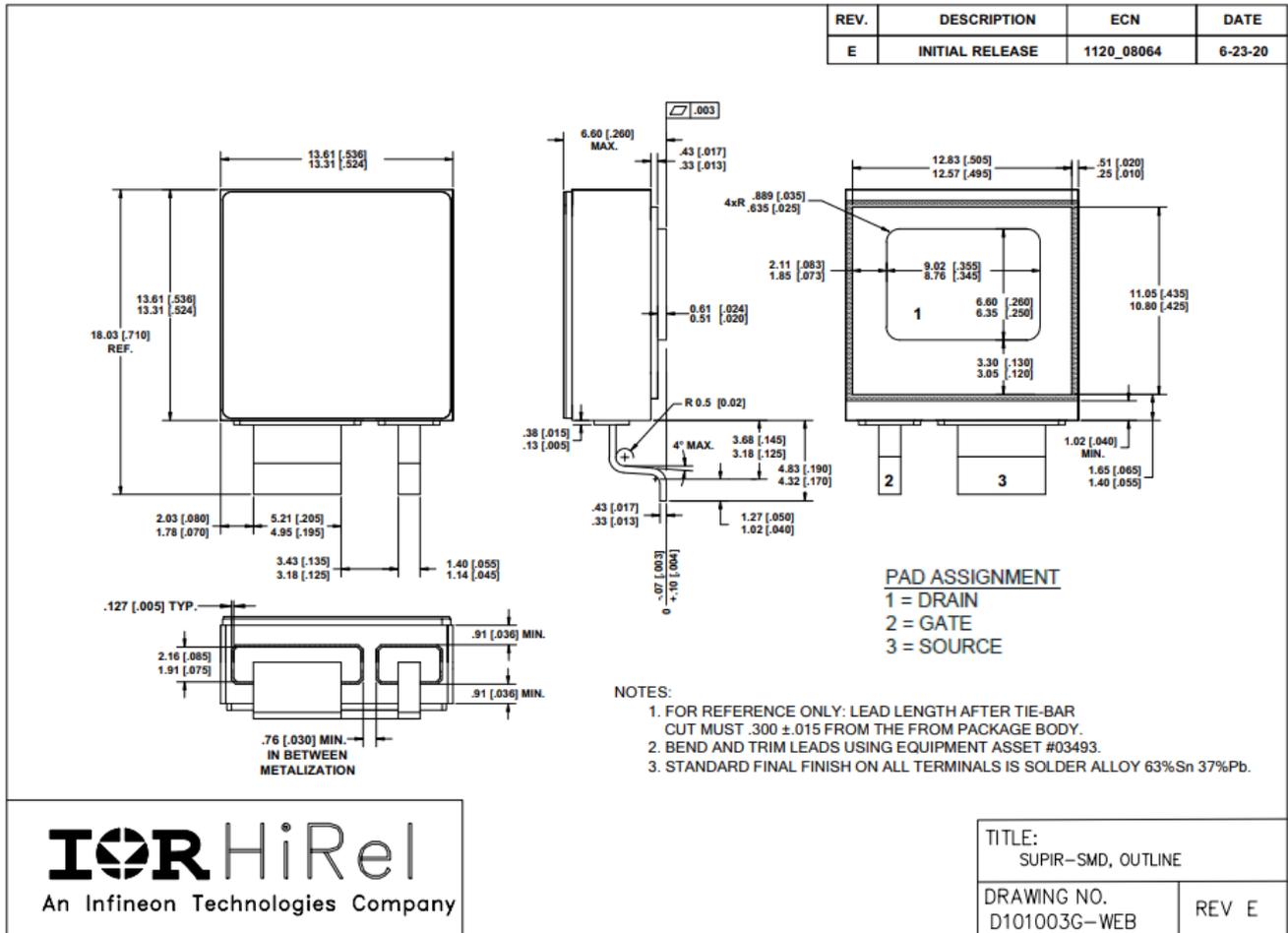
Figure 22 Switching Time Waveforms

IRHNS9A7160 (JANSR2N7653U2A)
Radiation Hardened Power MOSFET (SupIR-SMD™)

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [SupIR-SMD](http://www.infineon.com/SUPIR-SMD)



IRHNS9A7160 (JANSR2N7653U2A)

Radiation Hardened Power MOSFET (SupIR-SMD™)

Revision history

Revision history

Document version	Date of release	Description of changes
	09/22/2021	Preliminary datasheet with PPD number (PPD-97930A)
Rev B	09/27/2021	Final datasheet with PD number
Rev C	01/21/2022	Updated based on ECN-1120_8889

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Edition 2022-01-21

Published by

**International Rectifier HiRel Products,
Inc.**

**An Infineon Technologies company
El Segundo, California 90245 USA**

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