

IRHNKC9A97130 (JANSR2N7660U3CE)

PD-97998B

Radiation Hardened Power MOSFET
Surface Mount (SMD-0.5e Ceramic Lid)
-100V, -24A, P-channel, R9 Superjunction Technology

Features

- Single event effect (SEE) hardened (up to LET of 91.2 MeV·cm²/mg)
- Low $R_{DS(on)}$
- Rugged SOA
- Improved Avalanche Energy
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Light weight
- Surface mount
- ESD rating: Class 2 per MIL-STD-750, Method 1020

Potential Applications

- Power distribution
- Latching current limiter
- Motor drives
- DC-DC converter

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 91.2 MeV·cm²/mg. Their combination of low $R_{DS(on)}$ and improved SOA will allow for better performance in applications such as Latching Current Limiters or Solid-State Power Controllers. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 **Ordering options**

Part number	Package	Screening Level	TID Level
IRHNKC9A97130	SMD-0.5e (Ceramic Lid)	COTS	100 krad(Si)
JANSR2N7660U3CE	SMD-0.5e (Ceramic Lid)	JANS	100 krad(Si)
IRHNKC9A93130	SMD-0.5e (Ceramic Lid)	COTS	300 krad(Si)
JANSF2N7660U3CE	SMD-0.5e (Ceramic Lid)	JANS	300 krad(Si)

Product Summary

- **BV_{DSS}** : -100V
- **I_D** : -24A
- **$R_{DS(on),max}$** : 72mΩ
- **Q_{Gmax}** : 50nC
- **REF**: MIL-PRF-19500/780



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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = -12V, T_C = 25^{\circ}C$	Continuous Drain Current	-24	A
$I_{D2} @ V_{GS} = -12V, T_C = 100^{\circ}C$	Continuous Drain Current	-15	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	-96	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	810	mJ
I_{AR}	Avalanche Current ¹	-15	A
E_{AR}	Repetitive Avalanche Energy ¹	7.5	mJ
dv/dt	Peak Diode Reverse Recovery ³	-11	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	1.0 (Typical)	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² $V_{DD} = -100V$, starting $T_J = 25^{\circ}C$, $L = 7.2mH$, Peak $I_L = -15A$, $V_{GS} = -20V$

³ $I_{SD} \leq -24A$, $di/dt \leq -1050A/\mu s$, $V_{DD} \leq -100V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	72	m Ω	$V_{GS} = -12V, I_{D2} = -15A^1$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} \geq V_{GS}, I_D = -1mA$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	5.6	—	mV/ $^\circ\text{C}$	
G_{fs}	Forward Transconductance	14	—	—	S	$V_{DS} = -15V, I_{D2} = -15A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-10	μA	$V_{DS} = -80V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 20V$
Q_G	Total Gate Charge	—	—	50	nC	$I_{D1} = -24A$
Q_{GS}	Gate-to-Source Charge	—	—	16		$V_{DS} = -50V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	12		$V_{GS} = -12V$
$t_{d(on)}$	Turn-On Delay Time	—	—	18	ns	$I_{D1} = -24A^{**}$ $V_{DD} = -50V$ $R_G = 7.5\Omega$ $V_{GS} = -12V$
t_r	Rise Time	—	—	48		
$t_{d(off)}$	Turn-Off Delay Time	—	—	74		
t_f	Fall Time	—	—	39		
$L_s + L_D$	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	2465	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	524	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	14	—		$f = 1.0MHz$
R_G	Gate Resistance	—	5.6	—	Ω	$f = 1.0MHz$, open drain

****** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-24	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	-196	A	
V _{SD}	Diode Forward Voltage	—	—	-1.3	V	T _J = 25°C, I _S = -24A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	73	110	ns	T _J = 25°C, I _F = -24A, V _{DD} ≤ -25V di/dt = -100A/μs
Q _{rr}	Reverse Recovery Charge	—	258	—	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	$^\circ\text{C}/\text{W}$

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	Up to 300 krad (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	V	$V_{GS} = 0\text{V}$, $I_D = -1.0\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	V	$V_{DS} \geq V_{GS}$, $I_D = -1.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	$V_{GS} = -20\text{V}$
	Gate-to-Source Leakage Reverse	—	100		$V_{GS} = 20\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	μA	$V_{DS} = -80\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	73	$\text{m}\Omega$	$V_{GS} = -12\text{V}$, $I_{D2} = -15\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-0.5e) ²	—	72	$\text{m}\Omega$	$V_{GS} = -12\text{V}$, $I_{D2} = -15\text{A}$
V_{SD}	Diode Forward Voltage	—	-1.3	V	$V_{GS} = 0\text{V}$, $I_F = -24\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = -12\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = -80\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part numbers IRHNKC9A97130 (JANSR2N7660U3CE) and IRHNKC9A93130 (JANSF2N7660U3CE)

IRHNKC9A97130 (JANSR2N7660U3CE)
Radiation Hardened Power MOSFET (SMD-0.5e)

Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)			
			V _{GS} = 0V	V _{GS} = 1V	V _{GS} = 5V	V _{GS} = 10V
38.5 ± 2%	336.5 ± 5%	41.4 ± 5%	-100	-100	-100	-100
61.3 ± 2%	623.5 ± 5%	51.5 ± 5%	-100	-100	-100	---
91.2 ± 2%	1322.5 ± 5%	72.9 ± 5%	-100	-100	—	—

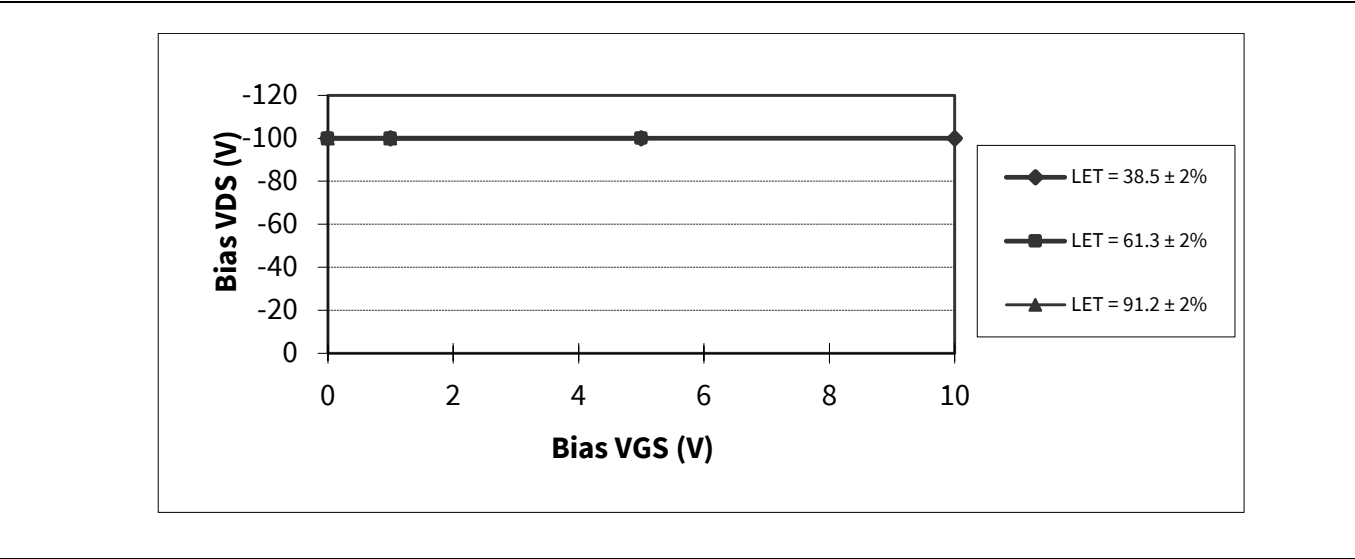


Figure 1 Typical Single Event Effect, Safe Operating Area

IRHNKC9A97130 (JANSR2N7660U3CE)
Radiation Hardened Power MOSFET (SMD-0.5e)

Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

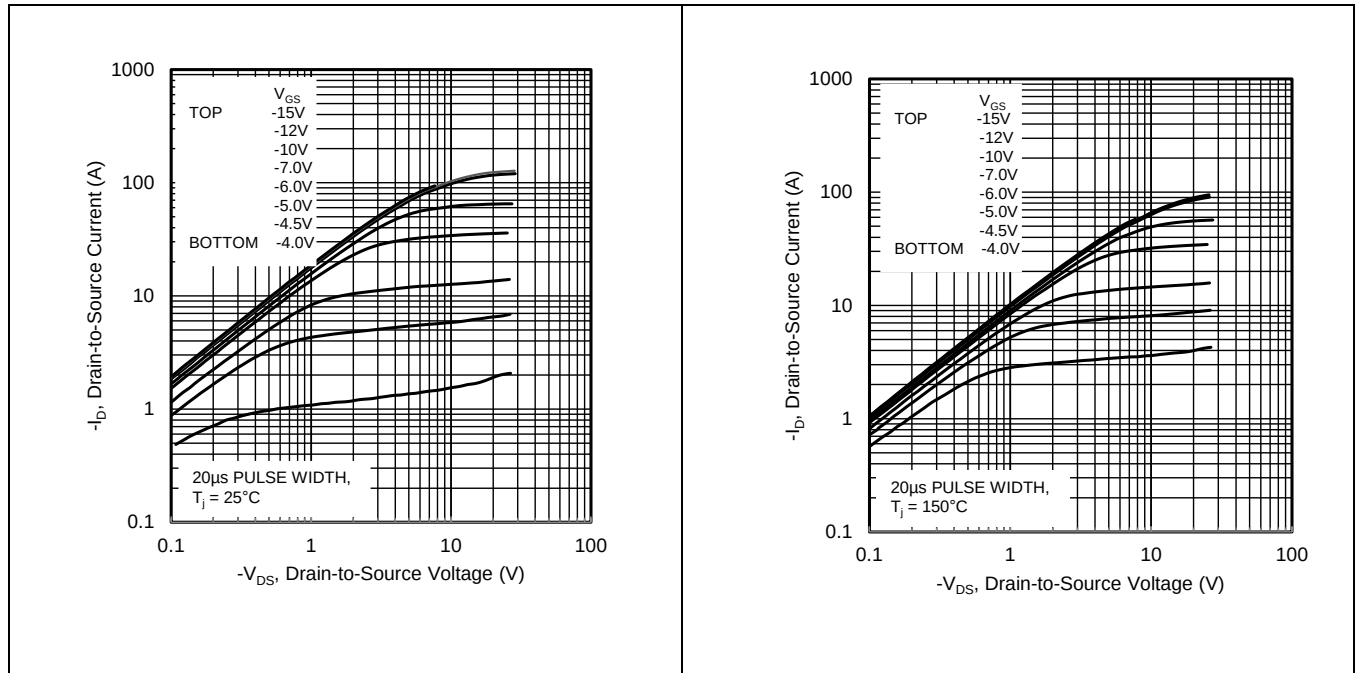


Figure 2 Typical Output Characteristics

Figure 3 Typical Output Characteristics

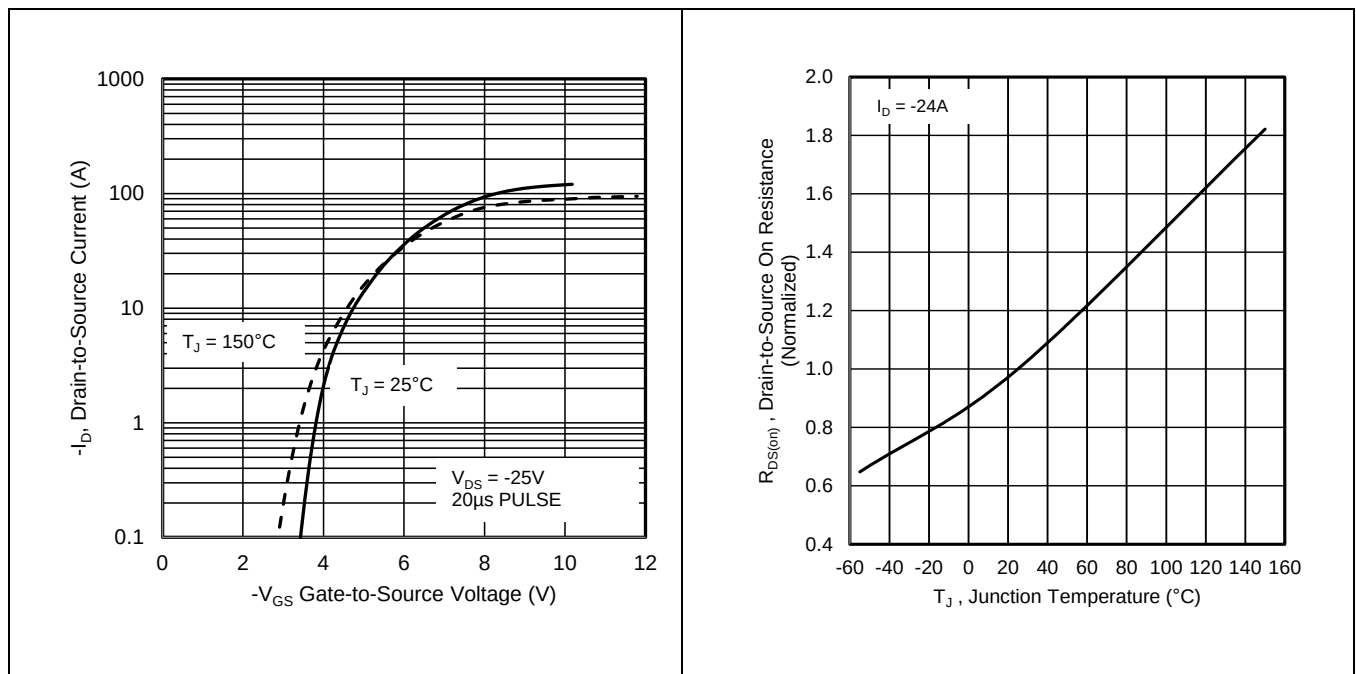


Figure 4 Typical Transfer Characteristics

Figure 5 Normalized On-Resistance Vs. Temperature

IRHNKC9A97130 (JANSR2N7660U3CE)

Radiation Hardened Power MOSFET (SMD-0.5e)

Electrical Characteristics Curves (Pre-irradiation)

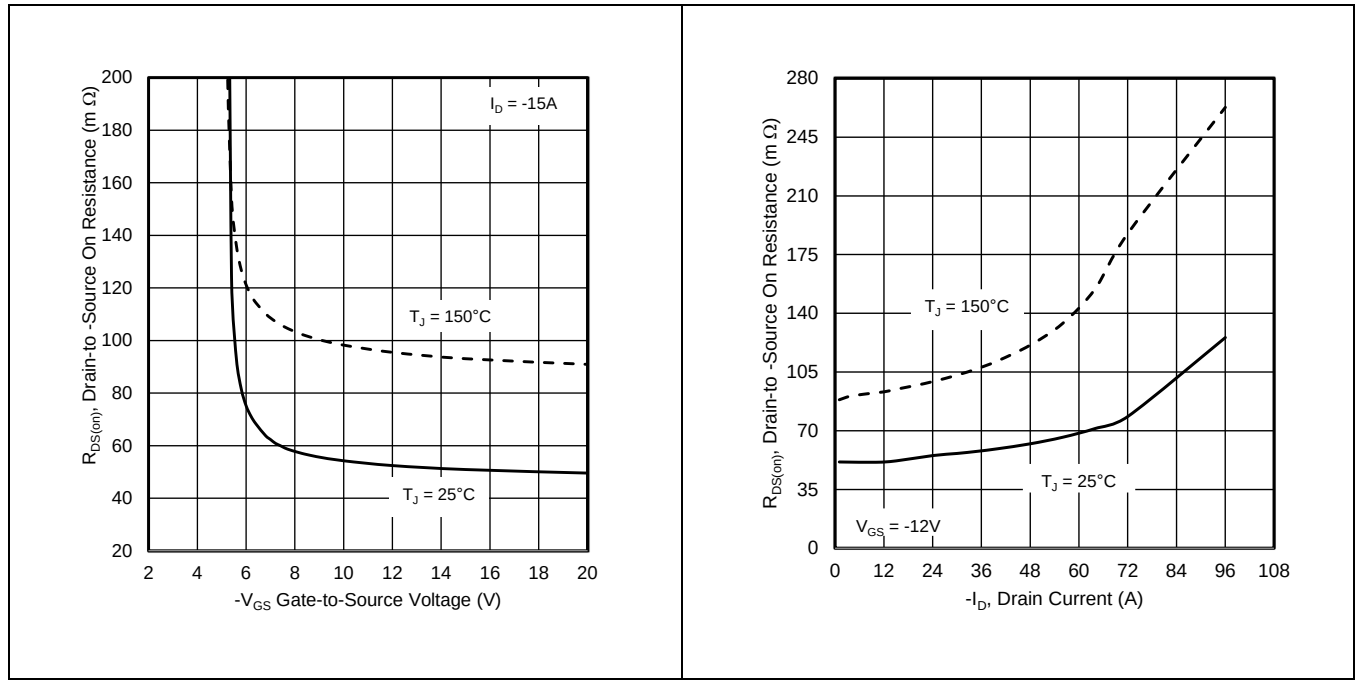


Figure 6 Typical On-Resistance Vs Gate Voltage **Figure 7 Typical On-Resistance Vs Drain Current**

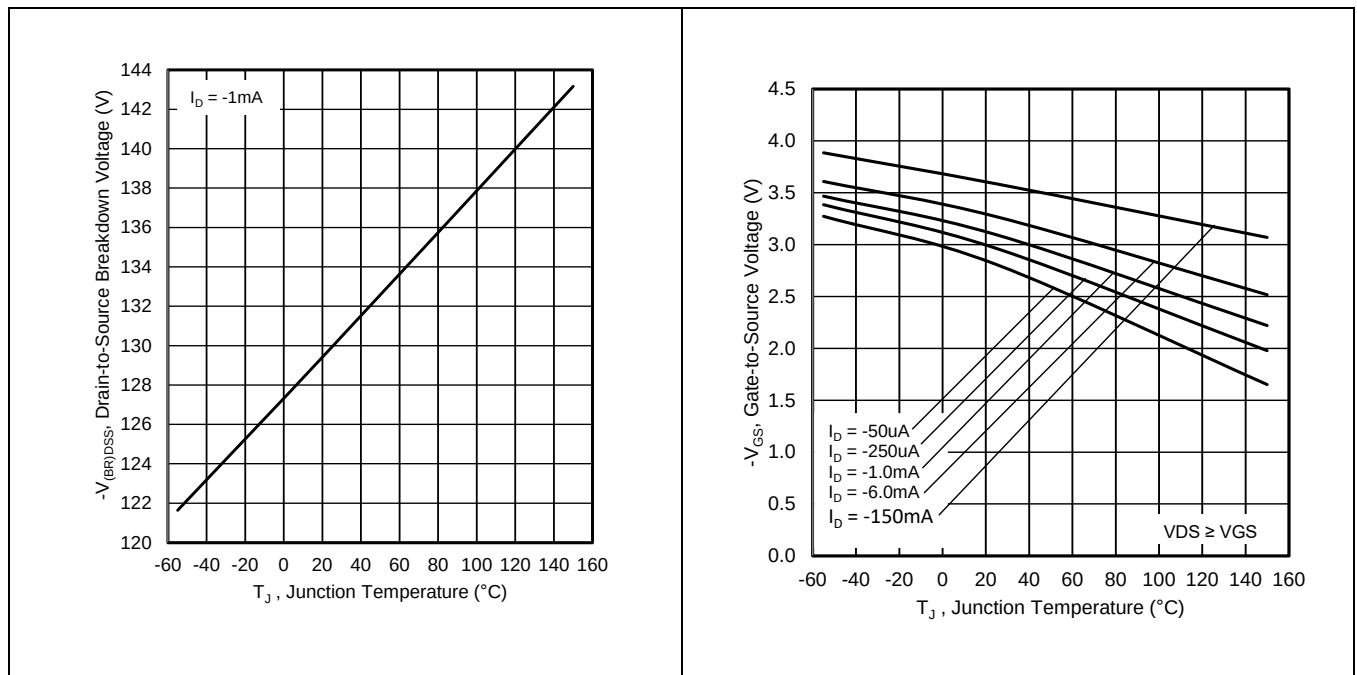


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature **Figure 9 Typical Threshold Voltage Vs. Temperature**

IRHNKC9A97130 (JANSR2N7660U3CE)
Radiation Hardened Power MOSFET (SMD-0.5e)

Electrical Characteristics Curves (Pre-irradiation)

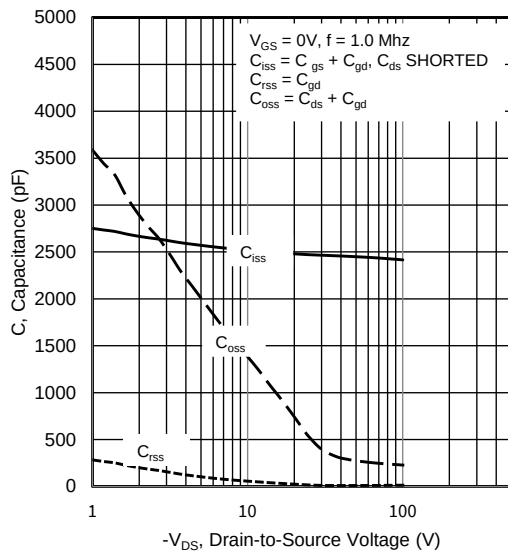


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

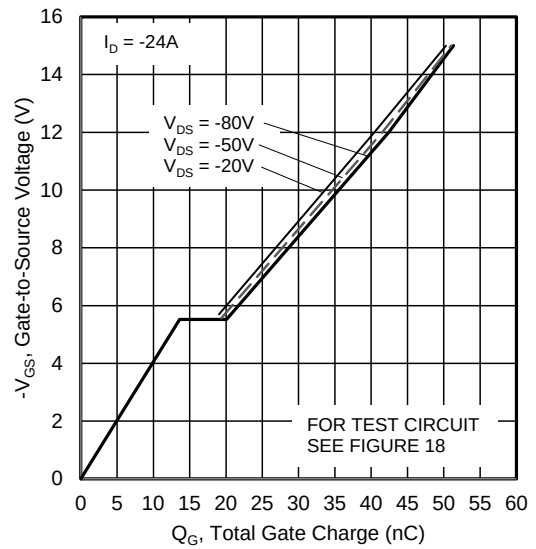


Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge

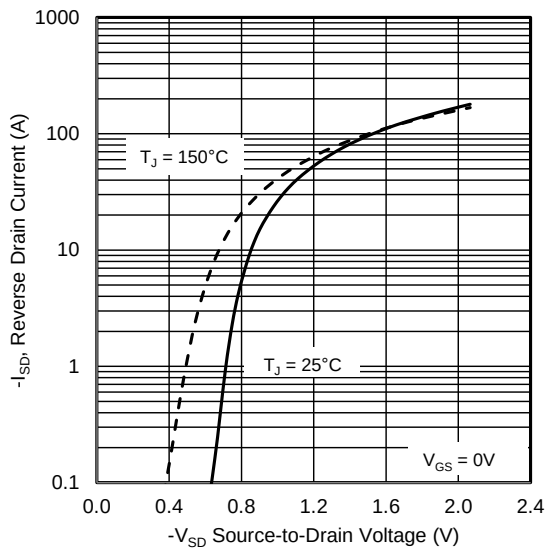


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

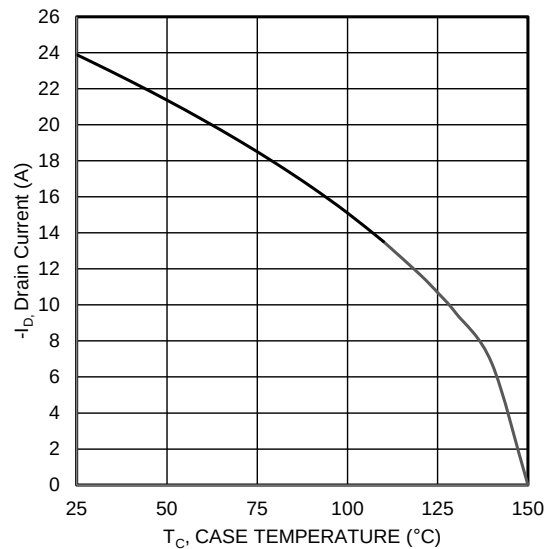


Figure 13 Maximum Drain Current Vs. Case Temperature

IRHNKC9A97130 (JANSR2N7660U3CE)

Radiation Hardened Power MOSFET (SMD-0.5e)

Electrical Characteristics Curves (Pre-irradiation)

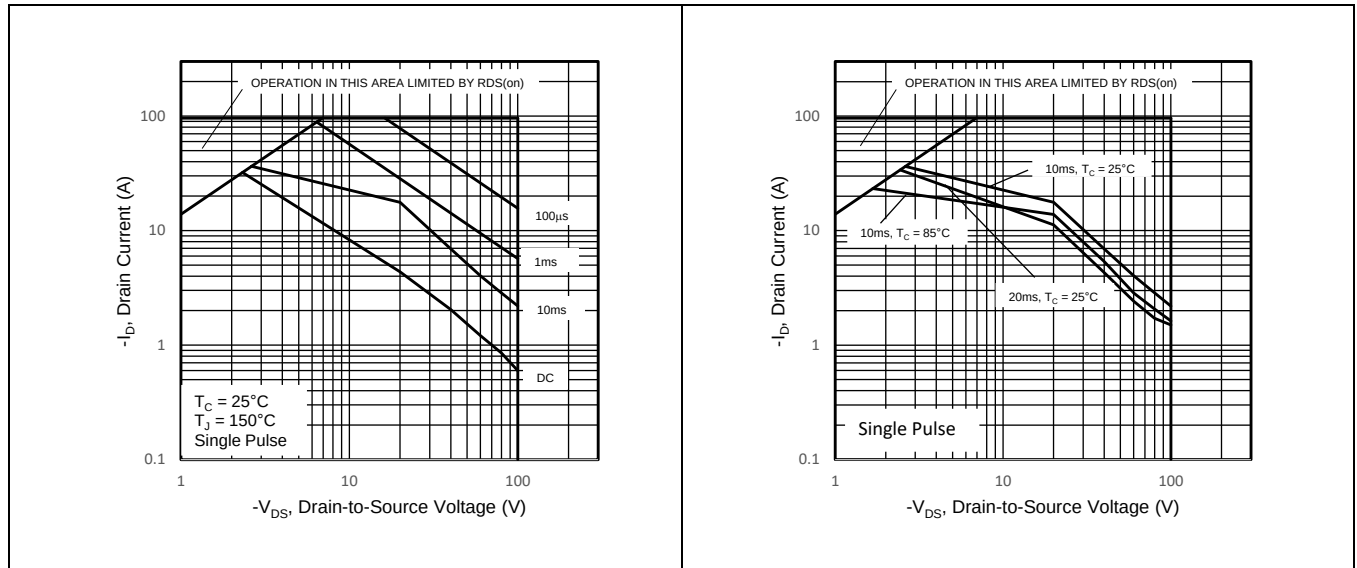


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Safe Operating Area

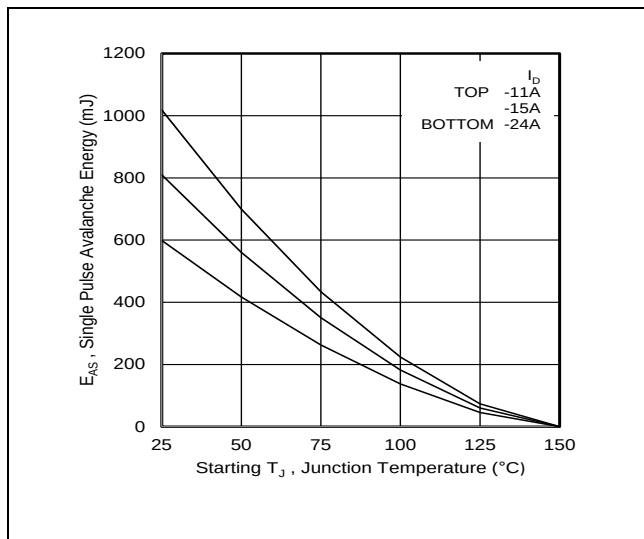


Figure 16 Maximum Avalanche Energy Vs. Junction Temperature

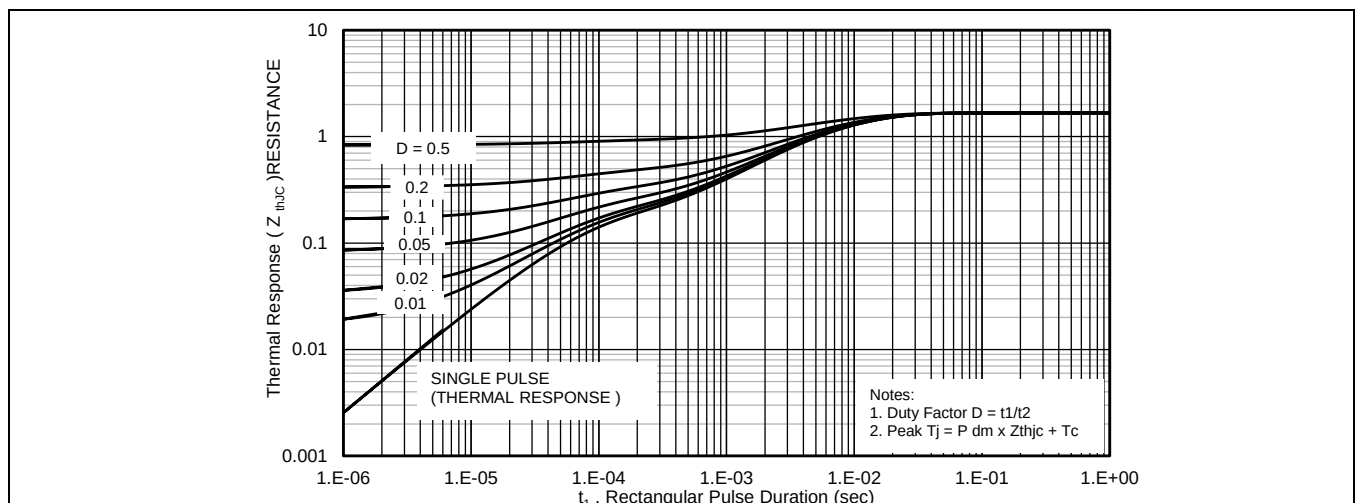


Figure 17 Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRHNKC9A97130 (JANSR2N7660U3CE)
Radiation Hardened Power MOSFET (SMD-0.5e)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

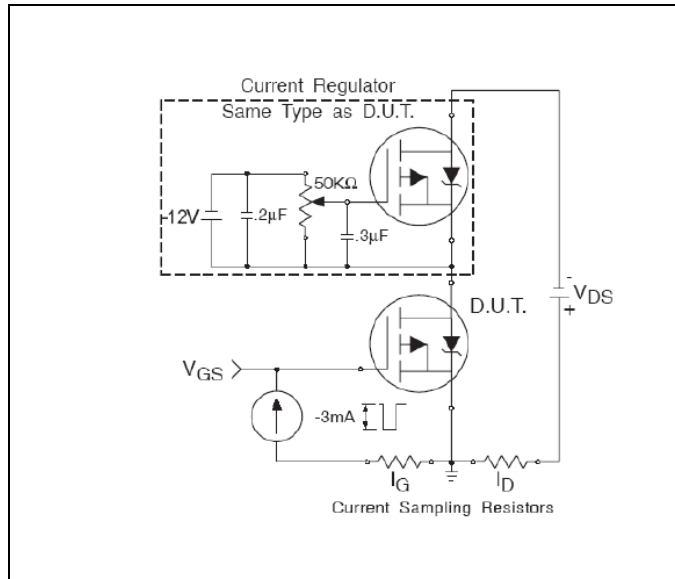


Figure 18 Gate Charge Test Circuit

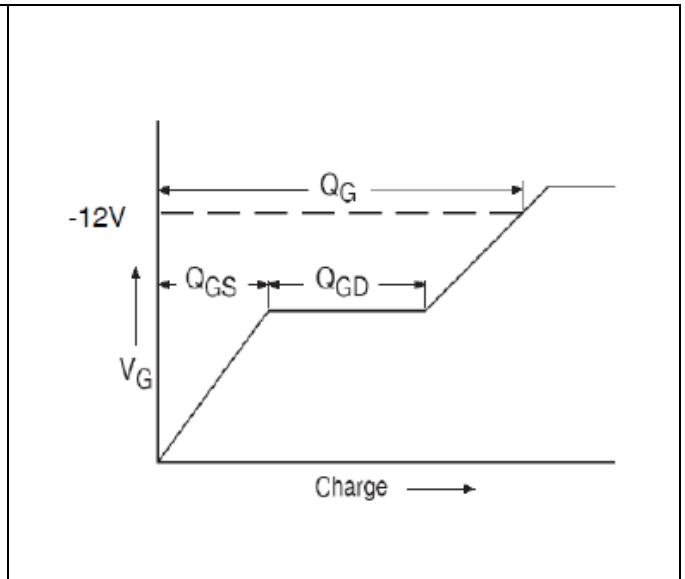


Figure 19 Gate Charge Waveform

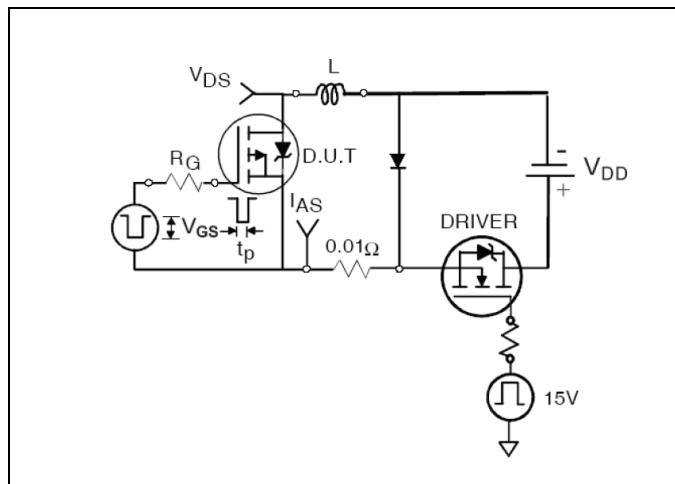


Figure 20 Unclamped Inductive Test Circuit

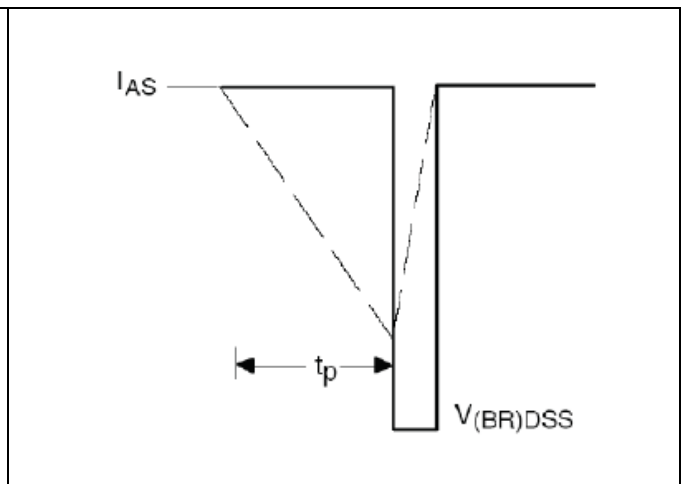


Figure 21 Unclamped Inductive Waveform

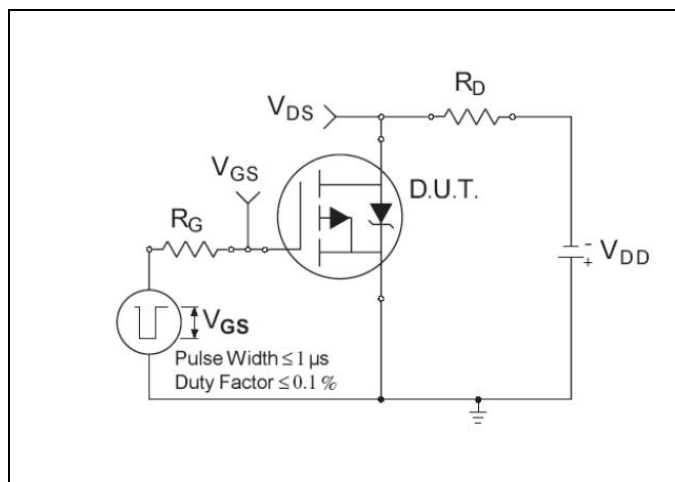


Figure 22 Switching Time Test Circuit

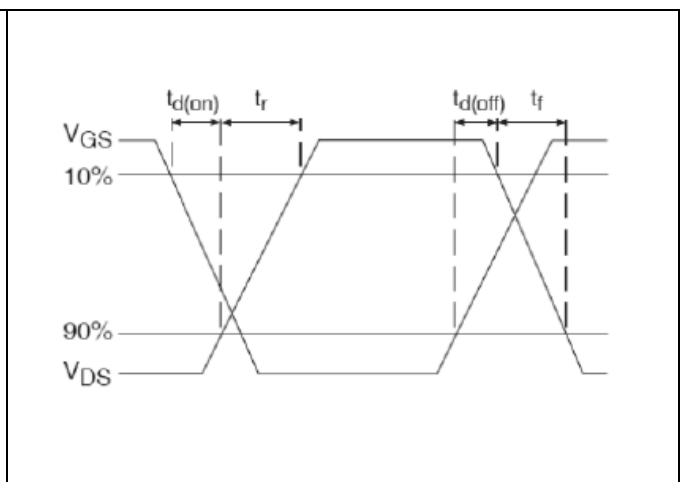
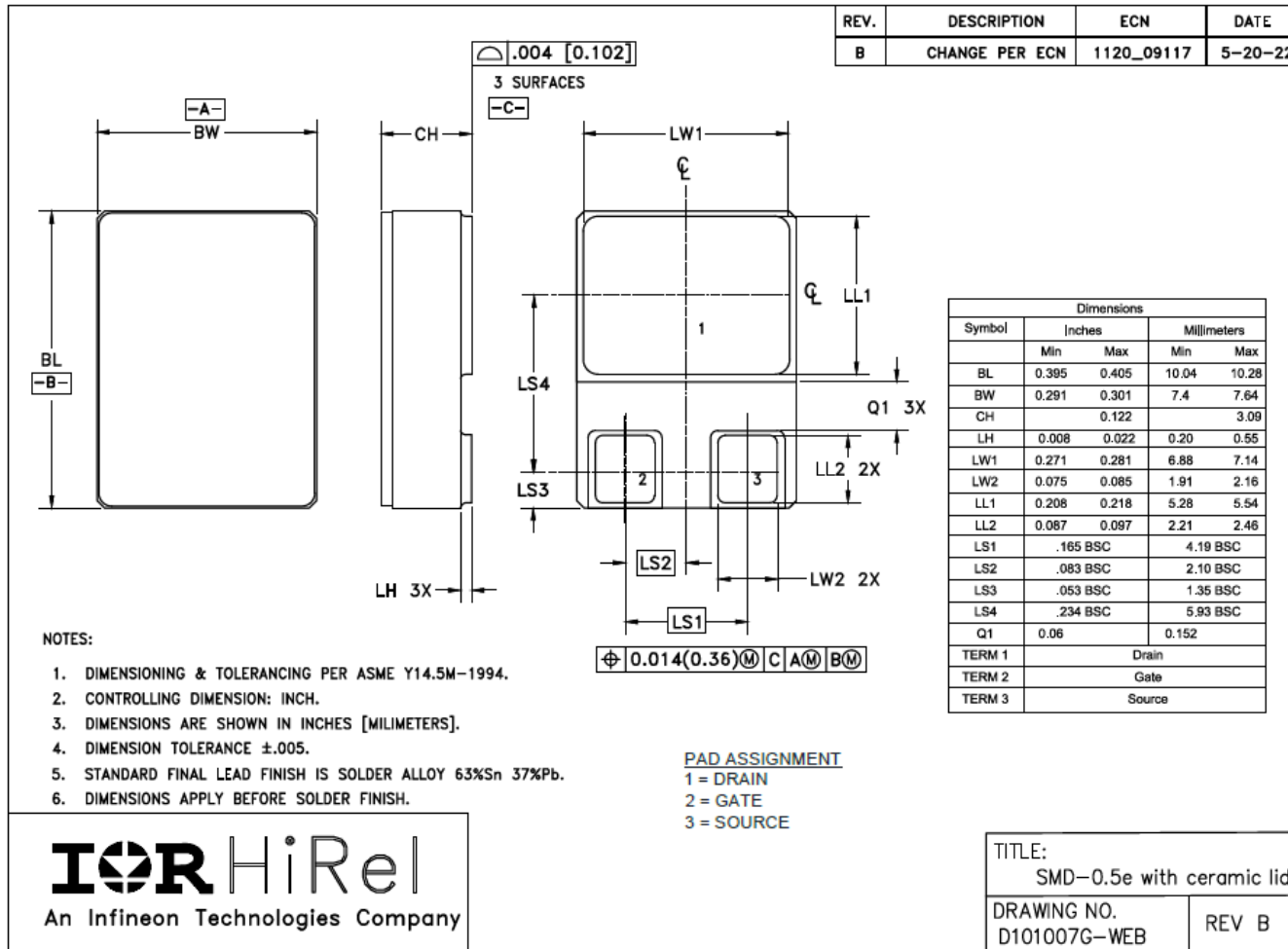


Figure 23 Switching Time Waveforms

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [SMD-0.5e \(Ceramic Lid\)](#)



IRHNKC9A97130 (JANSR2N7660U3CE)
Radiation Hardened Power MOSFET (SMD-0.5e)

Revision history

Revision history

Document version	Date of release	Description of changes
	10/24/2022	Preliminary datasheet with PPD number (PPD-97998)
Rev A	12/19/2022	Final datasheet with PD number (PD-97998A)
Rev B	07/26/2023	Updated based on ECN-1120_09644

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