IRHMS9A97064 (JANSR2N7664T1)

PD-97988A

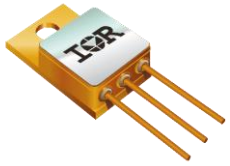
Radiation Hardened Power MOSFET
Thru-Hole (TO-254AA Low Ohmic)
-60V, -45A, P-channel, R9 Superjunction Technology

Features

- Single event effect (SEE) hardened (up to LET of 92.4 MeV·cm^2/mg)
- Low $R_{DS(on)}$
- Improved SOA for linear mode operation
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- Ceramic eyelets
- ESD rating: Class 3B per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}:** -60V
- **I_D :** -45A*
- **$R_{DS(on), max}$:** 12.5mΩ
- **$Q_{G, max}$:** 221nC
- **REF:** MIL-PRF-19500/791



TO-254AA Low Ohmic

Potential Applications

- DC-DC converter
- Motor drives
- Power distribution
- Latching current limiter

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. This family of p-channel MOSFETs are the first radiation hardened devices that are based on a superjunction technology. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 92.4 MeV·cm^2/mg. Their combination of low $R_{DS(on)}$ and improved SOA allows for better performance in applications such as Latching Current Limiters (LCL), Solid-State Power Controllers (SSPC) or DC-DC converters. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHMS9A97064	Low-Ohmic TO-254AA	COTS	100 krad (Si)
JANSR2N7664T1	Low-Ohmic TO-254AA	JANS	100 krad (Si)
IRHMS9A93064	Low-Ohmic TO-254AA	COTS	300 krad (Si)
JANSF2N7664T1	Low-Ohmic TO-254AA	JANS	300 krad (Si)

Table of contents

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = -12V, T_C = 25°C	Continuous Drain Current	-45*	A
I_{D2} @ V_{GS} = -12V, T_C = 100°C	Continuous Drain Current	-45*	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	-180	A
P_D @ T_C = 25°C	Maximum Power Dissipation	208	W
	Linear Derating Factor	1.7	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	9922	mJ
I_{AR}	Avalanche Current [1]	-45	A
E_{AR}	Repetitive Avalanche Energy [1]	20.8	mJ
dv/dt	Peak Diode Reverse Recovery [3]	6.7	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	°C
	Weight	9.3 (Typical)	g

*Current is limited by package

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] V_{DD} = -60V, starting T_J = 25°C, L = 9.8mH, Peak I_L = -45A, V_{GS} = -20V
[3] $I_{SD} \leq$ -45A, di/dt $\leq$ -800A/µs, $V_{DD} \leq$ -60V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.07	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	12.5	mΩ	V_{GS} = -12V, I_{D2} =- 45A [1]
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} \geq V_{GS}$, I_D = -5mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	5.9	—	mV/°C	
Gfs	Forward Transconductance	50	—	—	S	V_{DS} = -15V, I_{D2} = -45A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-10	µA	V_{DS} = -48V, V_{GS} = 0V
		—	—	-25		V_{DS} = -48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	221	nC	I_{D1} = -45A V_{DS} = -30V V_{GS} = -12V
Q_{GS}	Gate-to-Source Charge	—	—	53		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	54		
$t_{d(on)}$	Turn-On Delay Time	—	—	33	ns	I_{D1} = -45A ** V_{DD} = -30V R_G = 2.4Ω V_{GS} = -12V
t_r	Rise Time	—	—	116		
$t_{d(off)}$	Turn-Off Delay Time	—	—	264		
t_f	Fall Time	—	—	159		
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25in from package) to Source lead (6mm / 0.25in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	11495	—	pF	V_{GS} = 0V V_{DS} = -25V f = 100KHz
C_{oss}	Output Capacitance	—	3450	—		
C_{rss}	Reverse Transfer Capacitance	—	180	—		
R_G	Gate Resistance	—	3.4	—	Ω	f = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-45	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	-180	A	
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	T_J = 25°C, I_S =- 45A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	100	125	ns	T_J = 25°C, I_F = -45A, V_{DD} ≤ -25V di/dt = -100A/µs
Q_{rr}	Reverse Recovery Charge	—	355	—	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.6	°C/W
$R_{\theta CS}$	Junction-to-Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	48	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300 krad (Si)[5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	V	$V_{DS} \geq V_{GS}$, I_D = -5.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	100		V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	µA	V_{DS} = -48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [2]	—	11.5	mΩ	V_{GS} = -12V, I_{D2} = -45A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (Low-Ohmic TO-254AA) [2]	—	12.5	mΩ	V_{GS} = -12V, I_{D2} =- 45A
V_{SD}	Diode Forward Voltage	—	-1.3	V	V_{GS} = 0V, I_F = -45A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = -12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = -48V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[5] Part numbers IRHMS9A97064 (JANSR2N7664T1) and IRHMS9A93064 (JANSF2N7664T1)

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 **Typical Single Event Effects Safe Operating Area**

LET ($MeV·cm^2/mg$)	Energy (MeV)	Range (µm)	V_{DS} (V)			
			V_{GS} = 0V	V_{GS} = 1V	V_{GS} = 5V	V_{GS} = 10V
39.7 ± 5%	365 ± 7.5%	43 .2 ± 7.5%	-60	-60	-60	-60
68 ± 5%	665 ± 7.5%	51.9 ± 7.5%	-60	-60	-60	-60
92.4 ± 5%	1202 ± 7.5%	69.6 ± 7.5%	-60	-60	—	—

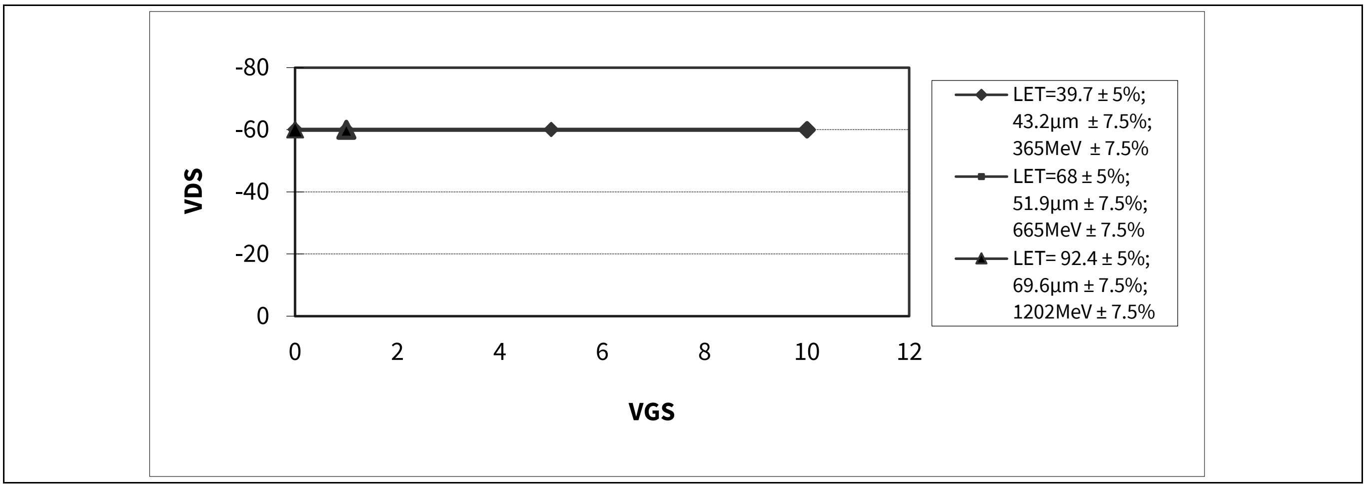


Figure 1 **Typical Single Event Effect, Safe Operating Area**

3 Electrical Characteristics Curves (Pre-irradiation)

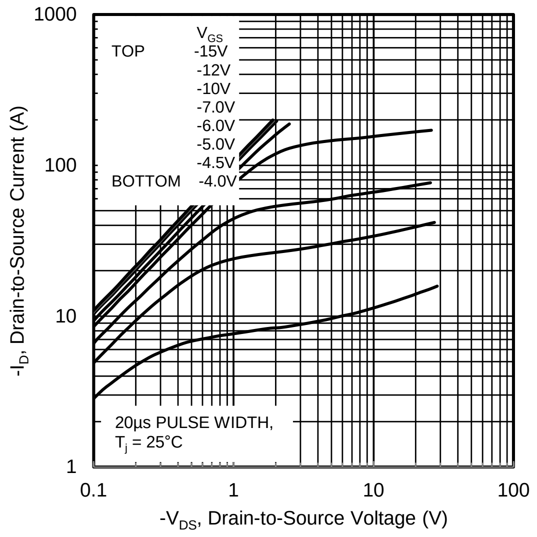


Figure 2 **Typical Output Characteristics**

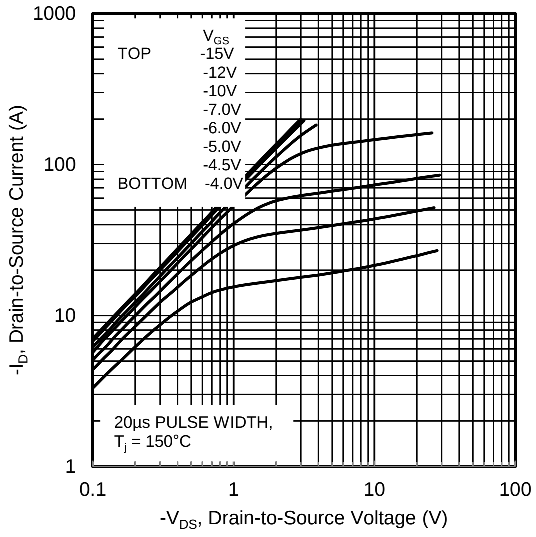


Figure 3 **Typical Output Characteristics**

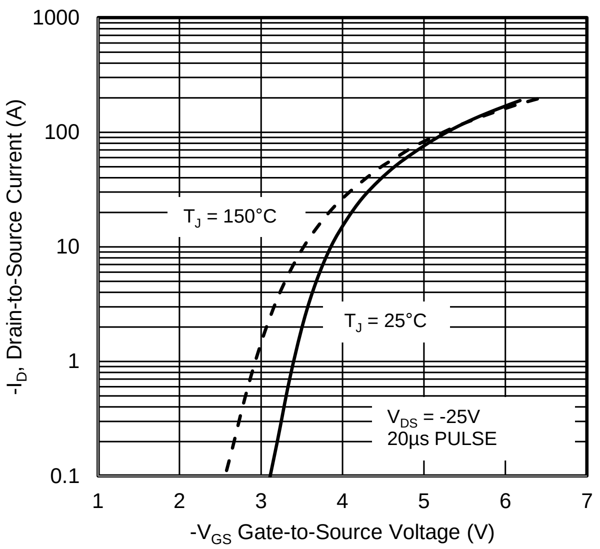


Figure 4 **Typical Transfer Characteristics**

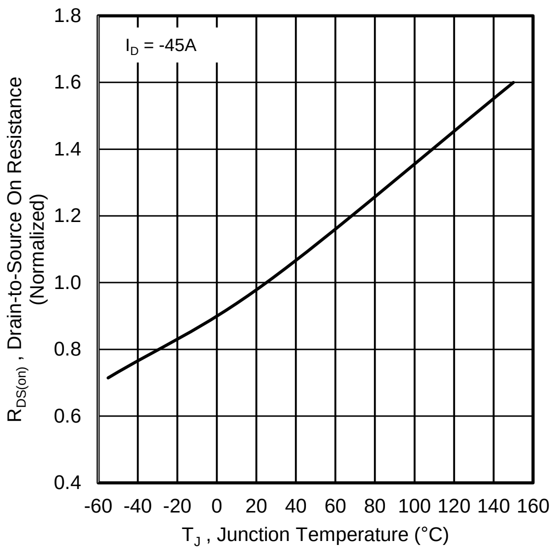


Figure 5 **Normalized On-Resistance Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

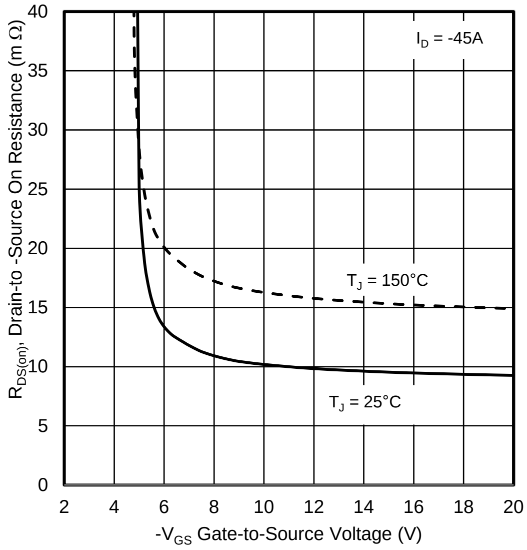


Figure 6 **Typical On-Resistance Vs Gate Voltage**

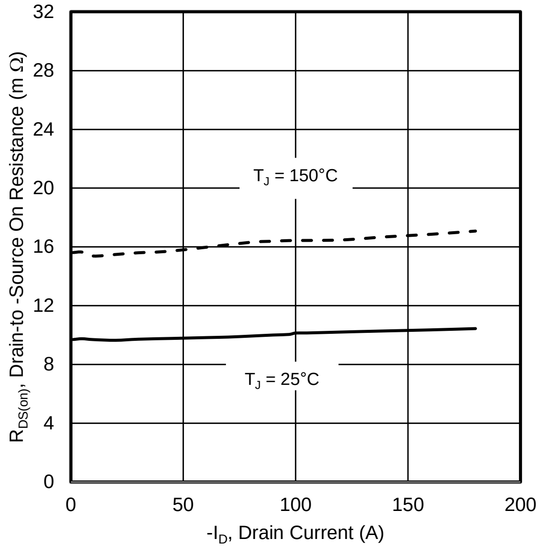


Figure 7 **Typical On-Resistance Vs Drain Current**

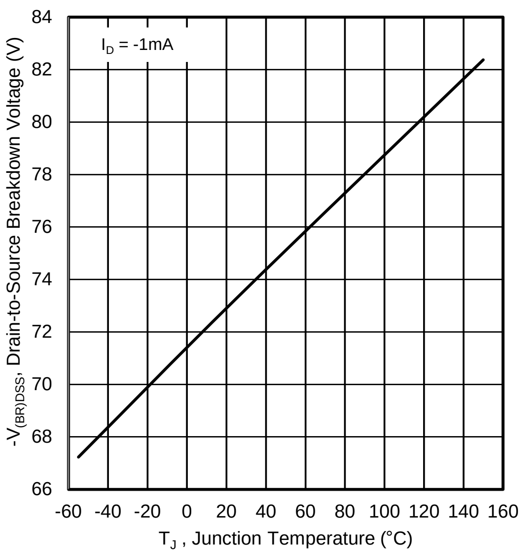


Figure 8 **Typical Drain-to-Source Breakdown Voltage Vs. Temperature**

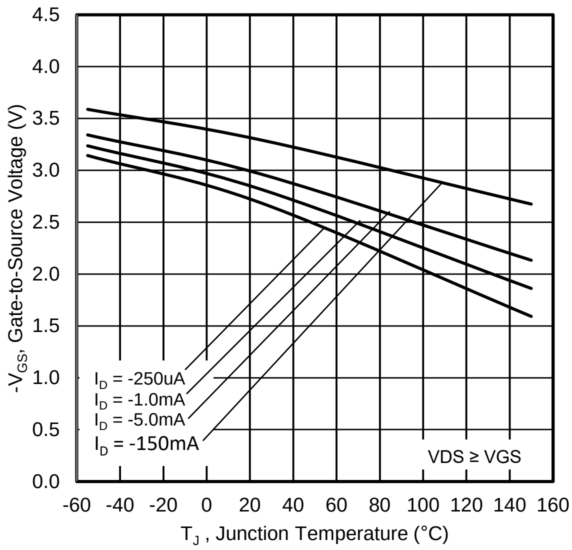


Figure 9 **Typical Gate-to-Source Voltage Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

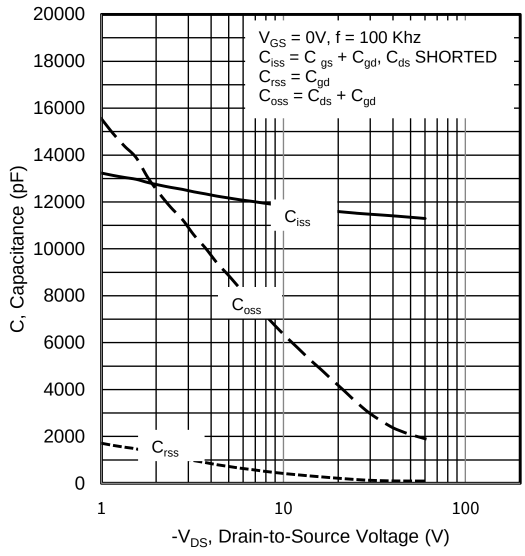


Figure 10 **Typical Capacitance Vs. Drain-to-Source Voltage**

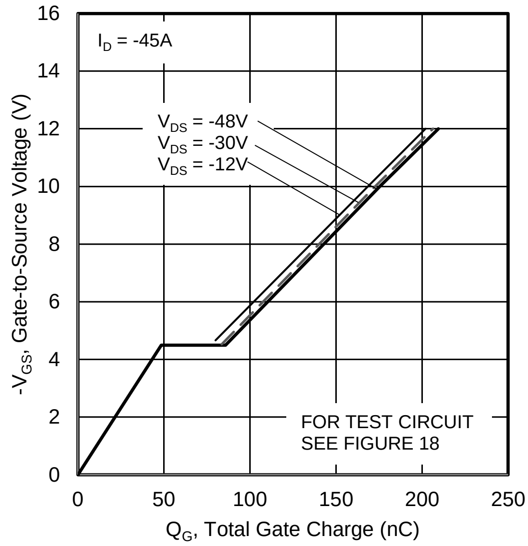


Figure 11 **Gate-to-Source Voltage Vs. Typical Gate Charge**

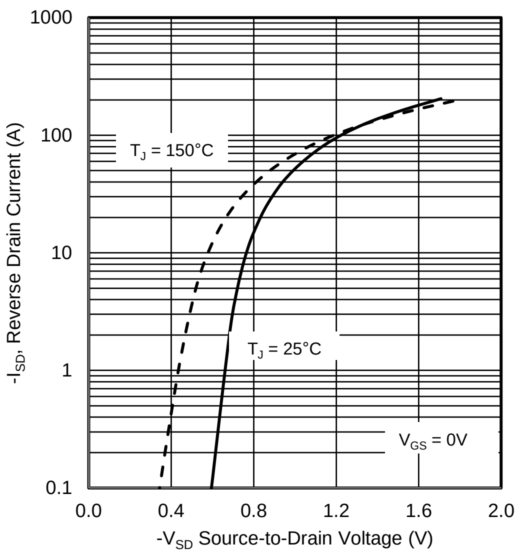


Figure 12 **Typical Source-Drain Current Vs. Diode Forward Voltage**

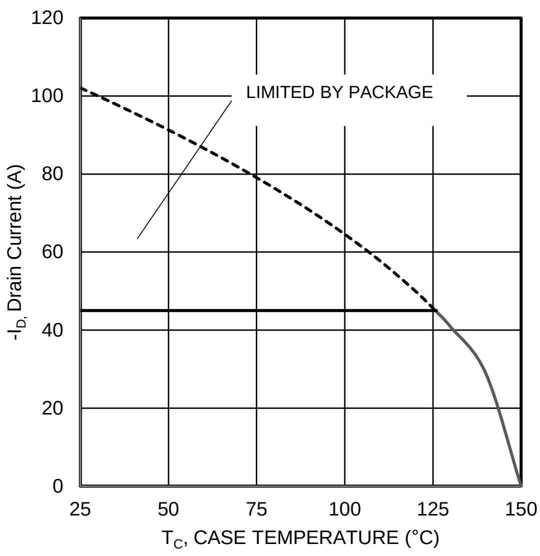


Figure 13 **Maximum Drain Current Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

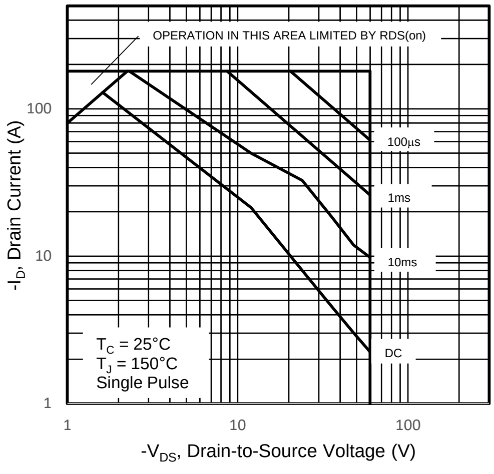


Figure 14 Maximum Safe Operating Area

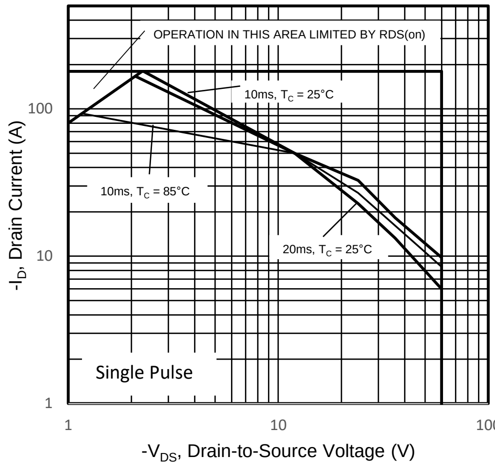


Figure 15 Maximum Safe Operating Area

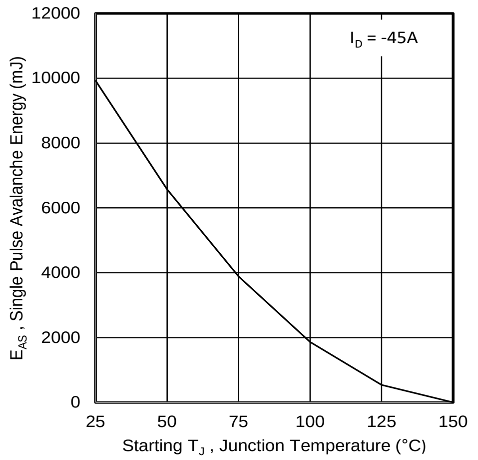


Figure 16 Maximum Avalanche Energy Vs. Junction Temperature

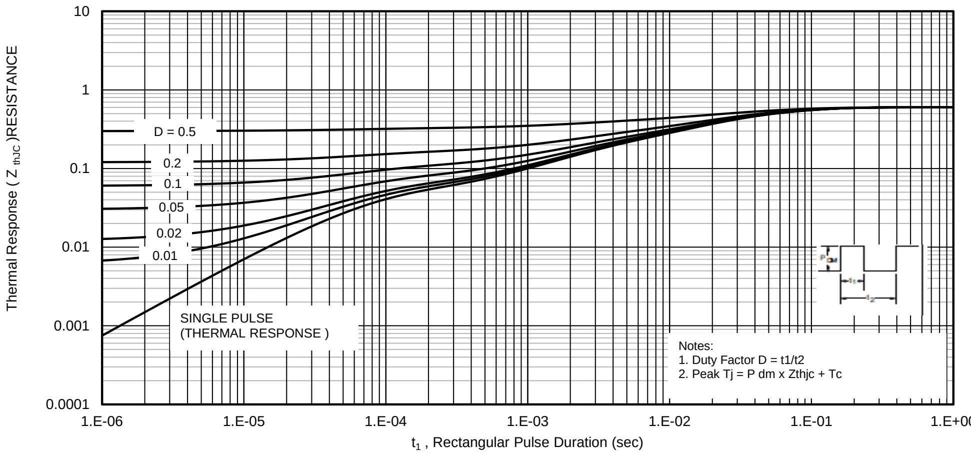


Figure 17 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

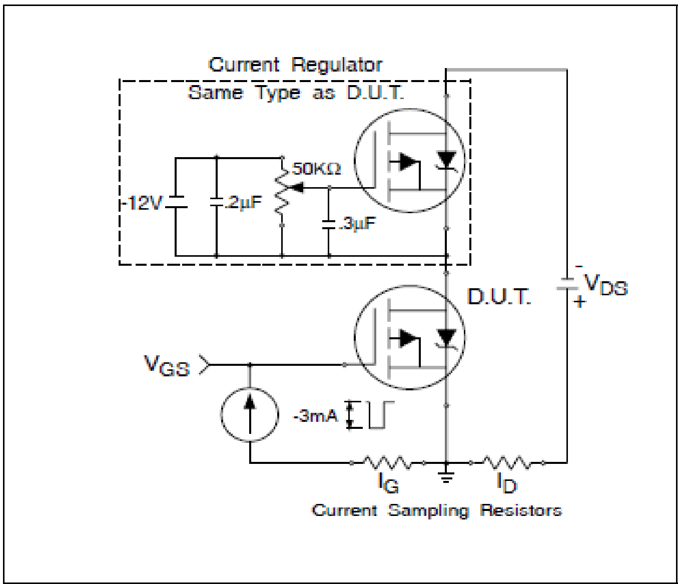


Figure 18 Gate Charge Test Circuit

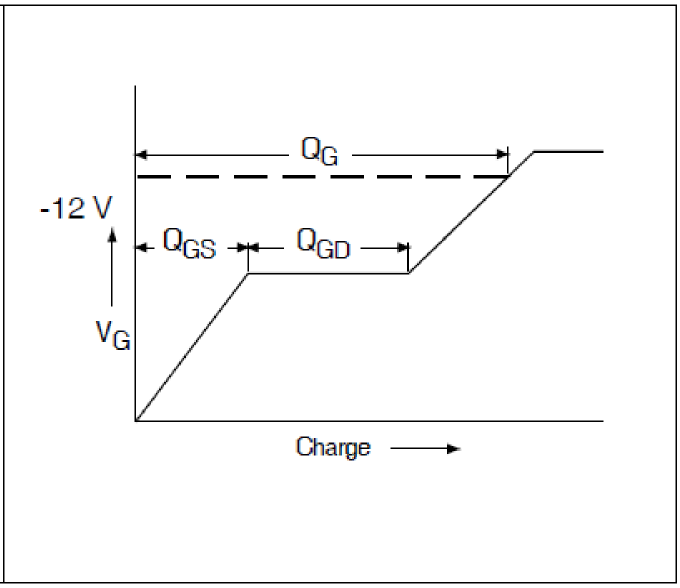


Figure 19 Gate Charge Waveform

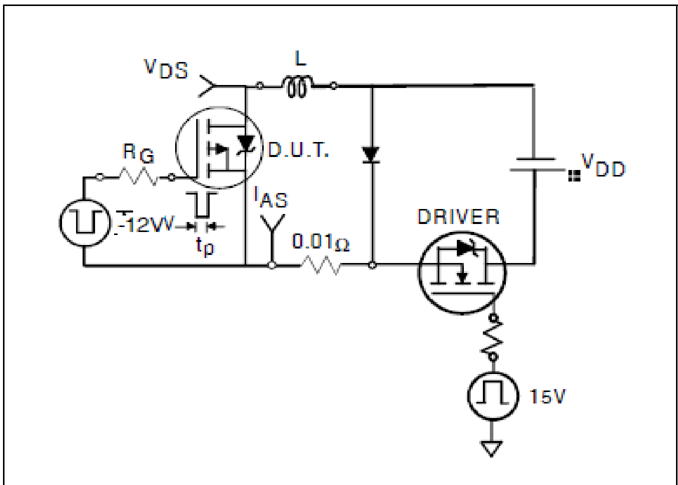


Figure 20 Unclamped Inductive Test Circuit

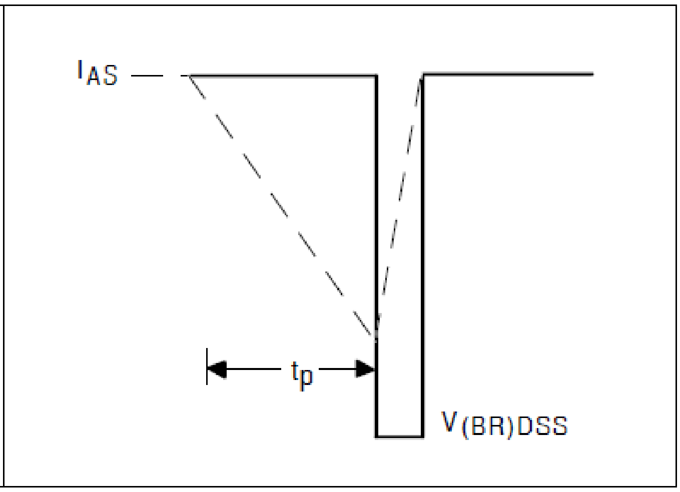


Figure 21 Unclamped Inductive Waveform

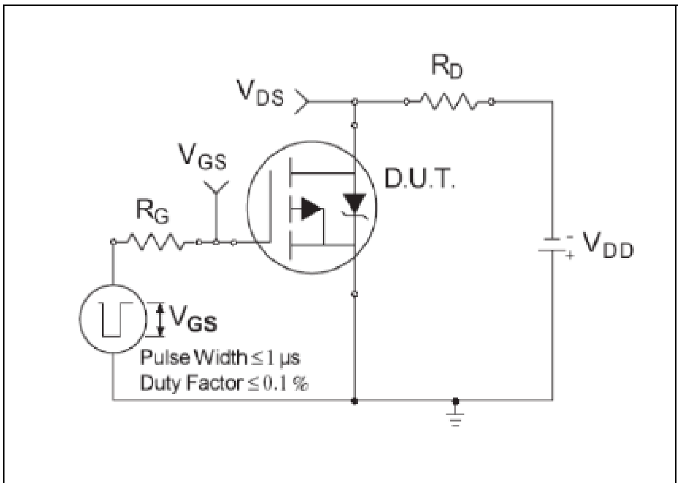


Figure 22 Switching Time Test Circuit

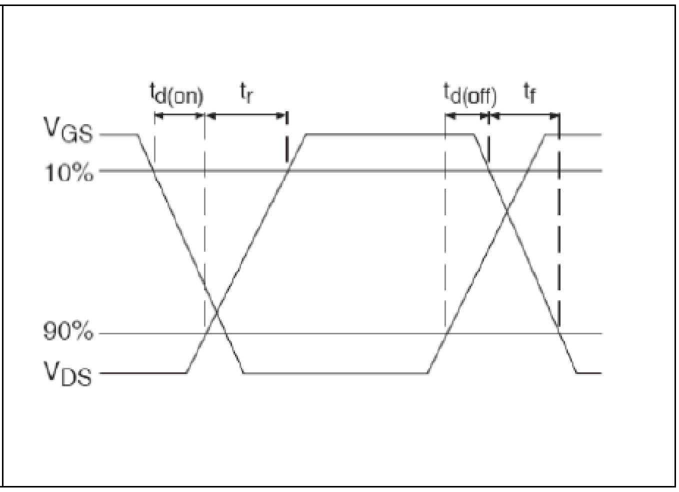
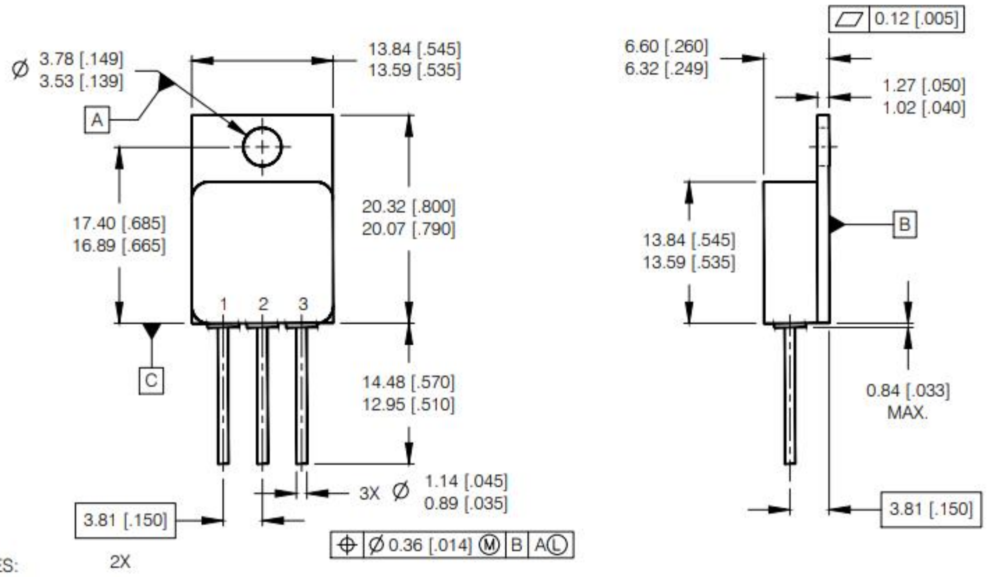


Figure 23 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: Low-Ohmic TO-254AA

REV.	DESCRIPTION	ECN	DATE
A	INITIAL RELEASE	1120_ER6904	4–3–20



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.
5. FINAL LEAD FINISH IS SOLDER ALLOY 63%Sn 37%Pb.
6. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

PIN ASSIGNMENTS
1 = DRAIN
2 = SOURCE
3 = GATE

IOR HiRel
An Infineon Technologies Company

TITLE: TO–254AA PACKAGE OUTLINE (STD & LOW OHMIC)
DRAWING NO. D100720G–WEB
REV A

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

Revision history

Document version	Date of release	Description of changes
	10/13/2023	Preliminary datasheet with PPD number (PPD-97983)
Rev A	11/20/2023	Final datasheet with PD number

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-11-20

Published by

International Rectifier HiRel Products, Inc.

An Infineon Technologies company

El Segundo, California 90245 USA

© 2025 Infineon Technologies AG.
All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest International Rectifier HiRel Products, Inc., an Infineon Technologies company, office.

International Rectifier HiRel Components may only be used in life-support devices or systems with the expressed written approval of International Rectifier HiRel Products, Inc., an Infineon Technologies company, if failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety and effectiveness of that device or system.

Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.