



An Infineon Technologies Company

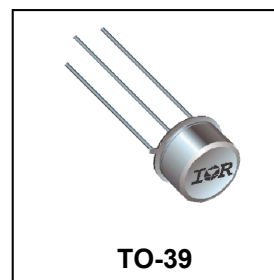
**IRFF9130**  
**JANTX2N6849**  
**JANTXV2N6849**  
**JANS2N6849**

**REPETITIVE AVALANCHE AND dv/dt RATED  
 HEXFET® TRANSISTORS  
 THRU-HOLE TO-205AF (TO-39)**

**100V, P-CHANNEL**  
 REF: MIL-PRF-19500/564

**Product Summary**

Part Number	BVDSS	RDS(on)	I <sub>D</sub>
IRFF9130	-100V	0.30Ω	-6.5A

**Description**

The HEXFET® technology is the key to International Rectifier's HiRel advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on state resistance combined with high trans conductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

**Absolute Maximum Ratings**

Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = -10V, T <sub>C</sub> = 25°C	Continuous Drain Current	-6.5	A
I <sub>D2</sub> @ V <sub>GS</sub> = -10V, T <sub>C</sub> = 100°C	Continuous Drain Current	-4.1	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	-25	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	25	W
	Linear Derating Factor	0.20	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	92	mJ
I <sub>AR</sub>	Avalanche Current ①	-6.5	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	0.98 (Typical)	

For Footnotes, refer to the page 2.

**Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.10	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.30	Ω	V <sub>GS</sub> = -10V, I <sub>D2</sub> = -4.1A ④
		—	—	0.320		V <sub>GS</sub> = -10V, I <sub>D1</sub> = -6.5A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	-25	μA	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V
		—	—	-250		V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V <sub>GS</sub> = 20V
Q <sub>G</sub>	Total Gate Charge	14.7	—	34.8	nC	I <sub>D1</sub> = -6.5A
Q <sub>GS</sub>	Gate-to-Source Charge	1.0	—	6.8		V <sub>DS</sub> = -50V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	2.0	—	23.1		V <sub>GS</sub> = -10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	60	ns	V <sub>DD</sub> = -40V
t <sub>r</sub>	Rise Time	—	—	140		I <sub>D1</sub> = -6.5A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	140		R <sub>G</sub> = 7.5Ω
t <sub>f</sub>	Fall Time	—	—	140		V <sub>GS</sub> = -10V
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
C <sub>iSS</sub>	Input Capacitance	—	800	—	pF	V <sub>GS</sub> = 0V
C <sub>oSS</sub>	Output Capacitance	—	350	—		V <sub>DS</sub> = -25V
C <sub>rSS</sub>	Reverse Transfer Capacitance	—	125	—		f = 1.0MHz

**Source-Drain Diode Ratings and Characteristics**

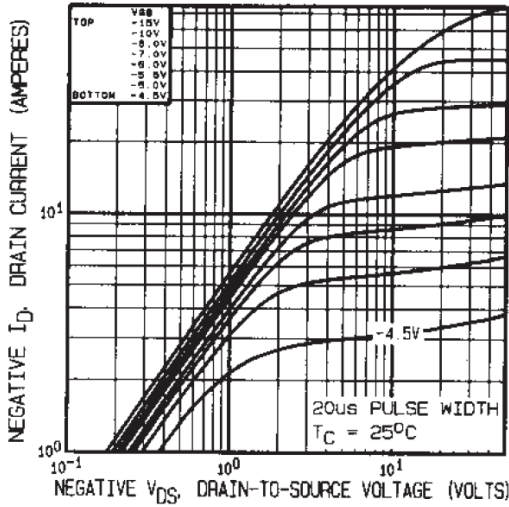
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-6.5	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-25		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-4.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -6.5A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	250	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -6.5A, V <sub>DD</sub> ≤ -50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	3.0	μC	di/dt = -100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Thermal Resistance**

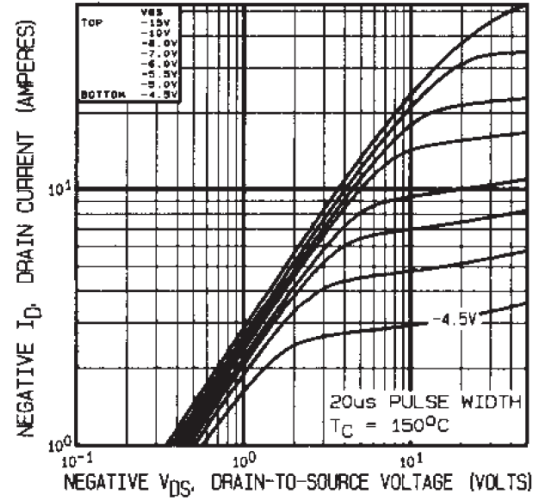
Symbol	Parameter	Min.	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	—	5.0	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (Typical Socket Mount)	—	—	175	

**Footnotes:**

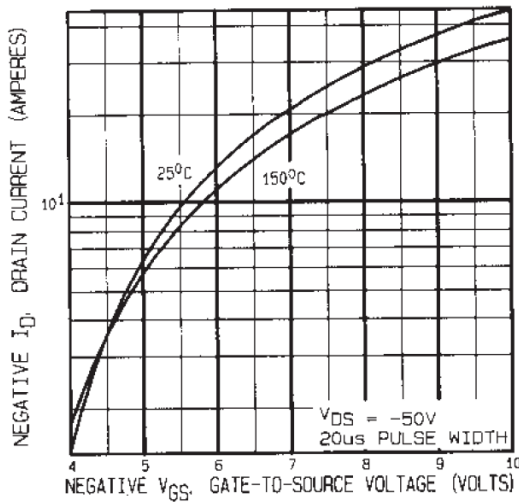
- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V<sub>DD</sub> = -25V, starting T<sub>J</sub> = 25°C, Peak I<sub>L</sub> = -6.5A, V<sub>GS</sub> = -10V
- ③ I<sub>SD</sub> ≤ -6.5A, di/dt ≤ -140A/μs, V<sub>DD</sub> ≤ -100V, T<sub>J</sub> ≤ 150°C, Suggested R<sub>G</sub> = 7.5 Ω
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%



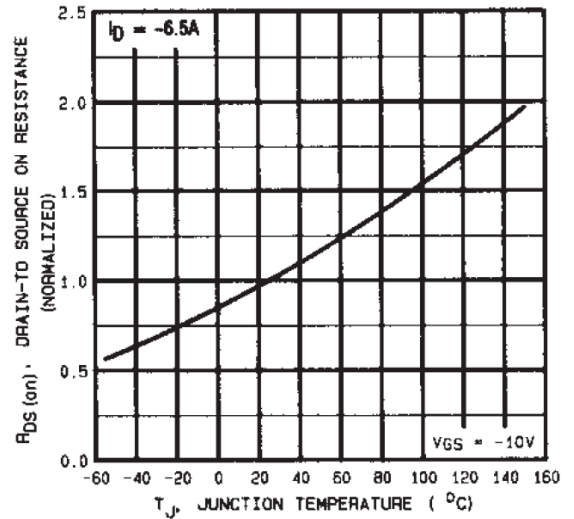
**Fig 1.** Typical Output Characteristics



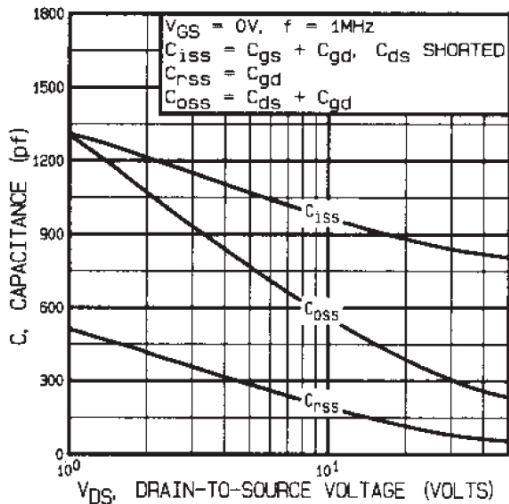
**Fig 2.** Typical Output Characteristics



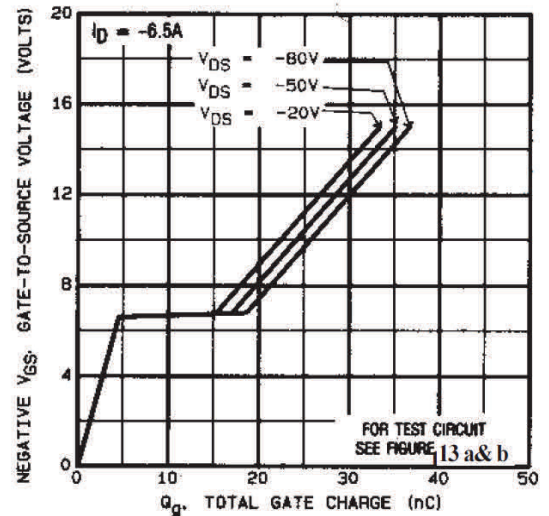
**Fig 3.** Typical Transfer Characteristics



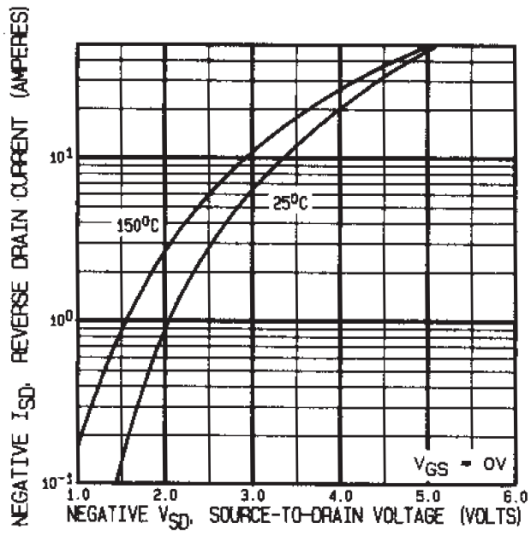
**Fig 4.** Normalized On-Resistance Vs. Temperature



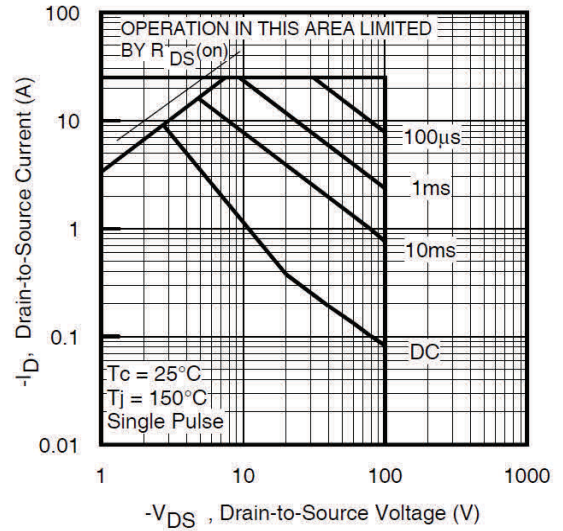
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



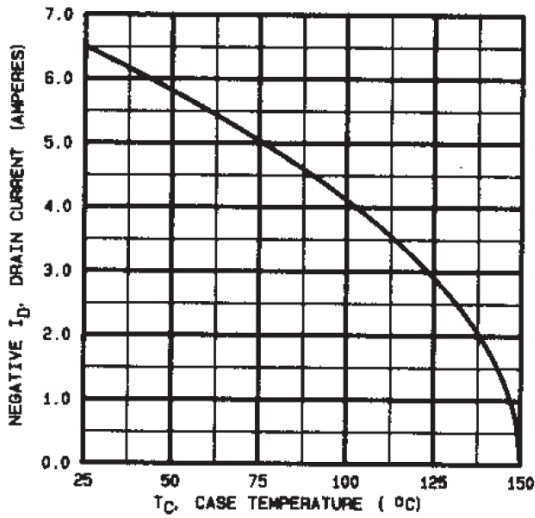
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



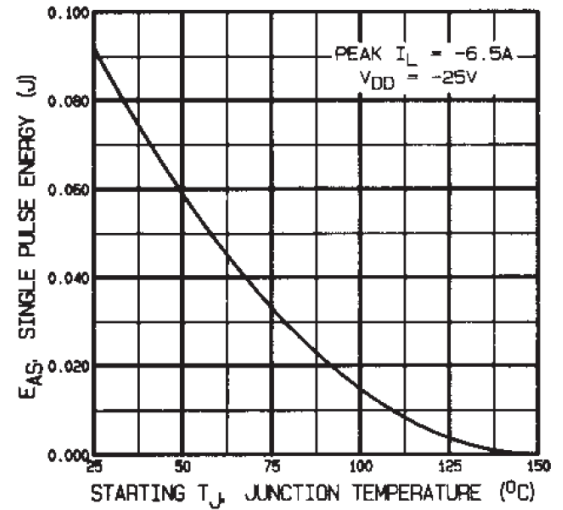
**Fig 7. Typical Source-Drain Diode Forward Voltage**



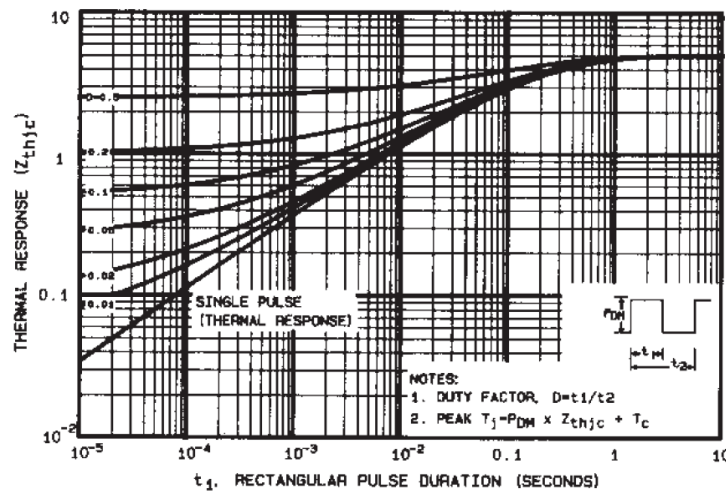
**Fig 8. Maximum Safe Operating Area**



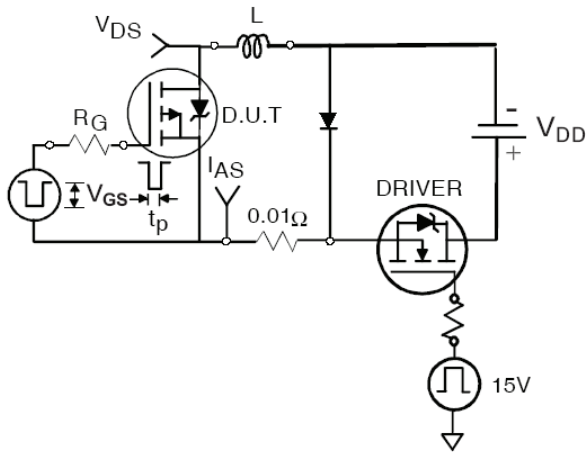
**Fig 9. Maximum Drain Current Vs. Case Temperature**



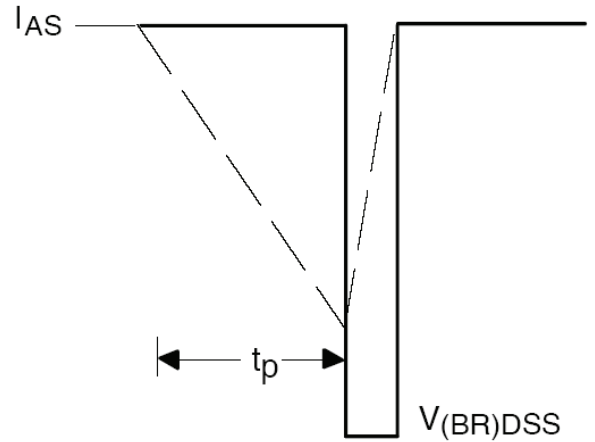
**Fig 10. Maximum Avalanche Energy Vs. Drain Current**



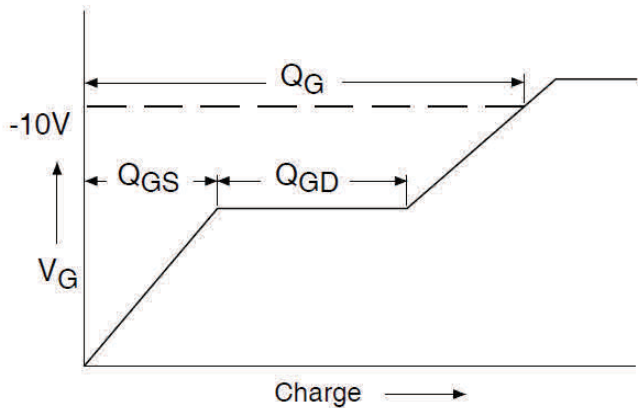
**Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case**



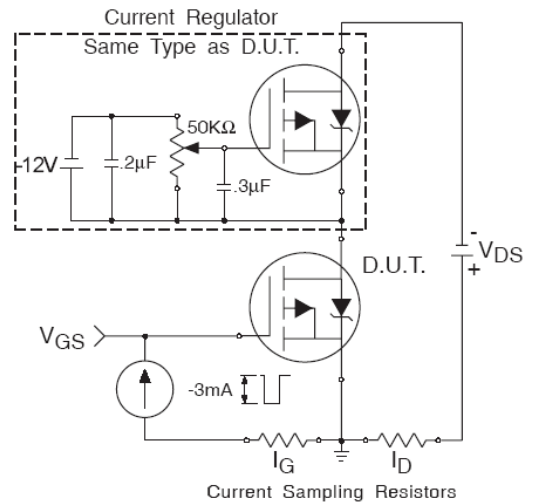
**Fig 12a.** Unclamped Inductive Test Circuit



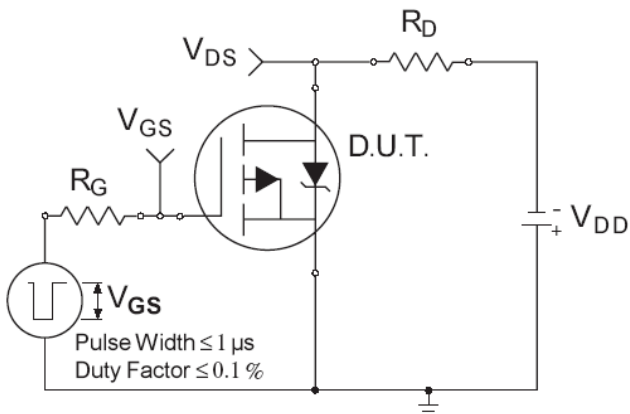
**Fig 12b.** Unclamped Inductive Waveforms



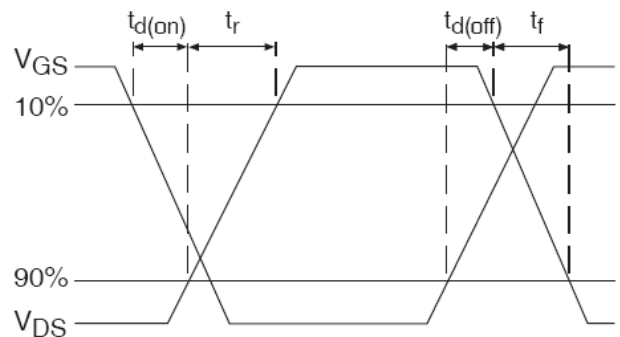
**Fig 13a.** Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

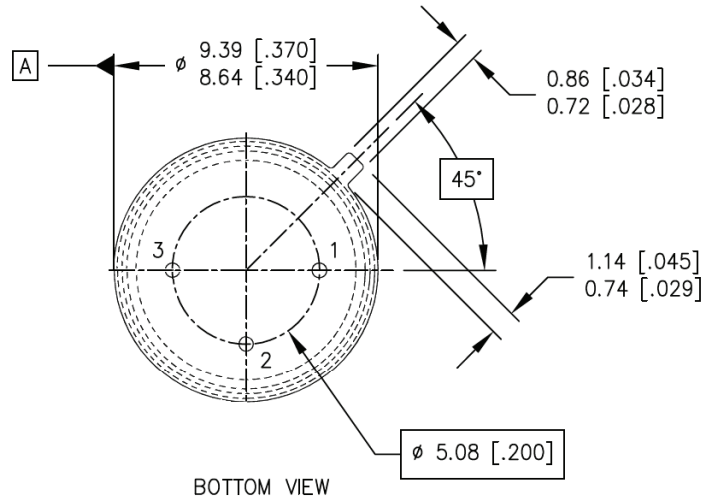
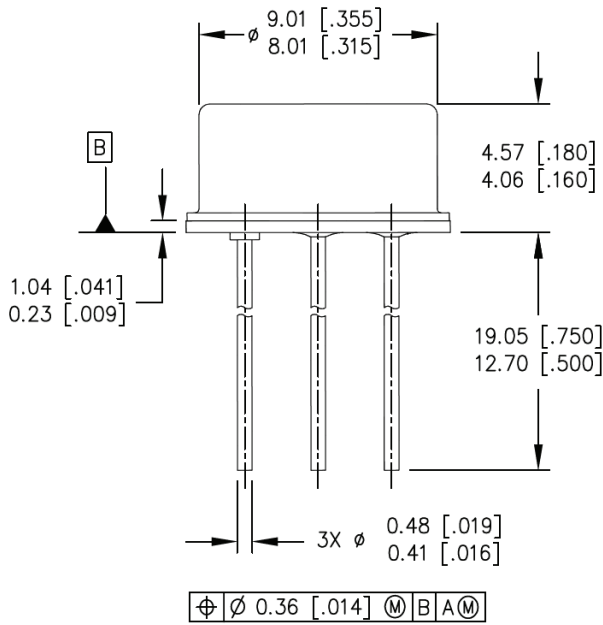


**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms

**Case Outline and Dimensions - TO-205AF (TO-39)**



NOTES:

SIDE VIEW

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN (CONNECTED TO THE CASE)

### **IMPORTANT NOTICE**

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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