# IRHNS67264 (JANSR2N7585U2A)

PD-97882C

## Radiation Hardened Power MOSFET
## Surface Mount (SupIR-SMD™)
## 250V, 50A, N-channel, R6 Technology

### Features

- Single event effect (SEE) hardened (up to LET of 85 MeV·cm²/mg)
- Low $R_{DS(on)}$
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Light weight
- Surface mount
- ESD rating: Class 3A per MIL-STD-750, Method 1020

### Product Summary

- **Part number:** IRHNS67264 (JANSR2N7585U2A), IRHNS63264 (JANSR2N7585U2A)
- **REF:** MIL-PRF-19500/760
- **Radiation level:** 100 krad (Si), 300 krad (Si)
- **$R_{DS(on),\,max}$:** 40mΩ

**SupIR-SMD™**

### Potential Applications

- DC-DC converter
- Motor drives

### Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications

### Description

IR HiRel R6 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 85 MeV·cm²/mg. Their combination of low $R_{DS(on)}$ and fast switching times will allow for better performance in applications such as DC-DC converters or motor drives. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

### Ordering Information

**Table 1 Ordering options**

| Part number | Package | Screening Level | TID Level |
|---|---|---|---|
| IRHNS67264 | SupIR-SMD™ | COTS | 100 krad (Si) |
| IRHNS67264SCS | SupIR-SMD™ | S-Level | 100 krad (Si) |
| JANSR2N7585U2A | SupIR-SMD™ | JANS | 100 krad (Si) |
| IRHNS63264 | SupIR-SMD™ | COTS | 300 krad (Si) |
| JANSF2N7585U2A | SupIR-SMD™ | JANS | 300 krad (Si) |

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# 1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings (Pre-Irradiation)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{D1}$ @ $V_{GS}$ = 12V, $T_C$ = 25°C | Continuous Drain Current | 50 | A |
| $I_{D2}$ @ $V_{GS}$ = 12V, $T_C$ = 100°C | Continuous Drain Current | 31.5 | A |
| $I_{DM}$ @ $T_C$ = 25°C | Pulsed Drain Current [1] | 200 | A |
| $P_D$ @ $T_C$ = 25°C | Maximum Power Dissipation | 250 | W |
| | Linear Derating Factor | 2.0 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy [2] | 240 | mJ |
| $I_{AR}$ | Avalanche Current [1] | 50 | A |
| $E_{AR}$ | Repetitive Avalanche Energy [1] | 25 | mJ |
| dv/dt | Peak Diode Reverse Recovery [3] | 5.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and Storage Temperature Range | -55 to +150 | °C |
| | Lead Temperature | 300 ( for 5s) | |
| | Weight | 3.3 (Typical) | g |

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] $V_{DD}$ = 50V, starting $T_J$ = 25°C, L = 0.19mH, Peak $I_L$ = 50A, $V_{GS}$ = 12V

[3] $I_{SD} \leq$ 50A, di/dt ≤ 900A/µs, $V_{DD} \leq$ 250V, $T_J \leq$ 150°C

# 2 Device Characteristics

## 2.1 Electrical Characteristics (Pre-Irradiation)

**Table 3 Static and Dynamic Electrical Characteristics @ $T_j$ = 25°C (Unless Otherwise Specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 250 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.3 | — | V/°C | Reference to 25°C, $I_D$ = 1.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance | — | — | 40 | mΩ | $V_{GS}$ = 12V, $I_{D2}$ = 31.5A [1] |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 1mA |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Coefficient | — | -10.1 | — | mV/°C | |
| Gfs | Forward Transconductance | 37 | — | — | S | $V_{DS}$ = 15V, $I_{D2}$ = 31.5A [1] |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | — | 10 | µA | $V_{DS}$ = 200V, $V_{GS}$ = 0V |
| | | — | — | 25 | | $V_{DS}$ = 200V,$V_{GS}$ = 0V,$T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Leakage Reverse | — | — | -100 | | $V_{GS}$ = -20V |
| $Q_G$ | Total Gate Charge | — | — | 220 | nC | $I_{D1}$ = 50A<br>$V_{DS}$ = 125V<br>$V_{GS}$ = 12V |
| $Q_{GS}$ | Gate-to-Source Charge | — | — | 50 | | |
| $Q_{GD}$ | Gate-to-Drain (‘Miller’) Charge | — | — | 70 | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | — | 50 | ns | $I_{D1}$ = 50A **<br>$V_{DD}$ = 125V<br>$R_G$ = 2.35Ω<br>$V_{GS}$ = 12V |
| $t_r$ | Rise Time | — | — | 150 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | — | 100 | | |
| $t_f$ | Fall Time | — | — | 50 | | |
| $L_s$ +$L_D$ | Total Inductance | — | 12 | — | nH | Measured from center of Drain pad to center of Source pad |
| $C_{iss}$ | Input Capacitance | — | 6912 | — | pF | $V_{GS}$ = 0V<br>$V_{DS}$ = 25V<br>$f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 940 | — | | |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 10.8 | — | | |
| $R_G$ | Gate Resistance | — | 0.52 | — | Ω | $f$ = 1.0MHz, open drain |

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

## 2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

**Table 4 Source-Drain Diode Characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 50 | A | |
| $I_{SM}$ | Pulsed Source Current (Body Diode) [1] | — | — | 200 | A | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.2 | V | $T_J$ = 25°C, $I_S$ = 50A, $V_{GS}$ = 0V [2] |
| $t_{rr}$ | Reverse Recovery Time | — | — | 700 | ns | $T_J$ = 25°C, $I_F$ = 50A, $V_{DD}$ ≤ 25V di/dt = 100A/µs [2] |
| $Q_{rr}$ | Reverse Recovery Charge | — | — | 15 | µC | |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

## 2.3 Thermal Characteristics

**Table 5 Thermal Resistance**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | — | 0.5 | °C/W |
| $R_{\theta J\text{-}PCB}$ | Junction-to-PC Board (Soldered to 2” sq copper clad board) | — | 1.6 | — | |

## 2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

## 2.4.1 Electrical Characteristics — Post Total Dose Irradiation

**Table 6 Electrical Characteristics @ $T_J$ = 25°C, Post Total Dose Irradiation [3, 4]**

| Symbol | Parameter | Up to 300 krad (Si)[5] | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 250 | — | V | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.0mA |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Leakage Reverse | — | -100 | | $V_{GS}$ = -20V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | 10 | µA | $V_{DS}$ = 200V, $V_{GS}$ = 0V |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance (TO-3) [2] | — | 41 | mΩ | $V_{GS}$ = 12V, $I_{D2}$ = 31.5A |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance (SupIR-SMD™) [2] | — | 40 | mΩ | $V_{GS}$ = 12V, $I_{D2}$ = 31.5A |
| $V_{SD}$ | Diode Forward Voltage | — | 1.2 | V | $V_{GS}$ = 0V, $I_F$ = 50A |

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] Total Dose Irradiation with $V_{GS}$ Bias. $V_{GS}$ = 12V applied and $V_{DS}$ = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[4] Total Dose Irradiation with $V_{DS}$ Bias. $V_{DS}$ = 200V applied and $V_{GS}$ = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[5] Part numbers IRHNS67264 (JANSR2N7585U2A) and IRHNS63264 (JANSR2F7585U2A)

## 2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

**Table 7 Typical Single Event Effects Safe Operating Area**

| LET (MeV·cm²/mg) | Energy (MeV) | Range (µm) | $V_{DS}$ (V) | | | | |
|---|---|---|---|---|---|---|---|
| | | | $V_{GS}$ = 0V | $V_{GS}$ = -5V | $V_{GS}$ = -10V | $V_{GS}$ = -15V | $V_{GS}$ = -20V |
| 50 ± 5% | 821 ± 5% | 74.2 ± 5% | 250 | 250 | 250 | 250 | 40 |
| 59 ± 5% | 1040 ± 5% | 79.7 ± 5% | 225 | 225 | 225 | 50 | — |
| 85 ± 5% | 1908 ± 5% | 101.2 ± 5% | 75 | 75 | — | — | — |

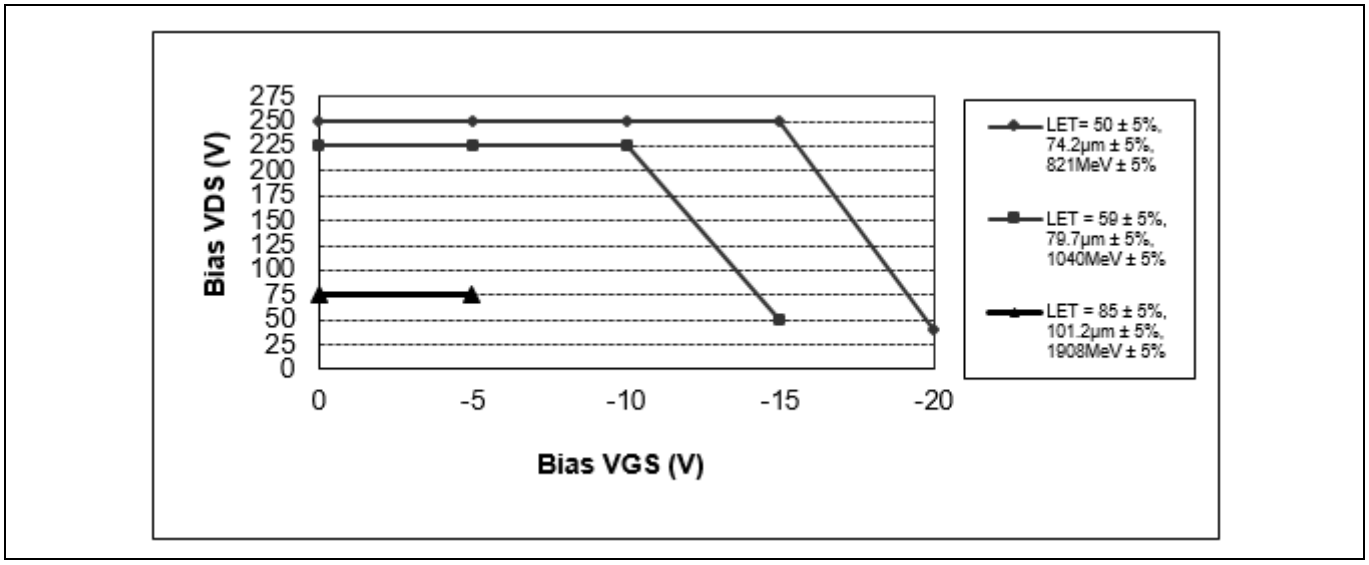



**Figure 1 Typical Single Event Effect, Safe Operating Area**

# 3 Electrical Characteristics Curves (Pre-irradiation)

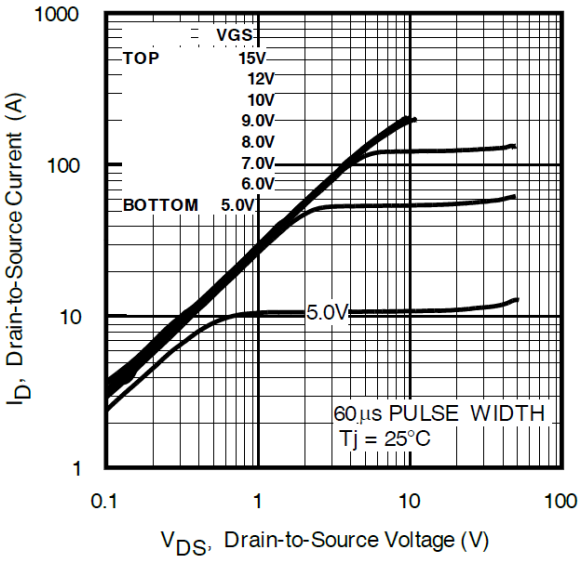



**Figure 2 Typical Output Characteristics**

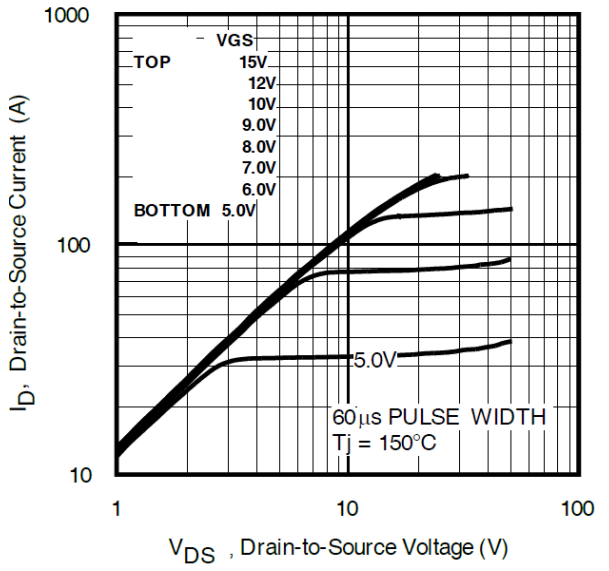



**Figure 3 Typical Output Characteristics**

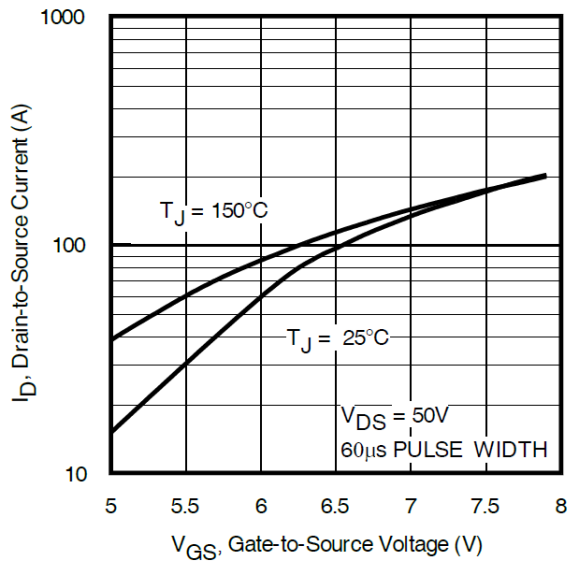



**Figure 4 Typical Transfer Characteristics**

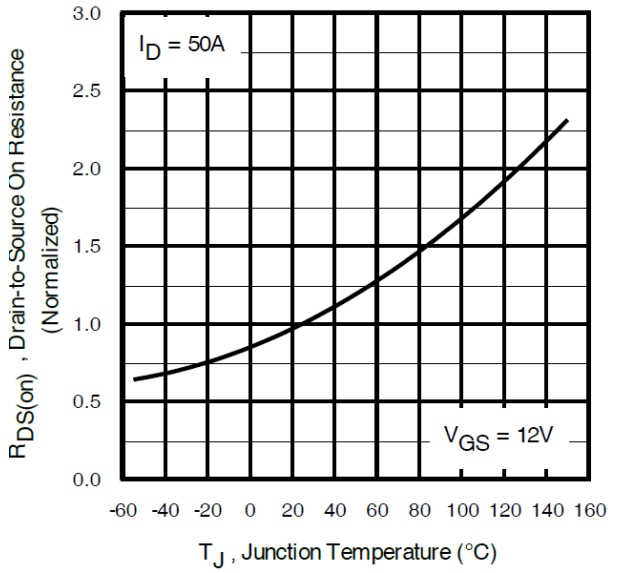



**Figure 5 Normalized On-Resistance Vs. Temperature**

## Electrical Characteristics Curves (Pre-irradiation)

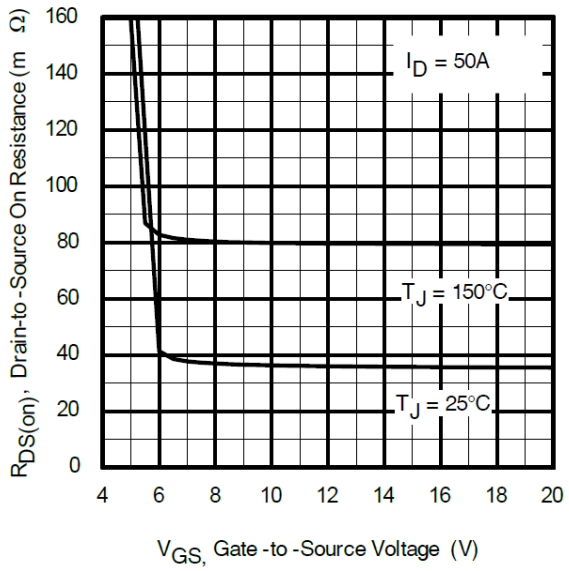



**Figure 6** Typical On-Resistance Vs Gate Voltage

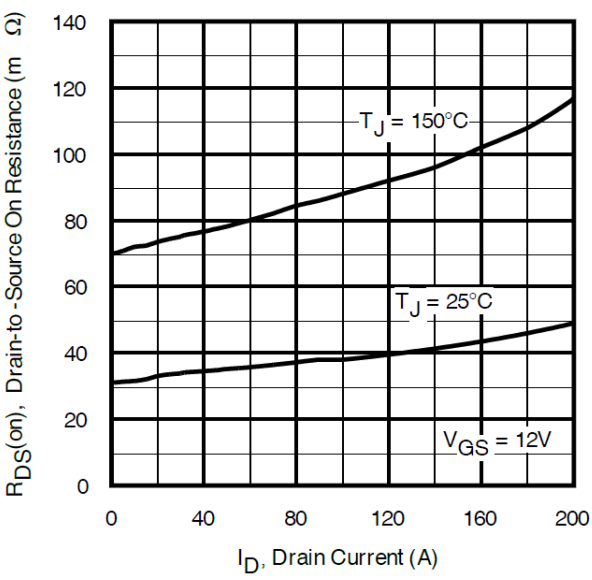



**Figure 7** Typical On-Resistance Vs Drain Current

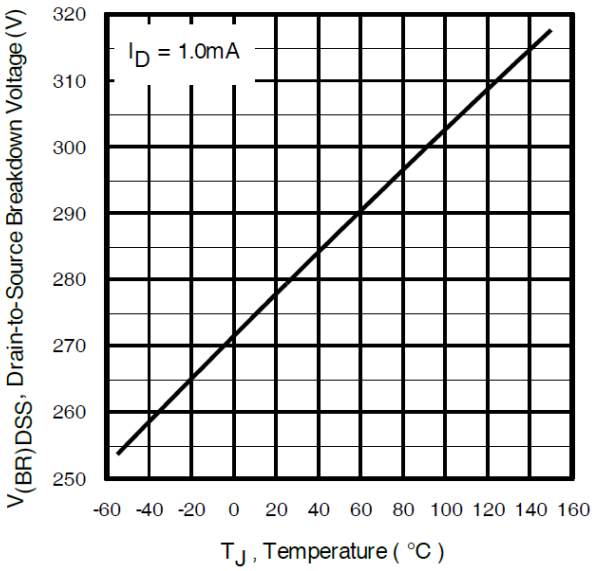



**Figure 8** Typical Drain-to-Source Breakdown Voltage Vs. Temperature

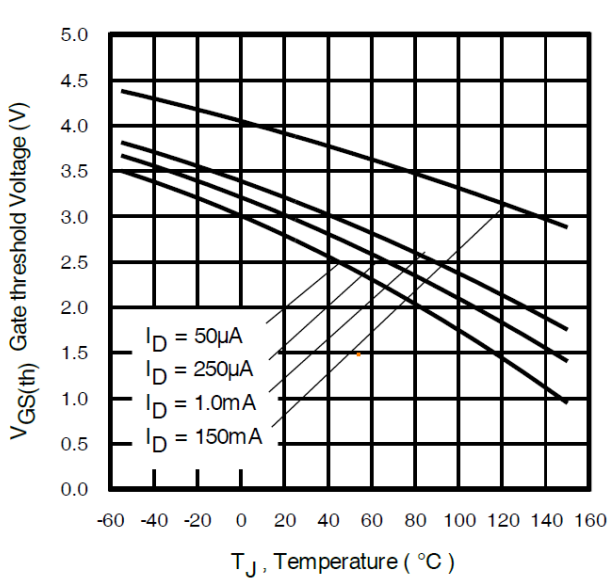



**Figure 9** Typical Gate-to-Source Voltage Vs. Temperature

## Electrical Characteristics Curves (Pre-irradiation)

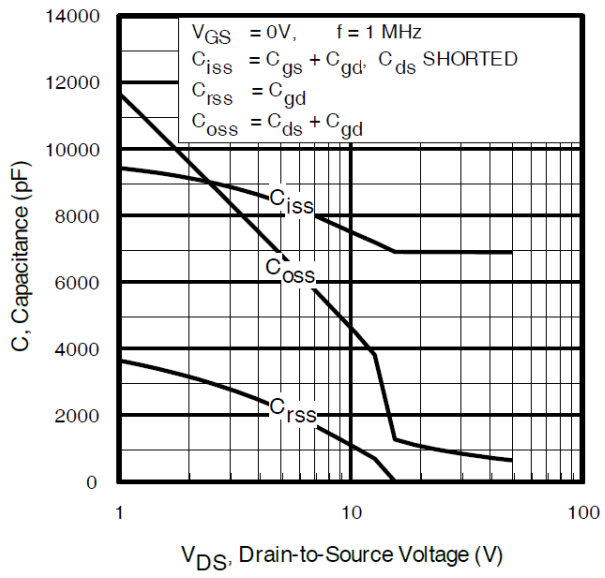



**Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage**

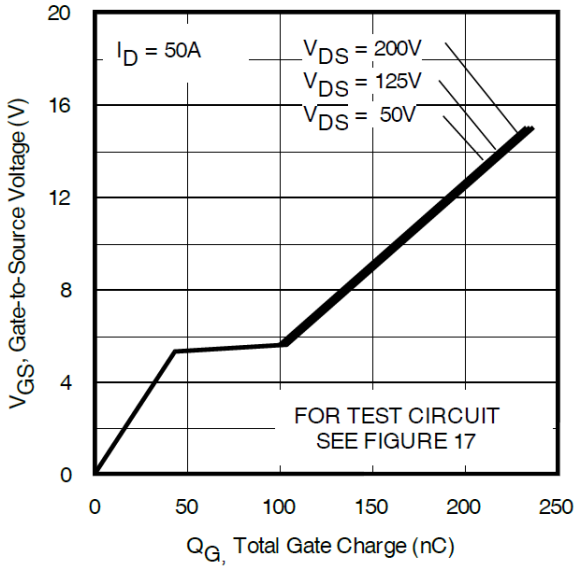



**Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge**

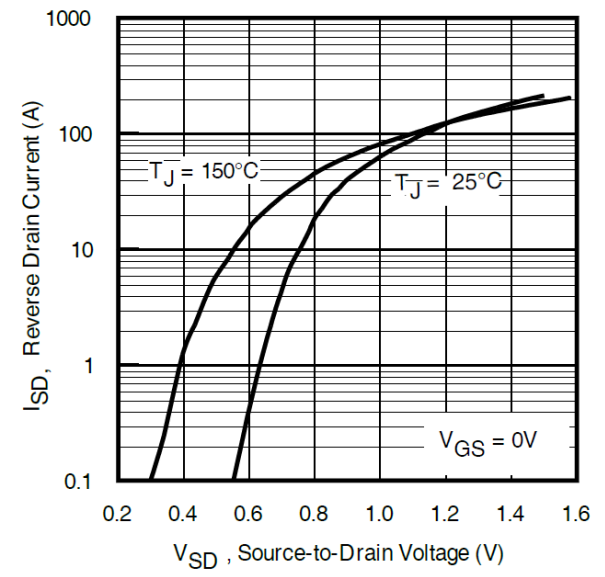



**Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage**

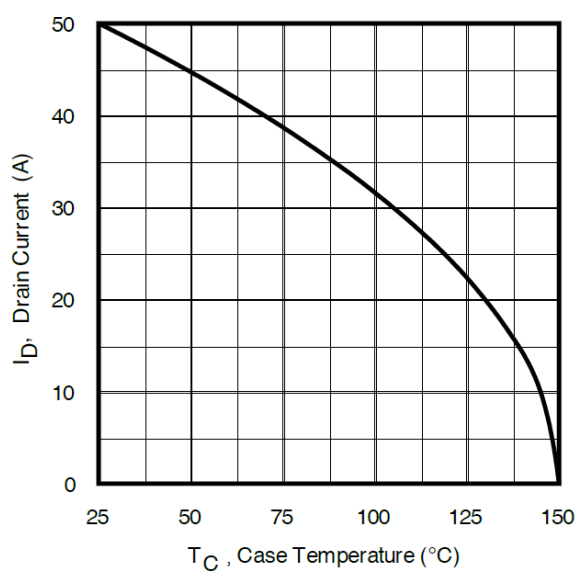



**Figure 13 Maximum Drain Current Vs. Temperature**

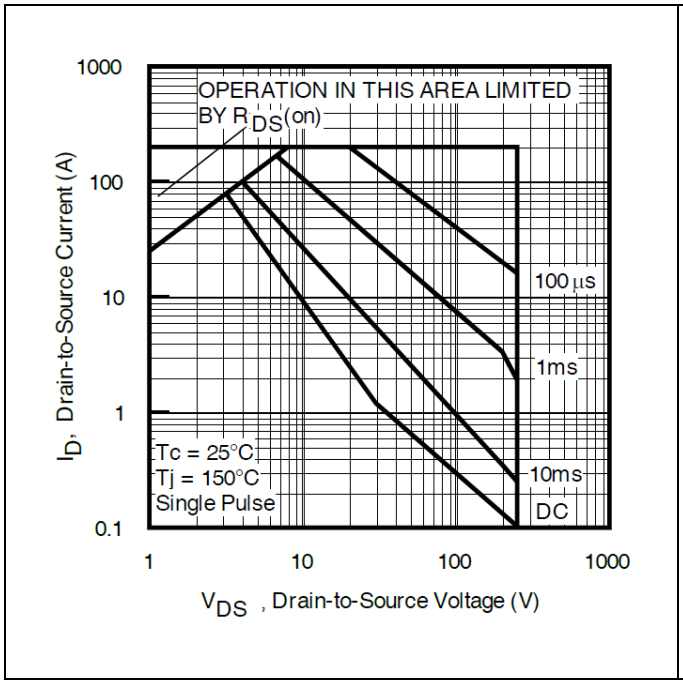



**Figure 14 Maximum Safe Operating Area**

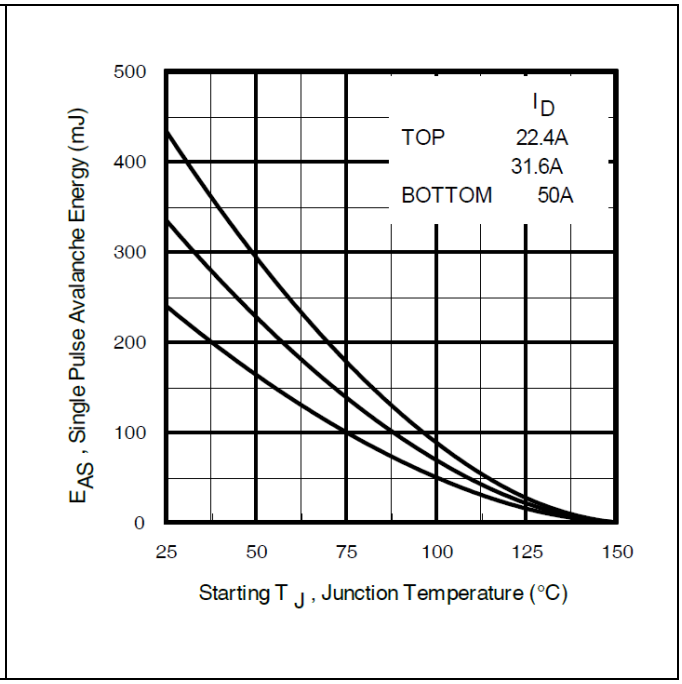



**Figure 15 Maximum Avalanche Energy Vs. Junction Temperature**

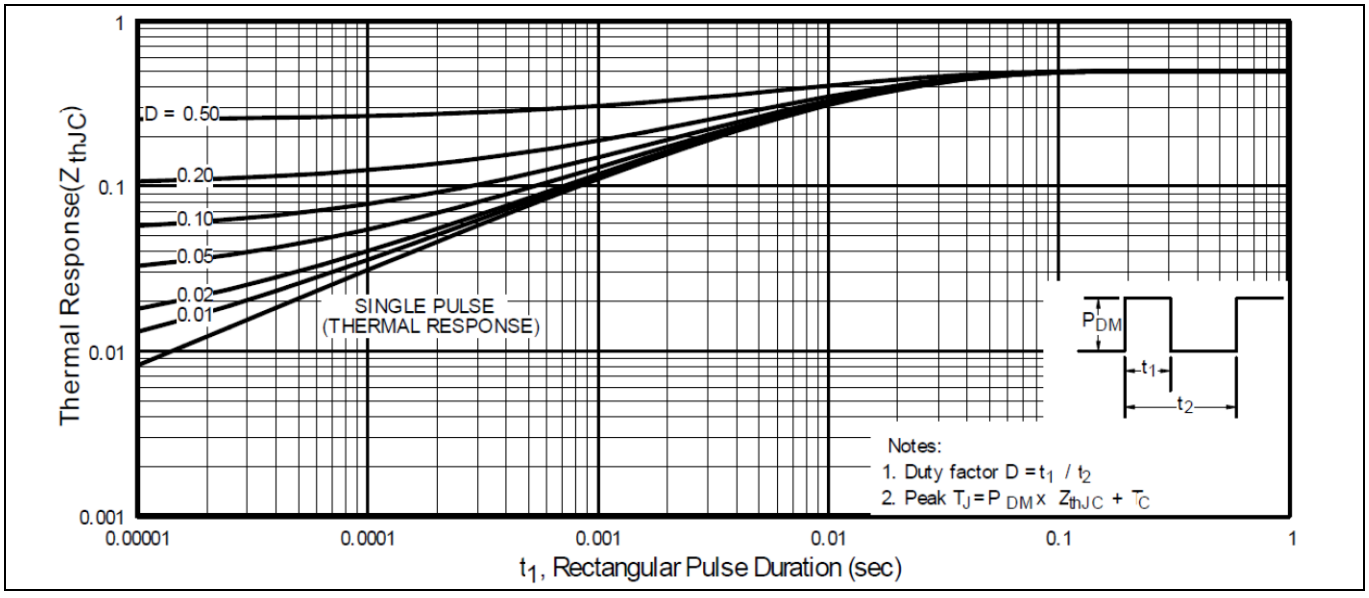



**Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case**

# 4 Test Circuits (Pre-irradiation)

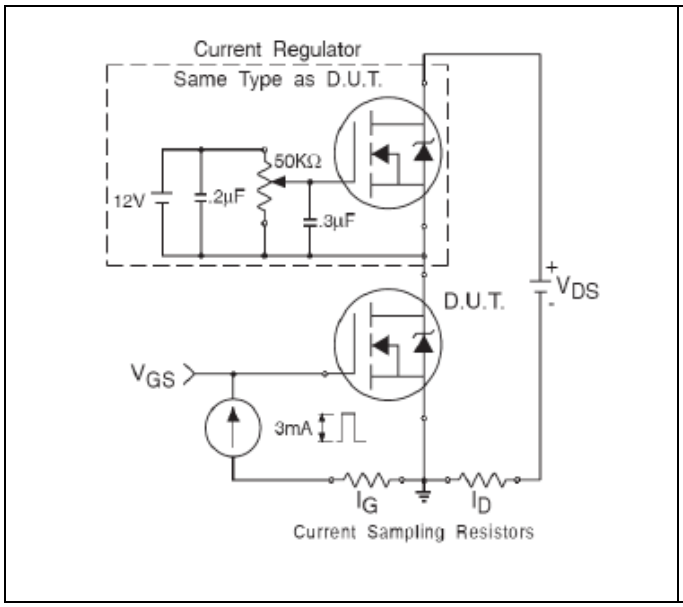



**Figure 17 Gate Charge Test Circuit**

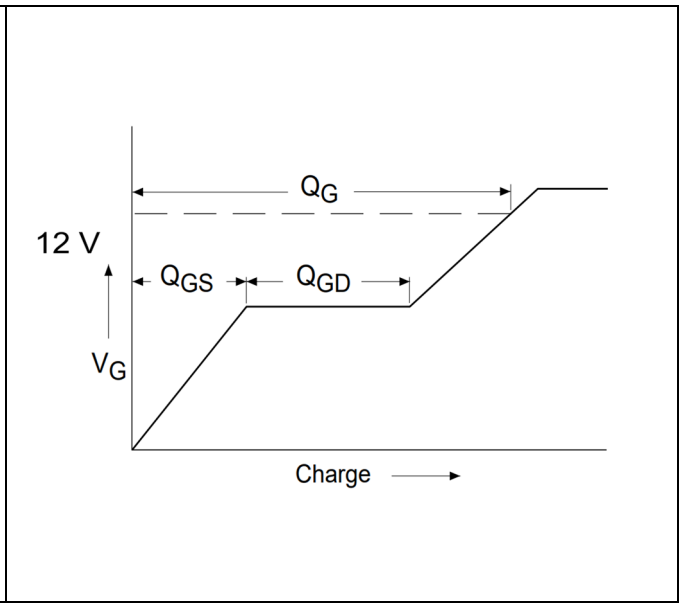



**Figure 18 Gate Charge Waveform**

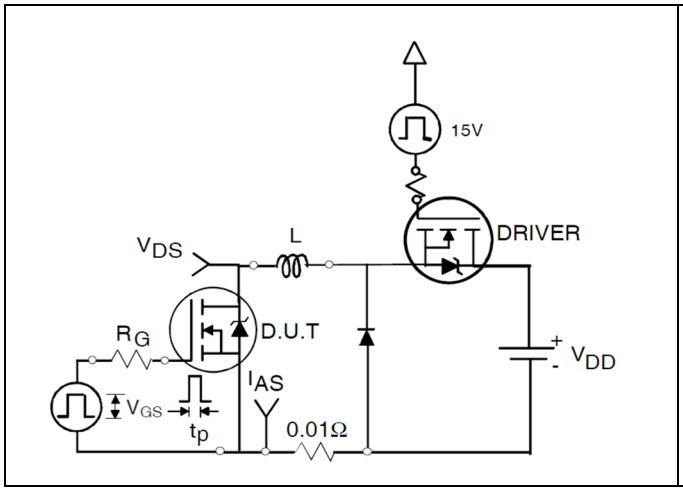



**Figure 19 Unclamped Inductive Test Circuit**

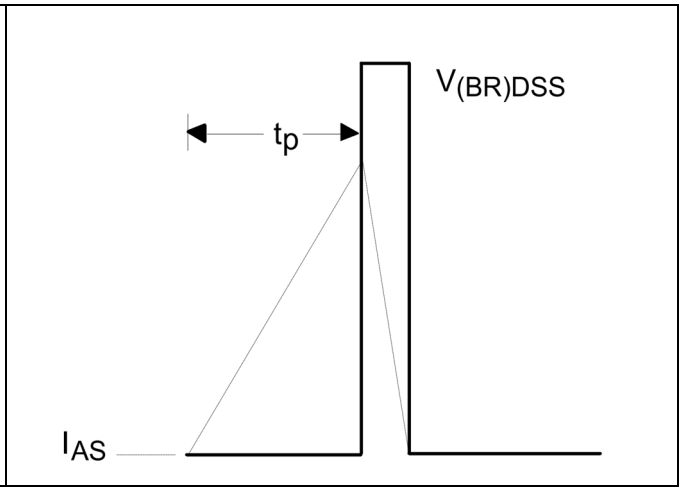



**Figure 20 Unclamped Inductive Waveform**

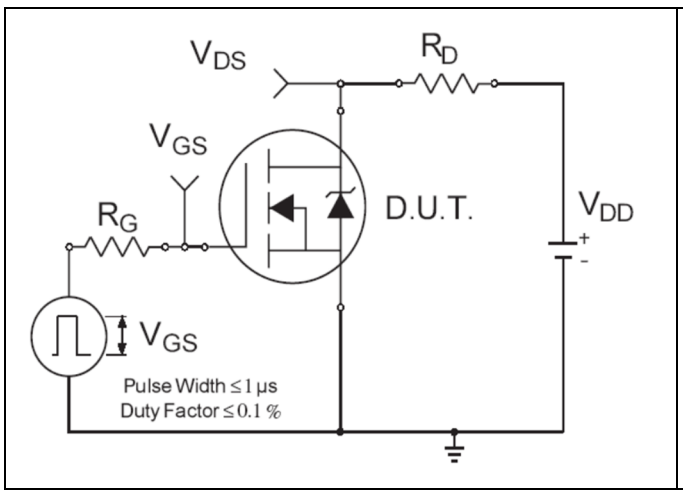



**Figure 21 Switching Time Test Circuit**

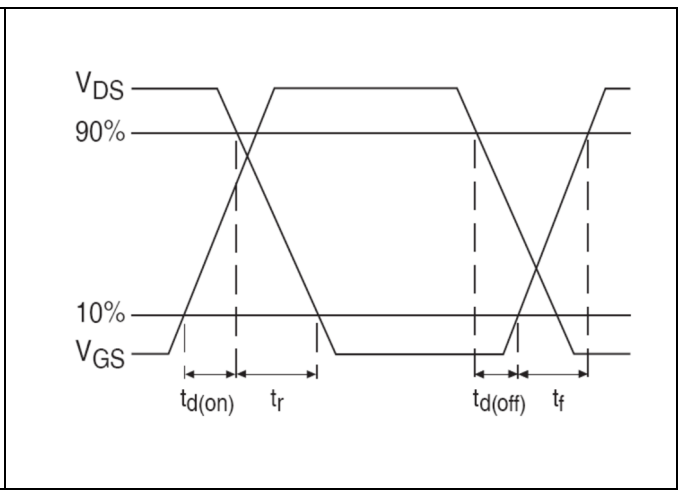
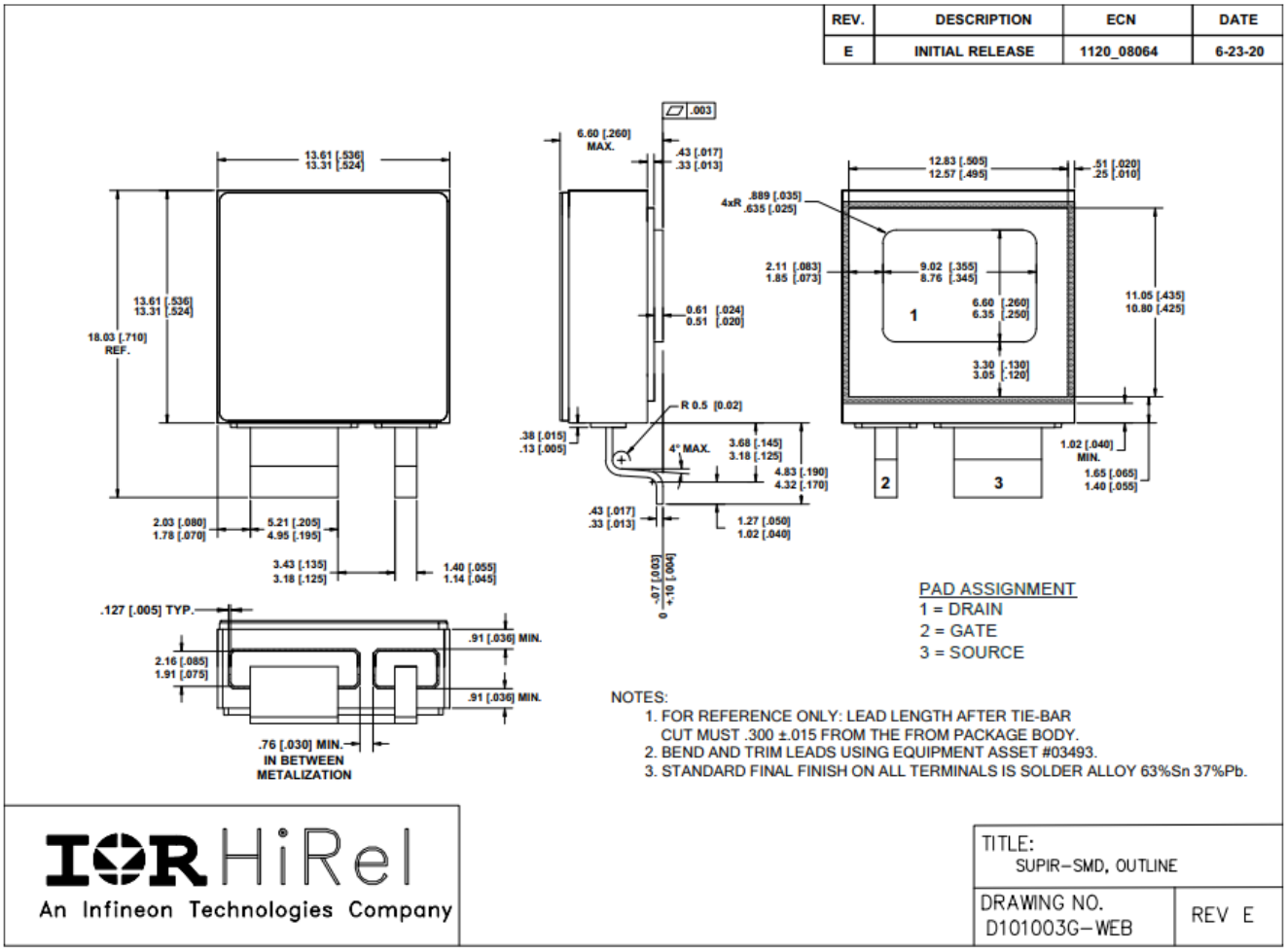



**Figure 22 Switching Time Waveforms**

# 5 Package Outline

**Note: For the most updated package outline, please see the website: SupIR-SMD™**



# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| | 10/25/2017 | Final datasheet with PD number (PD-97882) |
| Rev A | 12/18/2018 | Updated based on ECN-1120_06468 |
| Rev B | 04/14/2020 | Updated based on ECN-1120_07886-3 |
| Rev C | 03/07/2022 | Updated based on ECN-1120_08906 |

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