

IRHNS57264SE (JANSR2N7474U2A)

PD-97964A

**Radiation Hardened Power MOSFET
Surface Mount (SupIR-SMD™)
250V, 45A, N-channel, R5 Technology**

Features

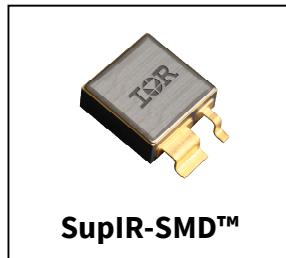
- Single event effect (SEE) hardened
- Low $R_{DS(on)}$
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Light weight
- Surface mount
- ESD rating: Class 3A per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications



Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 84 MeV/(mg/cm²). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNS57264SE	SupIR-SMD™	COTS	100 krad(Si)
JANSR2N7474U2A	SupIR-SMD™	JANS	100 krad(Si)

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Absolute Maximum Ratings**1 Absolute Maximum Ratings****Table 2 Absolute Maximum Ratings (Pre-Irradiation)**

Symbol	Parameter	Value	Unit
I_{D1} @ $V_{GS} = 12V$, $T_c = 25^\circ C$	Continuous Drain Current	45	A
I_{D2} @ $V_{GS} = 12V$, $T_c = 100^\circ C$	Continuous Drain Current	28	A
I_{DM} @ $T_c = 25^\circ C$	Pulsed Drain Current ¹	180	A
P_D @ $T_c = 25^\circ C$	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	222	mJ
I_{AR}	Avalanche Current ¹	45	A
E_{AR}	Repetitive Avalanche Energy ¹	25	mJ
dv/dt	Peak Diode Reverse Recovery ³	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ C$
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 0.22mH$, Peak $I_L = 45A$, $V_{GS} = 12V$ ³ $I_{SD} \leq 45A$, $di/dt \leq 274A/\mu s$, $V_{DD} \leq 250V$, $T_J \leq 150^\circ C$

Device Characteristics

2 Device Characteristics**2.1 Electrical Characteristics (Pre-Irradiation)****Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.28	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.06	Ω	V _{GS} = 12V, I _{D2} = 28A ¹
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1mA
G _{fs}	Forward Transconductance	27	—	—	S	V _{DS} = 15V, I _{D2} = 28A ¹
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	25		V _{DS} = 200V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	165	nC	I _{D1} = 45A
Q _{GS}	Gate-to-Source Charge	—	—	45		V _{DS} = 125V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	75		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time	—	—	35	ns	I _{D1} = 45A **
t _r	Rise Time	—	—	125		V _{DD} = 125V
t _{d(off)}	Turn-Off Delay Time	—	—	80		R _G = 2.35Ω
t _f	Fall Time	—	—	65		V _{GS} = 12V
L _s +L _D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C _{iss}	Input Capacitance	—	5045	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	781	—		
C _{rss}	Reverse Transfer Capacitance	—	70	—		

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

Device Characteristics**2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)****Table 4** Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	45	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	180	A	
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 45A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	—	560	ns	T _J = 25°C, I _F = 45A, V _{DD} ≤ 50V
Q _{rr}	Reverse Recovery Charge	—	—	8.6	μC	di/dt = 100A/μs ²
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics**Table 5** Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
R _{θJC}	Junction-to-Case	—	—	0.5	°C/W
R _{θJ-PCB}	Junction-to-PC Board (Soldered to 2" sq copper clad board)	—	1.6	—	

2.4 Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation**Table 6** Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation^{3, 4}

Symbol	Parameter	100krad (Si)		Unit	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	250	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	-100		V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	μA	V _{DS} = 200V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source On-State Resistance (TO-3) ²	—	0.061	Ω	V _{GS} = 12V, I _{D2} = 28A
R _{DS(on)}	Static Drain-to-Source On-State Resistance (SupIR-SMD TM) ²	—	0.060	Ω	V _{GS} = 12V, I _{D2} = 28A
V _{SD}	Diode Forward Voltage	—	1.2	V	V _{GS} = 0V, I _F = 45A

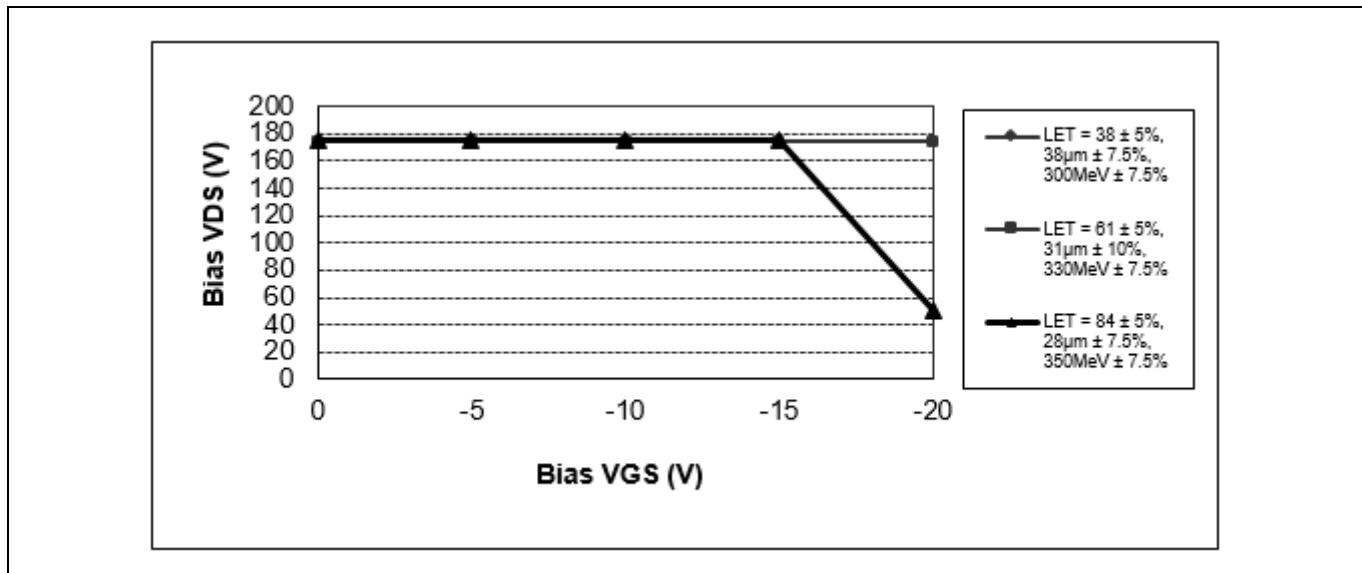
¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² Pulse width ≤ 300 μs; Duty Cycle ≤ 2%³ Total Dose Irradiation with V_{GS} Bias. V_{GS} = 12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.⁴ Total Dose Irradiation with V_{DS} Bias. V_{DS} = 200V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Device Characteristics**2.4.2 Single Event Effects – Safe Operating Area**

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V _{DS} (V)				
			V _{GS} = 0V	V _{GS} = -5V	V _{GS} = -10V	V _{GS} = -15V	V _{GS} = -20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	175	175	175	175	175
61 ± 5%	330 ± 7.5%	31 ± 10%	175	175	175	175	175
84 ± 5%	350 ± 7.5%	28 ± 7.5%	175	175	175	175	50

**Figure 1 Typical Single Event Effect, Safe Operating Area**

Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

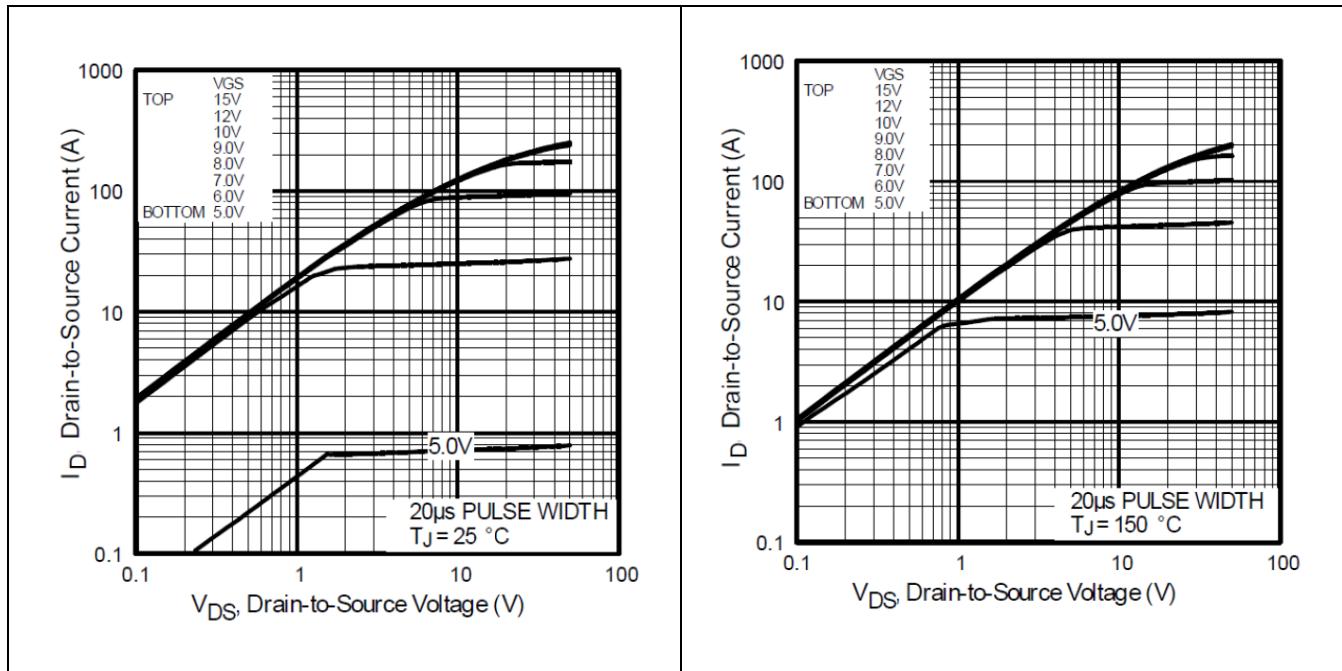


Figure 2 Typical Output Characteristics

Figure 3 Typical Output Characteristics

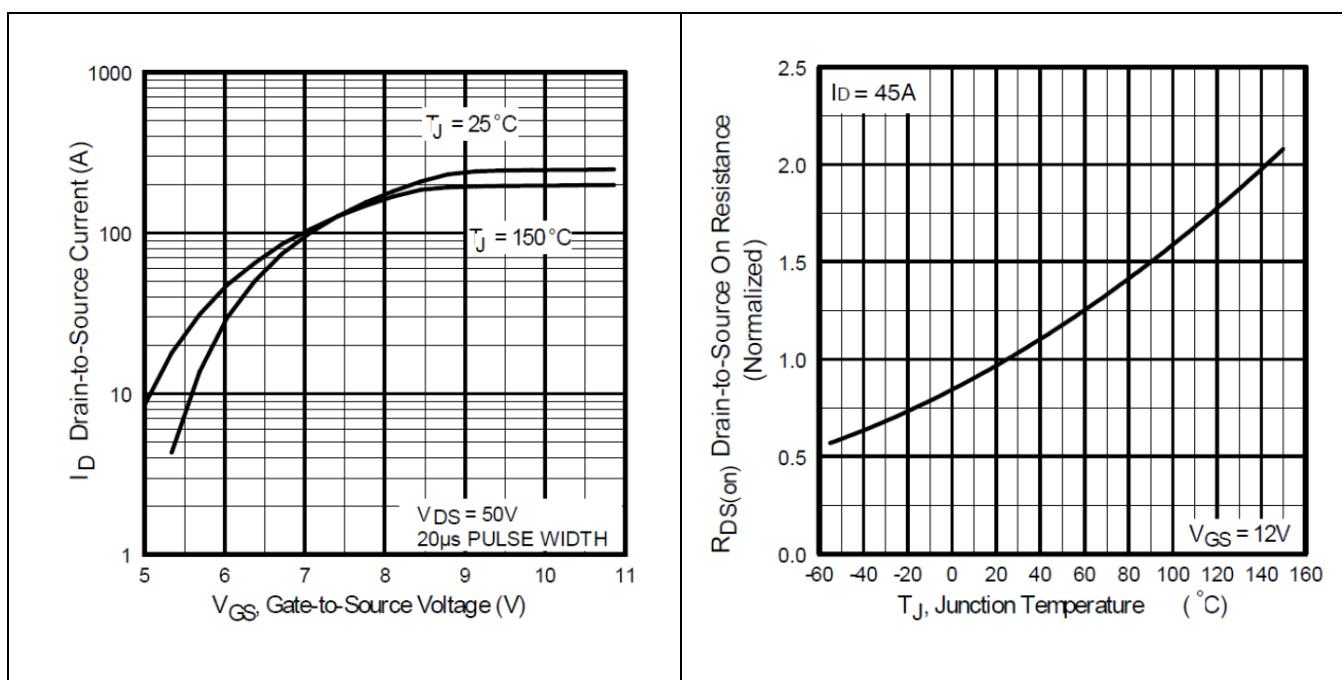
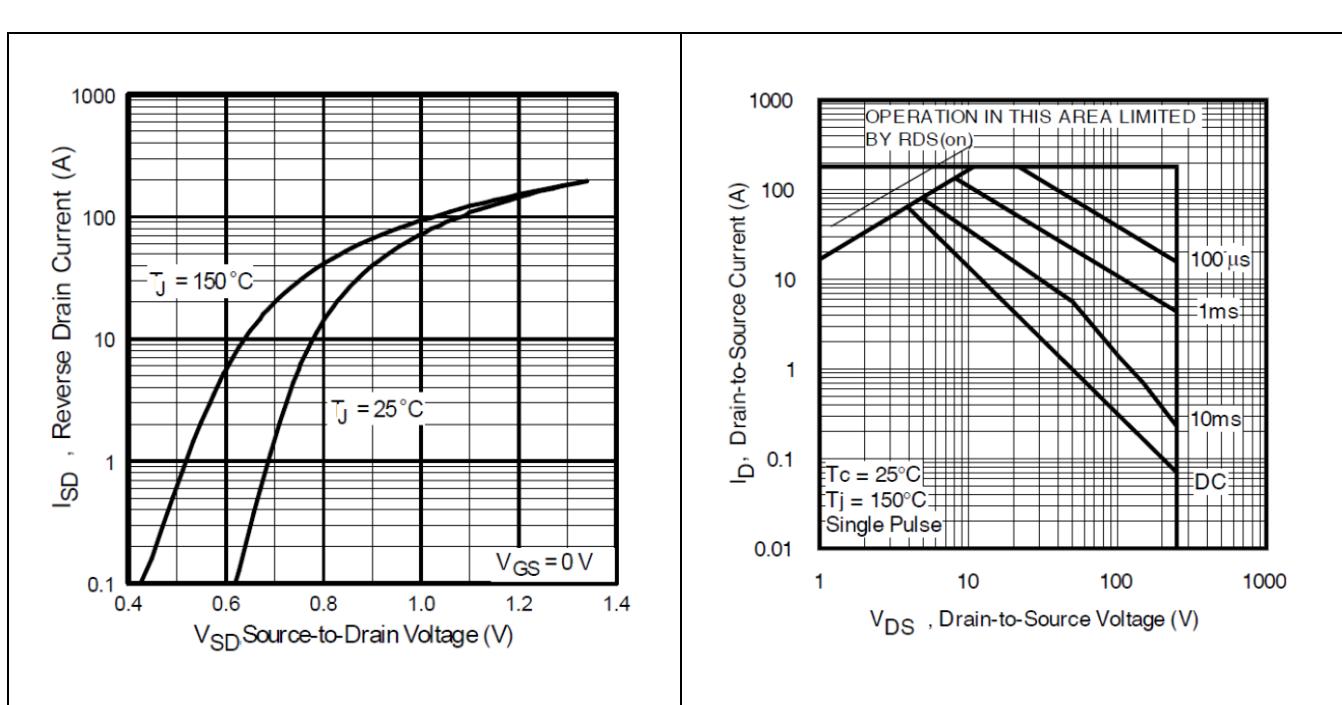
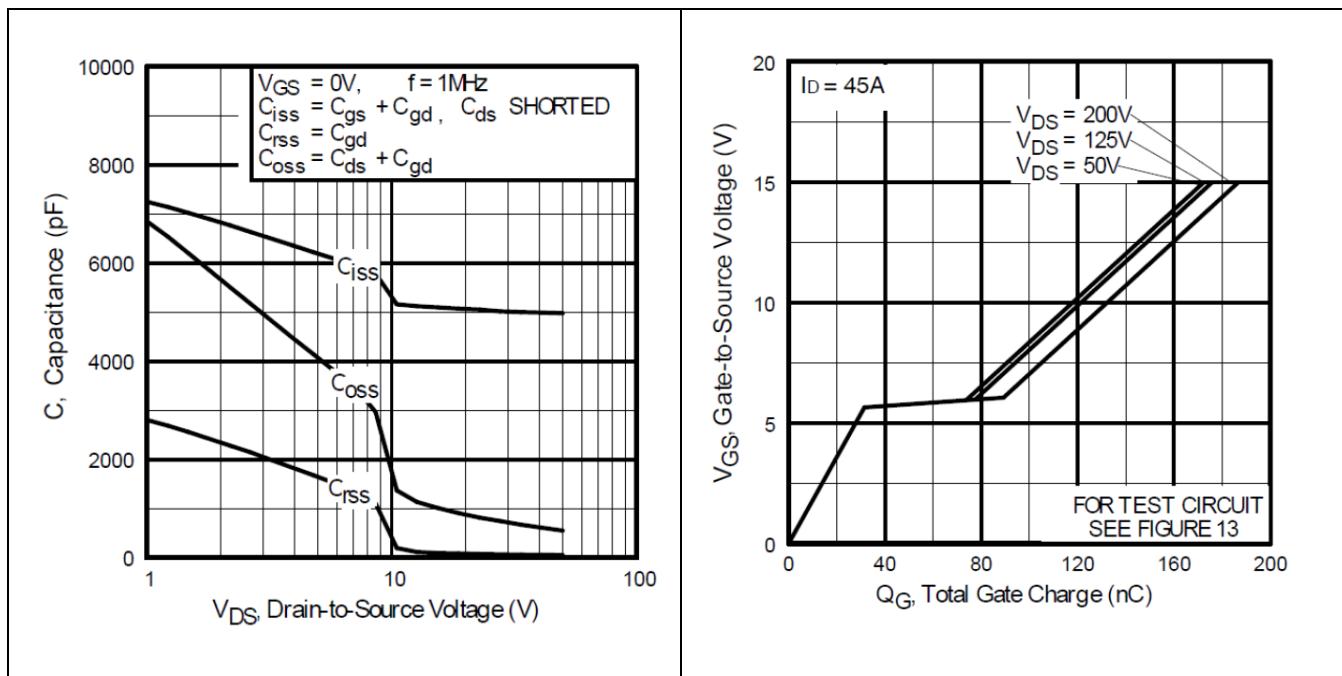


Figure 4 Typical Transfer Characteristics

Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)



Electrical Characteristics Curves (Pre-irradiation)

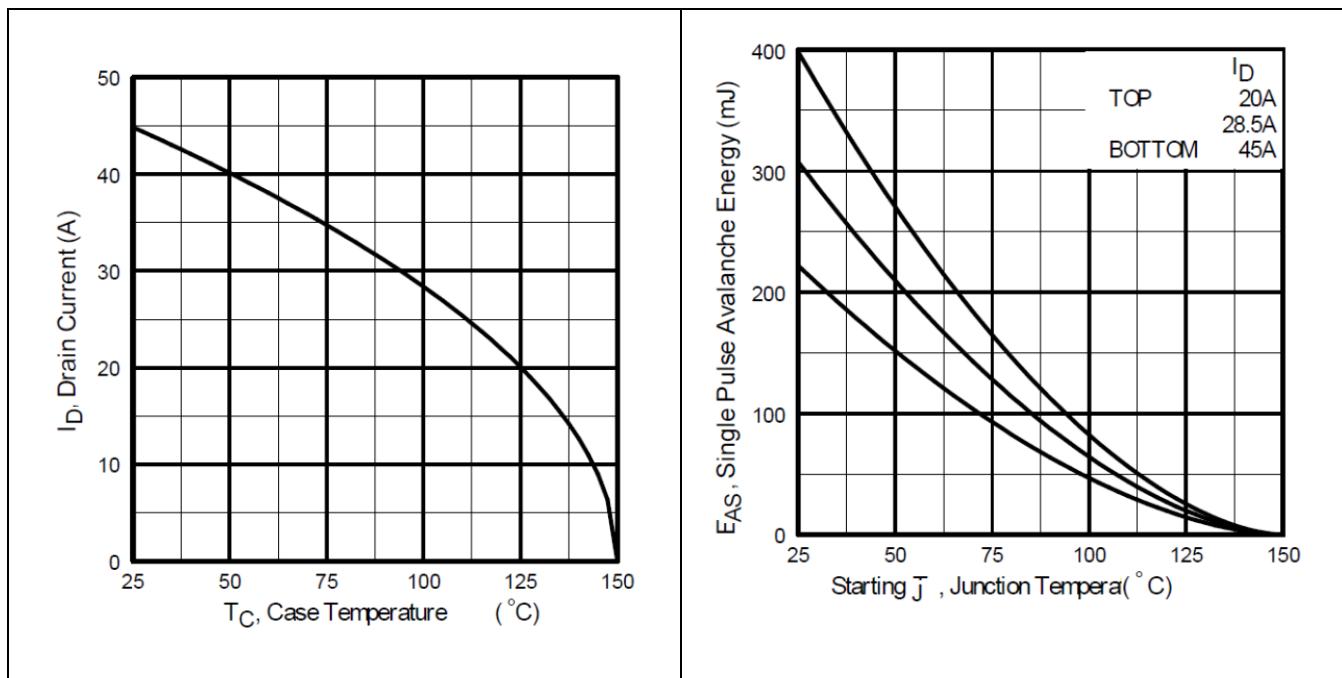


Figure 10 Maximum Drain Current Vs.
Case Temperature

Figure 11 Maximum Avalanche Energy Vs.
Junction Temperature

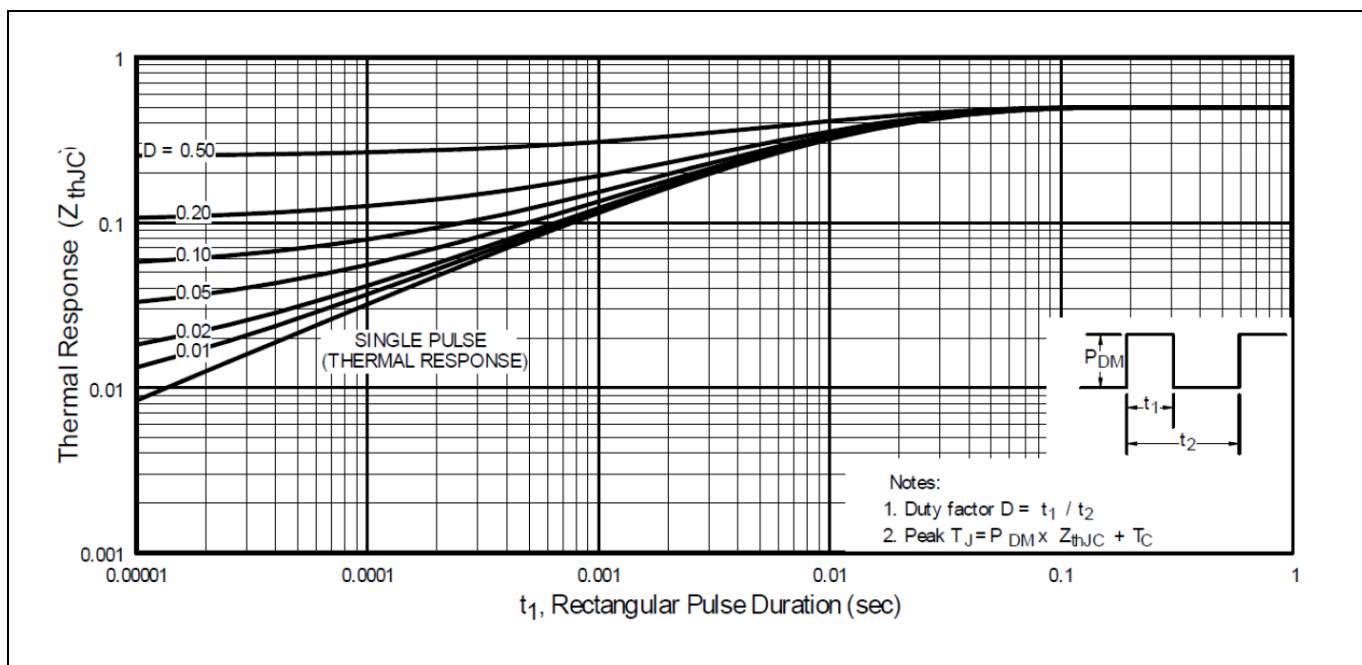


Figure 12 Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test Circuits (Pre-irradiation)

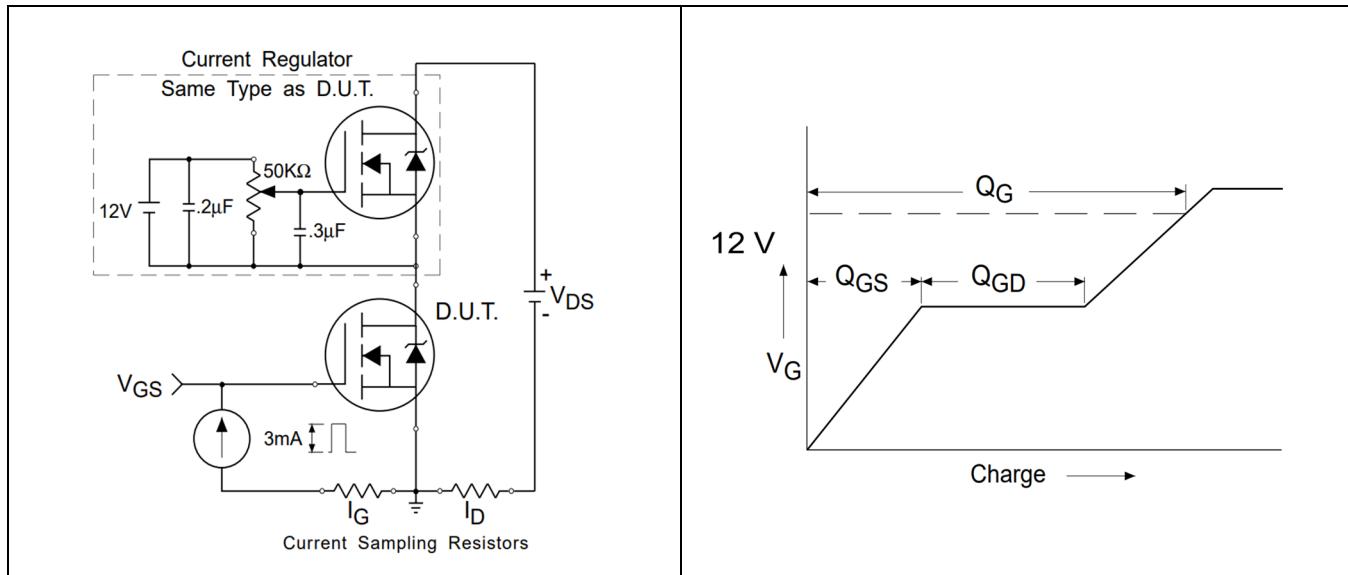
4 Test Circuits (Pre-irradiation)

Figure 13 Gate Charge Test Circuit

Figure 14 Gate Charge Waveform

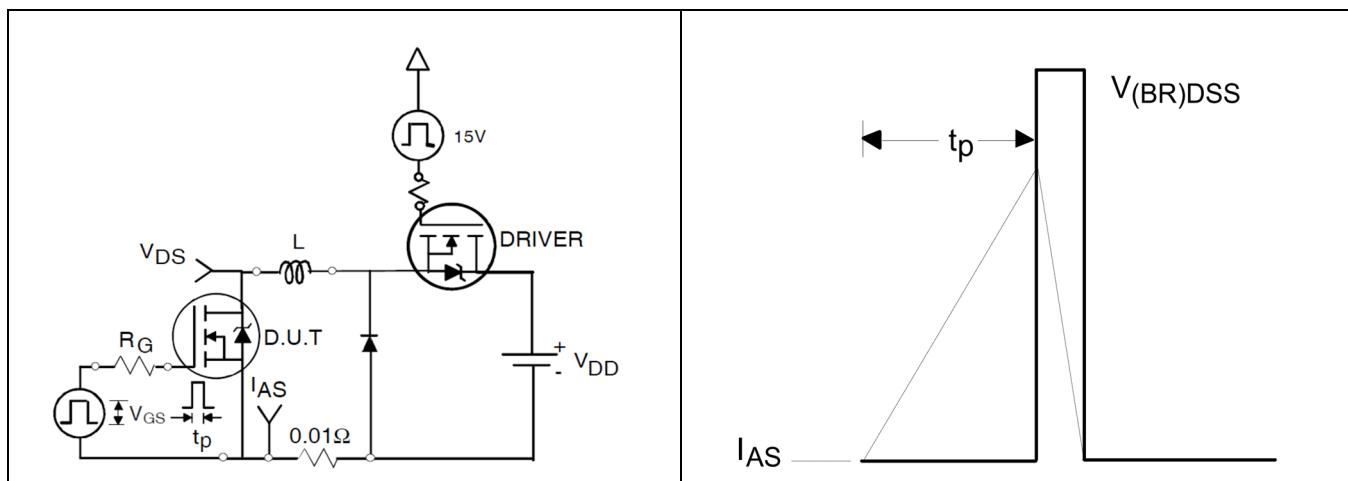


Figure 15 Unclamped Inductive Test Circuit

Figure 16 Unclamped Inductive Waveform

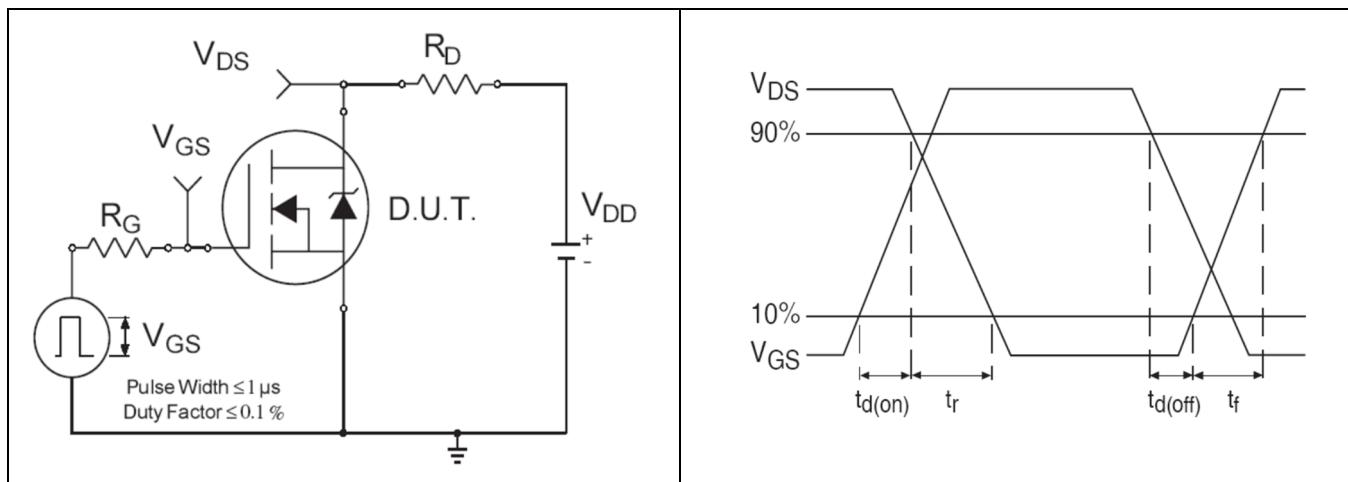


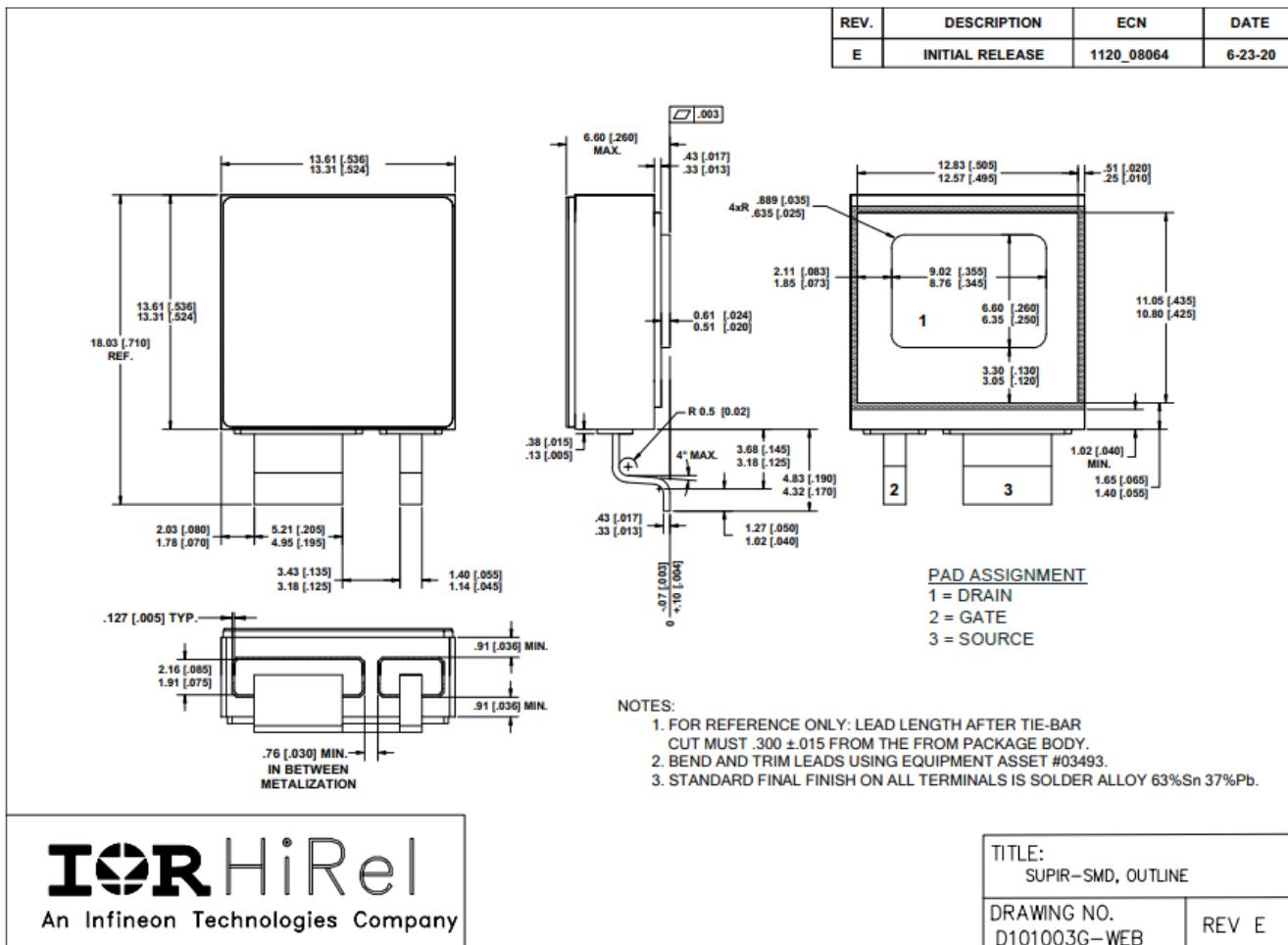
Figure 17 Switching Time Test Circuit

Figure 18 Switching Time Waveforms

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [SupIR-SMDTM](#)



Revision history

Document version	Date of release	Description of changes
	04/10/2020	Datasheet (PD-97964)
Rev A	08/09/2021	Updated based on ECN-1120_08659

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