

PD-97818D

Radiation Hardened Power MOSFET Surface Mount (SMD-0.2) 250V, 3.7A, N-channel, R5 Technology

#### **Features**

- Single event effect (SEE) hardened
- Low R<sub>DS(on)</sub>
- Low total gate charge
- Simple drive requirements
- Low total gate charge
- Hermetically sealed
- Surface mount
- Ceramic package
- Light weight
- ESD rating: Class 1B per MIL-STD-750, Method 1020

### **Potential Applications**

- DC-DC converter
- Motor drives

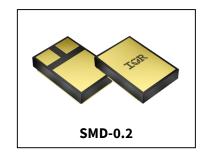
# **Product Summary**

BV<sub>DSS</sub>: 250V

• I<sub>D</sub>: 3.7A

•  $R_{DS(on), max}$ : 1.7 $\Omega$ 

• Q<sub>G, max</sub>: 9.1nC



#### **Product Validation**

Qualified to IR HiRel's S-level screening flow which is equivalent to MIL-PRF-19500

## **Description**

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of  $80 \text{MeV} \cdot \text{cm}^2/\text{mg}$ . The combination of low  $R_{DS(on)}$  and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

## **Ordering Information**

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNM57214SE	SMD-0.2	COTS	100 krad(Si)
			` '
IRHNM57214SESCS	SMD-0.2	S-level	100 krad(Si)
IRHNMC57214SE	SMD-0.2 ceramic lid	COTS	100 krad(Si)
IRHNMC57214SESCS	SMD-0.2 ceramic lid	S-level	100 krad(Si)





#### **Table of contents**

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Pote	ntial Applicationsntial Applications	<b>1</b>
Prod	luct Validation	1
	ription	
	ering Information	
	e of contents	
1	Absolute Maximum Ratings	
2	Device Characteristics	
2.1	Electrical Characteristics (Pre-Irradiation)	
2.2	Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)	5
2.3	Thermal Characteristics	5
2.4	Radiation Characteristics	5
2.4.1	Electrical Characteristics — Post Total Dose Irradiation	5
2.4.2	Single Event Effects — Safe Operating Area	6
3	Electrical Characteristics Curves (Pre-irradiation)	7
4	Test Circuits (Pre-irradiation)	11
5	Package Outline	12
Revis	sion history	





**Absolute Maximum Ratings** 

# 1 Absolute Maximum Ratings

 Table 2
 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1}$ @ $V_{GS}$ = 12V, $T_{C}$ = 25°C	Continuous Drain Current	3.7	А
$I_{D2}$ @ $V_{GS} = 12V$ , $T_{C} = 100$ °C	Continuous Drain Current	2.4	А
$I_{DM}$ @ $T_C = 25$ °C	Pulsed Drain Current <sup>1</sup>	14.8	А
$P_{D}$ @ $T_{C} = 25^{\circ}C$	Maximum Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>2</sup>	34	mJ
$I_{AR}$	Avalanche Current <sup>1</sup>	3.7	А
E <sub>AR</sub>	Repetitive Avalanche Energy <sup>1</sup>	4.0	mJ
dv/dt	Peak Diode Reverse Recovery <sup>3</sup>	3.7	V/ns
T <sub>J</sub> Operating Junction and Storage Temperature Range		-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	0.25 (Typical)	g

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 $<sup>^{\</sup>rm 1}$  Repetitive Rating; Pulse width limited by maximum junction temperature.

 $<sup>^2</sup>$  V<sub>DD</sub> = 50V, starting T<sub>J</sub> = 25°C, L = 5.0mH, Peak I<sub>L</sub> = 3.7A, V<sub>GS</sub> = 12V

 $<sup>^3</sup>$   $I_{SD}$   $\leq$  3.7A, di/dt  $\leq$  1018A/ $\mu s,\,V_{DD}$   $\leq$  250V,  $T_{J}$   $\leq$  150°C



**Device Characteristics** 

### 2 Device Characteristics

### 2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions	
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	250	ı	_	V	$V_{GS} = 0V, I_{D} = 1.0 \text{mA}$	
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	_	0.27	_	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA	
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	_	l	1.7	Ω	$V_{GS} = 12V$ , $I_{D2} = 2.4A^{1}$	
$V_{GS(th)}$	Gate Threshold Voltage	2.5	1	4.5	V	V = V   = 1.0mA	
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	_	-9.1	_	mV/°C	$V_{DS} = V_{GS}$ , $I_D = 1.0 \text{mA}$	
Gfs	Forward Transconductance	2.0	_	_	S	$V_{DS} = 15V$ , $I_{D2} = 2.4A^{1}$	
	7 6 1 1/1 5 : 6 1	_	_	10		$V_{DS} = 200V, V_{GS} = 0V$	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	_	_	25	μΑ	$V_{DS} = 200V, V_{GS} = 0V, T_{J} = 125^{\circ}C$	
	Gate-to-Source Leakage Forward	_	_	100	_	V <sub>GS</sub> = 20V	
$I_{GSS}$	Gate-to-Source Leakage Reverse	_	_	-100	nA	V <sub>GS</sub> = -20V	
$\overline{Q_G}$	Total Gate Charge	_	_	9.1		I <sub>D1</sub> = 3.7A	
$Q_{GS}$	Gate-to-Source Charge	_	_	2.9	nC	V <sub>DS</sub> = 125V	
$Q_{GD}$	Gate-to-Drain ('Miller') Charge	_	_	4.3		V <sub>GS</sub> = 12V	
t <sub>d(on)</sub>	Turn-On Delay Time	_	_	7.5		I <sub>D1</sub> = 3.7A **	
t <sub>r</sub>	Rise Time	_	_	6.6	]	$V_{DD} = 125V$	
$\overline{t_{d(off)}}$	Turn-Off Delay Time	_		16.8	ns	$R_G = 7.5\Omega$	
t <sub>f</sub>	Fall Time	_	_	14		$V_{GS} = 12V$	
L <sub>s</sub> +L <sub>D</sub>	Total Inductance	_	6.8	_	nH	Measured from center of Drain pad to center of Source pad	
C <sub>iss</sub>	Input Capacitance	_	308	_		$V_{GS} = 0V$	
C <sub>oss</sub>	Output Capacitance	_	51	_	pF	$V_{DS} = 20V$	
C <sub>rss</sub>	Reverse Transfer Capacitance	_	1.2	_		f = 1.0MHz	
$R_{G}$	Gate Resistance	_	6.6	_	Ω	f = 1.0MHz, open drain	

<sup>\*\*</sup> Switching speed maximum limits are based on manufacturing test equipment and capability.

 $<sup>^1</sup>$  Pulse width  $\leq$  300  $\mu s;$  Duty Cycle  $\leq$  2%

#### Radiation Hardened Power MOSFET Surface-Mount (SMD-0.2)



**Device Characteristics** 

### 2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions	
Is	Continuous Source Current (Body Diode)	_	_	3.7	Α		
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>1</sup>	_	_	14.8	Α		
$V_{\text{SD}}$	Diode Forward Voltage	_	_	1.0	V	$T_J = 25$ °C, $I_S = 3.7$ A, $V_{GS} = 0$ V <sup>2</sup>	
t <sub>rr</sub>	Reverse Recovery Time	_	_	145	ns	$T_J = 25$ °C, $I_F = 3.7$ A, $V_{DD} \le 25$ V	
Qrr	Reverse Recovery Charge	_	_	857	nC	di/dt = 100A/μs <sup>2</sup>	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )					

#### 2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Тур.	Max.	Unit
$R_{ heta JC}$	Junction-to-Case	_	1	3.12	°C/W

### 2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

#### 2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T<sub>J</sub> = 25°C, Post Total Dose Irradiation <sup>3, 4</sup>

Cymphal	Davamatav	Up to 100	krad (Si)	lle:t	Test Conditions	
Symbol	Parameter	Min.	Max.	Unit		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	250	_	V	$V_{GS} = 0V, I_D = 1.0 mA$	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	$V_{DS} = V_{GS}, I_{D} = 1.0 \text{mA}$	
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	_	100	Λ	V <sub>GS</sub> = 20V	
	Gate-to-Source Leakage Reverse	_	-100	nA	V <sub>GS</sub> = -20V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	_	10	μΑ	$V_{DS} = 200V, V_{GS} = 0V$	
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance (TO-3) <sup>2</sup>	_	1.7	Ω	$V_{GS} = 12V, I_{D2} = 2.4A$	
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance (SMD-0.2) <sup>2</sup>	_	1.7	Ω	$V_{GS} = 12V, I_{D2} = 2.4A$	
$\overline{V_{SD}}$	Diode Forward Voltage	_	1.0	V	$V_{GS} = 0V, I_F = 3.7A$	

 $<sup>^{\</sup>rm 1}$  Repetitive Rating; Pulse width limited by maximum junction temperature.

 $<sup>^2</sup>$  Pulse width  $\leq$  300  $\mu$ s; Duty Cycle  $\leq$  2%

<sup>&</sup>lt;sup>3</sup> Total Dose Irradiation with V<sub>GS</sub> Bias. V<sub>GS</sub> = 12V applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

 $<sup>^4</sup>$  Total Dose Irradiation with  $V_{DS}$  Bias.  $V_{DS}$  = 200V applied and  $V_{GS}$  = 0 during irradiation per MIL-STD-750, Method 1019, condition A.



**Device Characteristics** 

## 2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Worst Case Single Event Effects Safe Operating Area

lan	LET	Energy	Range	V <sub>DS</sub> (V)					V <sub>DS</sub> (V)			
lon	(MeV·cm²/mg)	(MeV)	(μm)	$V_{GS} = 0V$	$V_{GS} = -5V$	V <sub>GS</sub> = -10V	V <sub>GS</sub> = -15V	V <sub>GS</sub> = -20V				
Br	36.7	309	39.5	250	250	250	250	250				
1	59.8	341	32.5	250	250	250	250	240				
Au	82.3	350	28.4	250	250	225	175	50				

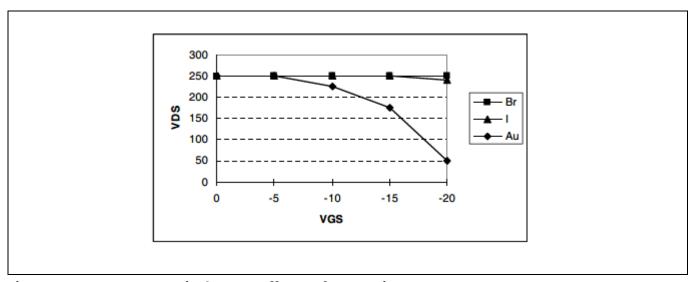


Figure 1 Worst Case Single Event Effect, Safe Operating Area



**Electrical Characteristics Curves (Pre-irradiation)** 

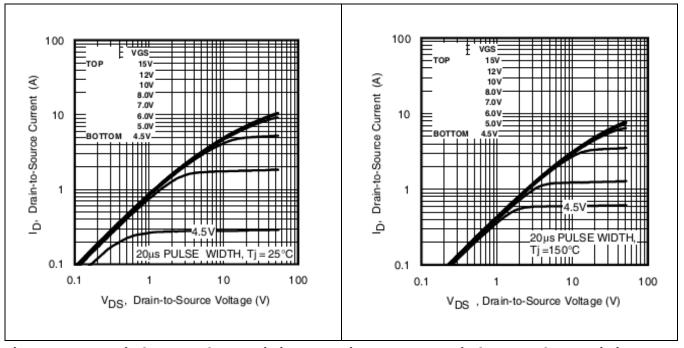


Figure 2 Typical Output Characteristics Figure 3 Typical Output Characteristics

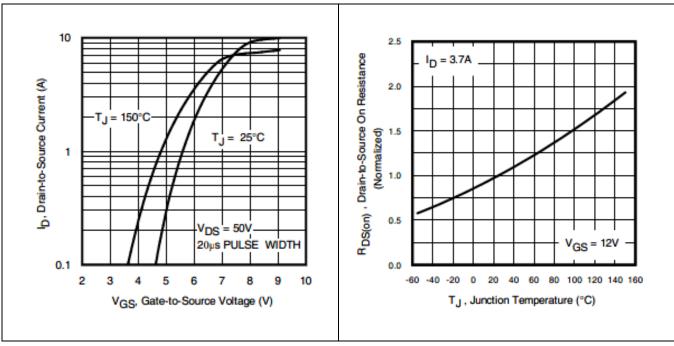


Figure 4 Typical Transfer Characteristics Figure 5 Normalized On-Resistance Vs.

Temperature





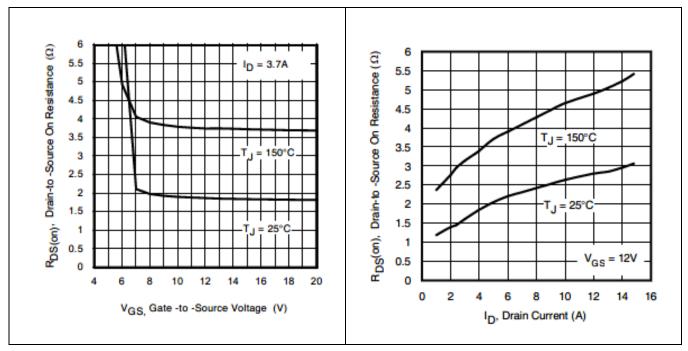


Figure 6 Typical On-Resistance Vs.
Gate Voltage

Figure 7 Typical On-Resistance Vs.

Drain Current

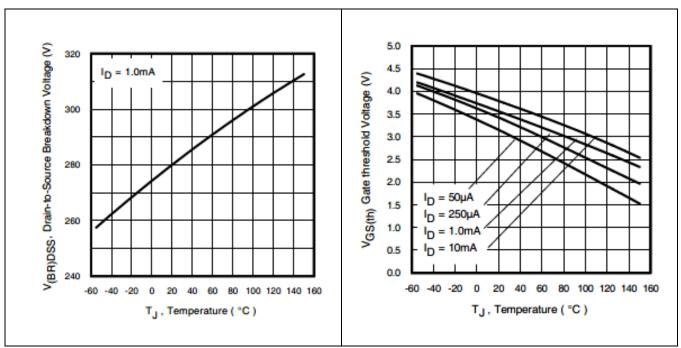


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

Figure 9 Typical Threshold Voltage Vs.
Temperature





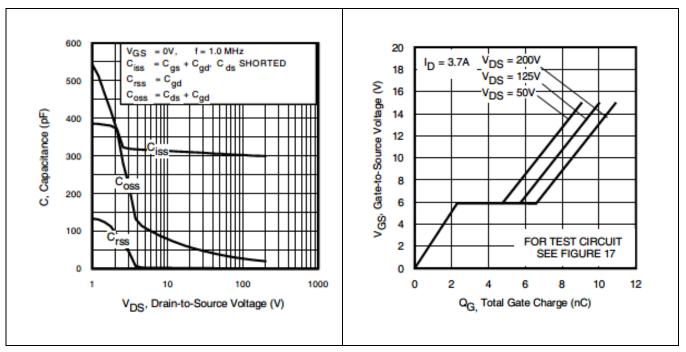


Figure 10 Typical Capacitance Vs.

Drain-to-Source Voltage

Figure 11 Gate-to-Source Voltage Vs.

Typical Gate Charge

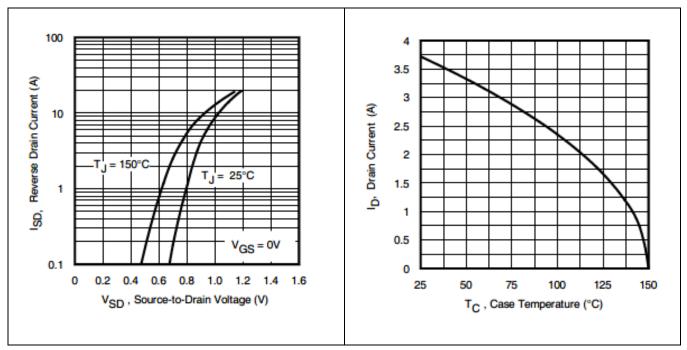


Figure 12 Typical Source-Drain Current Vs.
Diode Forward Voltage

Figure 13 Maximum Drain Current Vs. Case Temperature





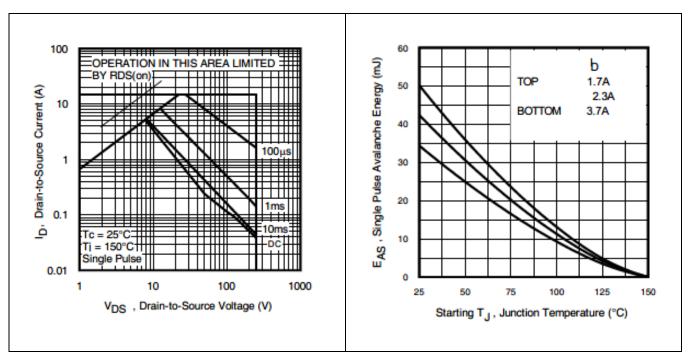


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Avalanche Energy Vs.
Junction Temperature

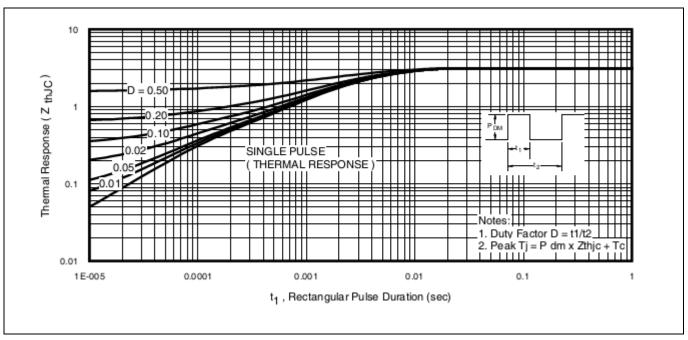


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Test Circuits (Pre-irradiation)** 

# 4 Test Circuits (Pre-irradiation)

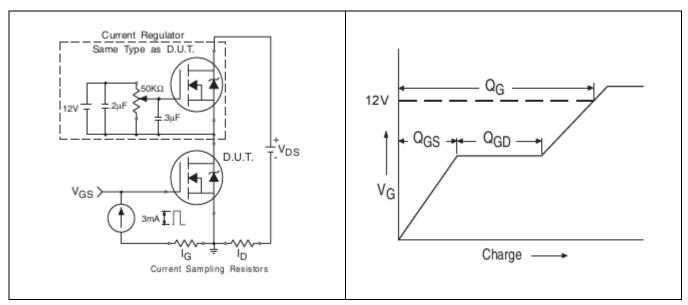


Figure 17 Gate Charge Test Circuit

Figure 18 Gate Charge Waveform

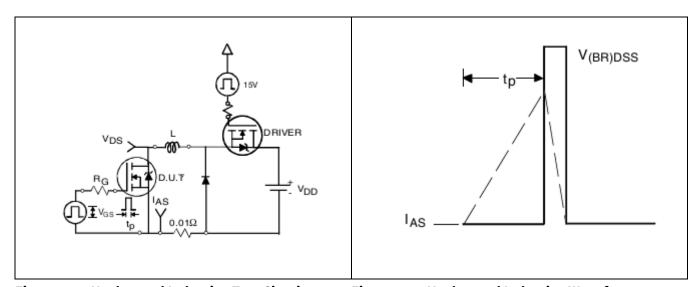


Figure 19 Unclamped Inductive Test Circuit

Figure 20 Unclamped Inductive Waveform

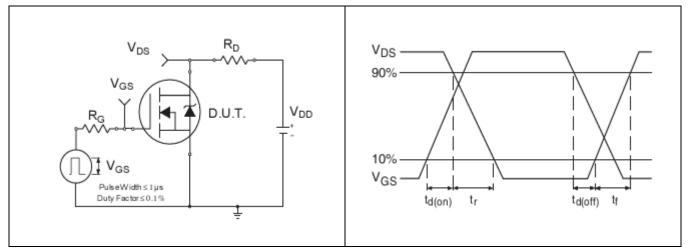


Figure 21 Switching Time Test Circuit

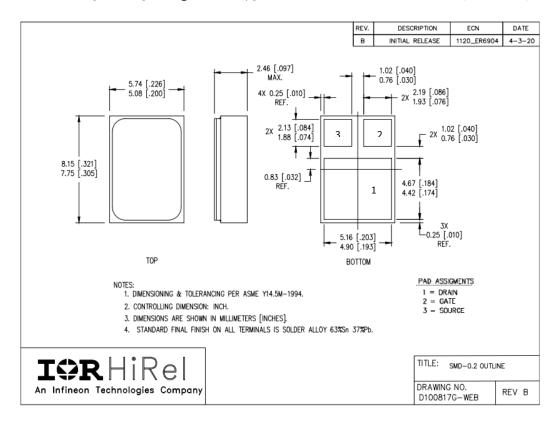
Figure 22 Switching Time Waveforms



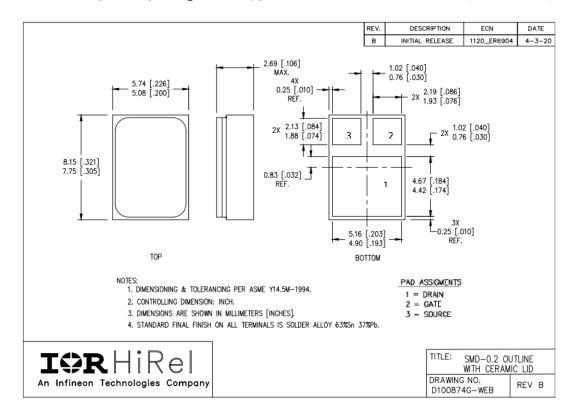
**Package Outline** 

## 5 Package Outline

Note: For the most updated package outline, please see the website: SMD-0.2 (Metal Lid)



Note: For the most updated package outline, please see the website: SMD-0.2 (Ceramic Lid)







**Revision history** 

# **Revision history**

Document version	Date of release	Description of changes
	02/12/2014	Datasheet (PD-97818)
Rev A	10/7/2016	Updated based on ECN-1120_04671
Rev B	06/16/2017	Updated based on ECN-1120_05233
Rev C	11/13/2019	Updated based on ECN-1120_07618
Rev D	05/23/2022	Updated based on ECN-1120_08905

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