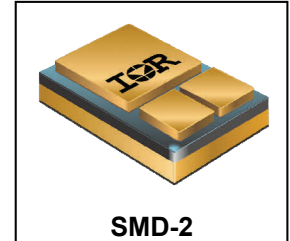


**RADIATION HARDENED  
POWER MOSFET  
SURFACE MOUNT (SMD-2)**

**200V, N-CHANNEL**  
**R<sub>6</sub> TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	I <sub>D</sub>
IRHNA6S7260	100 kRads(Si)	0.028Ω	56A*
IRHNA6S3260	300 kRads(Si)	0.028Ω	56A*



**Description**

IR HiRel R6 S-line technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 60 (MeV/(mg/cm<sup>2</sup>)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

**Features**

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Electrically Isolated
- Ceramic Package
- Light Weight
- Surface Mount
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

**Absolute Maximum Ratings**

**Pre-Irradiation**

Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 25°C	Continuous Drain Current	56*	A
I <sub>D2</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 100°C	Continuous Drain Current	40	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	224	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	268	mJ
I <sub>AR</sub>	Avalanche Current ①	56	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

\* Current is limited by package

For Footnotes, refer to the page 2.

**Electrical Characteristics @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.19	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.028	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 40A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-10.7	—	mV/°C	
g <sub>fs</sub>	Forward Transconductance	40	—	—	S	V <sub>DS</sub> = 15V, I <sub>D2</sub> = 40A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	10	μA	V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V
		—	—	25		V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>G</sub>	Total Gate Charge	—	—	240	nC	I <sub>D1</sub> = 56A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	70		V <sub>DS</sub> = 100V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	60		V <sub>GS</sub> = 12V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	50	ns	V <sub>DD</sub> = 100V
t <sub>r</sub>	Rise Time	—	—	150		I <sub>D1</sub> = 56A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	100		R <sub>G</sub> = 2.35Ω
t <sub>f</sub>	Fall Time	—	—	50		V <sub>GS</sub> = 12V
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	2.8	—	nH	Measured from center of Drain pad to center of Source pad
C <sub>iss</sub>	Input Capacitance	—	8120	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	949	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	13	—		f = 1.0MHz
R <sub>G</sub>	Gate Resistance	—	1.1	—	Ω	f = 1.0MHz, open drain

**Source-Drain Diode Ratings and Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	56*	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	224		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 56A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	640	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 56A, V <sub>DD</sub> ≤ 25V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	11.7	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

\* Current is limited by package

**Thermal Resistance**

Symbol	Parameter	Min.	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	—	0.5	°C/W
R <sub>θJ-PCB</sub>	Junction-to-PC Board (Soldered to 2" sq copper clad board)	—	1.6	—	

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 0.17mH, Peak I<sub>L</sub> = 56A, V<sub>GS</sub> = 12V
- ③ I<sub>SD</sub> ≤ 56A, di/dt ≤ 875A/μs, V<sub>DD</sub> ≤ 200V, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V<sub>GS</sub> Bias. 12 volt V<sub>GS</sub> applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V<sub>DS</sub> Bias. 160 volt V<sub>DS</sub> applied and V<sub>GS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

### Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

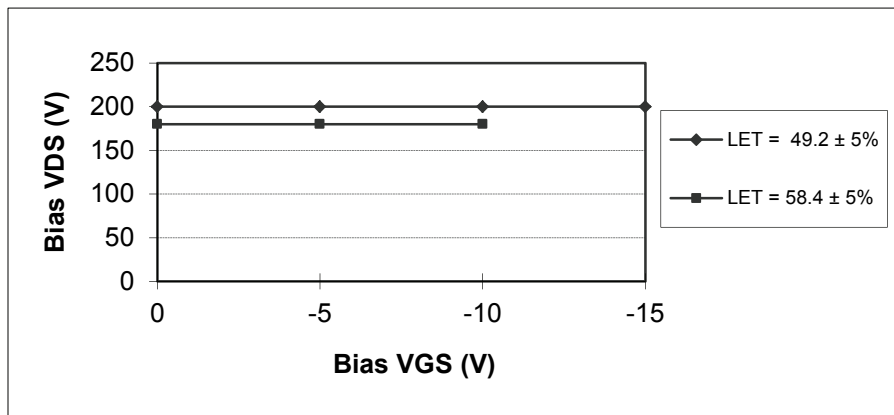
Symbol	Parameter	Up to 300 kRads (Si) <sup>1</sup>		Units	Test Conditions
		Min.	Max.		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	10	μA	V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source <sup>④</sup> On-State Resistance (TO-3)	—	0.029	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 40A
R <sub>DS(on)</sub>	Static Drain-to-Source <sup>④</sup> On-State Resistance (SMD-2)	—	0.028	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 40A
V <sub>SD</sub>	Diode Forward Voltage <sup>④</sup>	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 56A

1. Part numbers IRHNA6S7260 and IRHNA6S3260

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

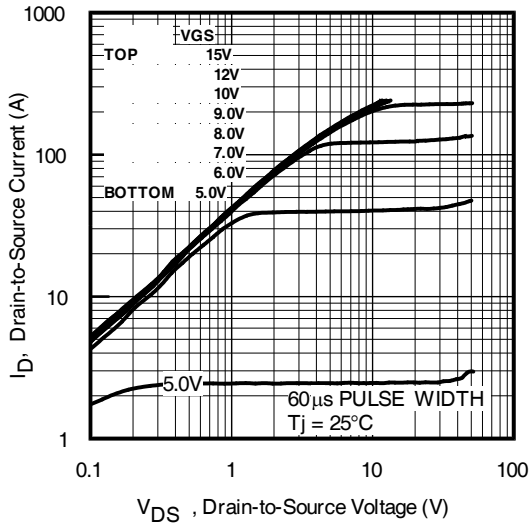
**Table 2. Typical Single Event Effect Safe Operating Area**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)			
			@ VGS = 0V	@ VGS = -5V	@ VGS = -10V	@ VGS = -15V
49.2 ± 5%	719 ± 5%	64.2 ± 5%	200	200	200	200
58.4 ± 5%	876 ± 5%	69.7 ± 7.5%	180	180	180	—

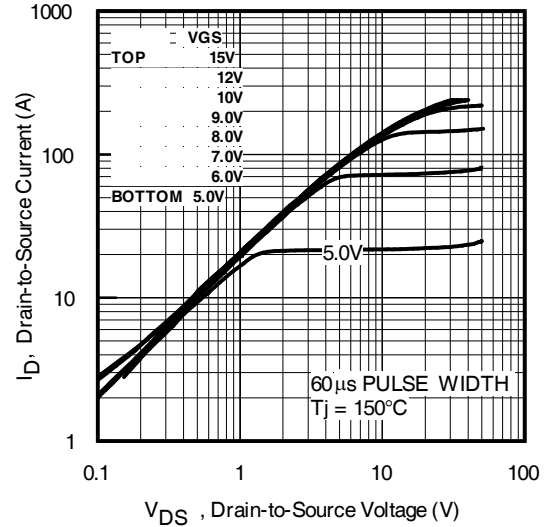


**Fig a.** Typical Single Event Effect, Safe Operating Area

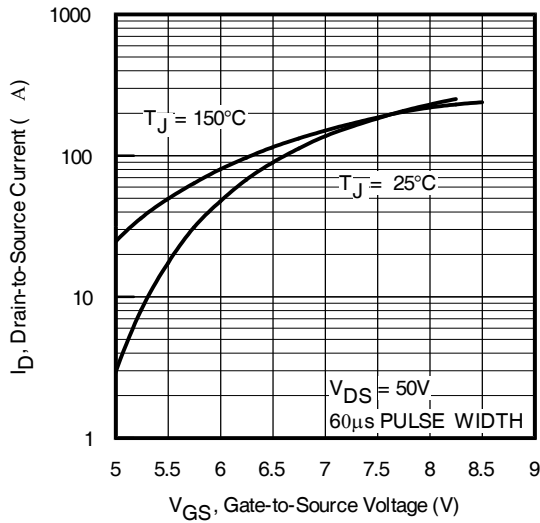
For Footnotes, refer to the page 2.



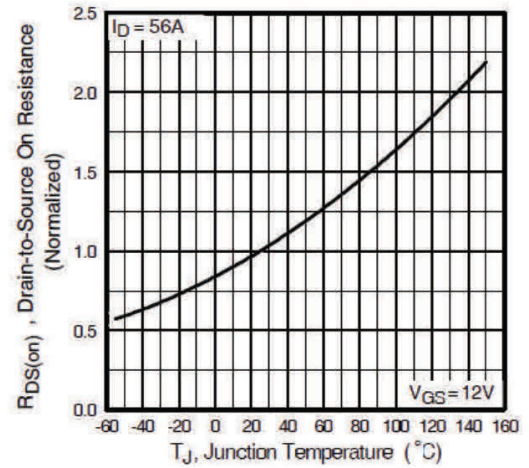
**Fig 1. Typical Output Characteristics**



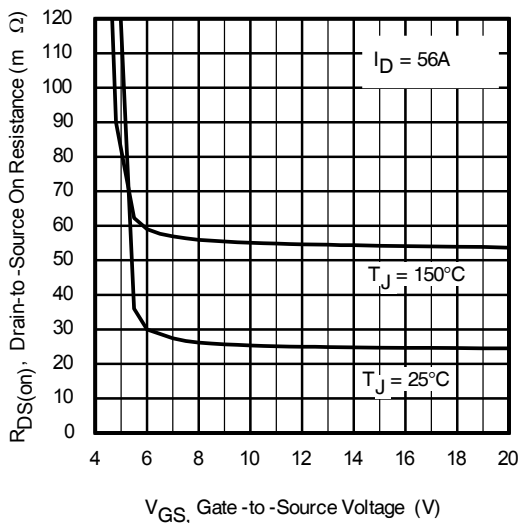
**Fig 2. Typical Output Characteristics**



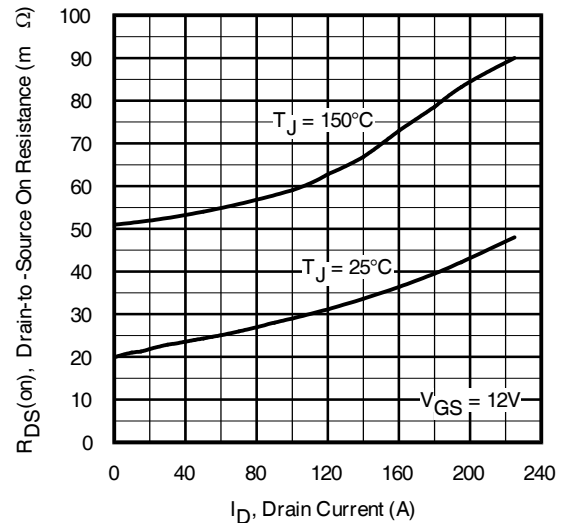
**Fig 3. Typical Transfer Characteristics**



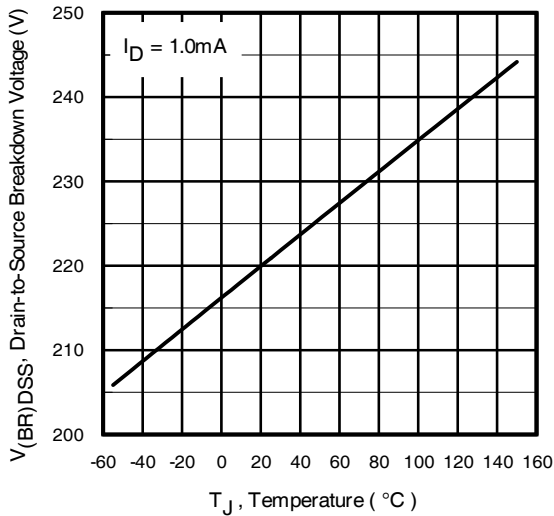
**Fig 4. Normalized On-Resistance Vs. Temperature**



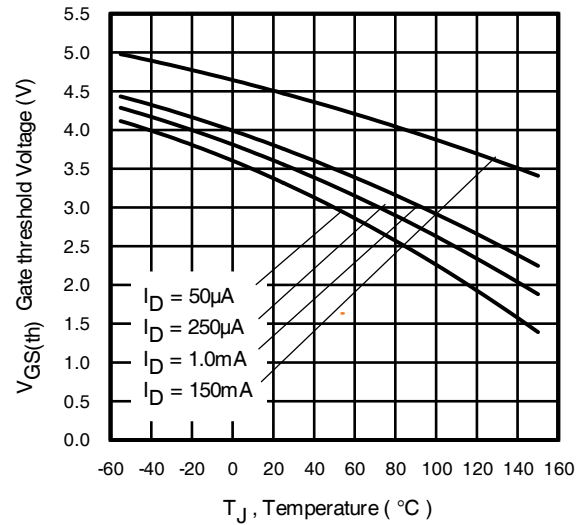
**Fig 5. Typical On-Resistance Vs Gate Voltage**



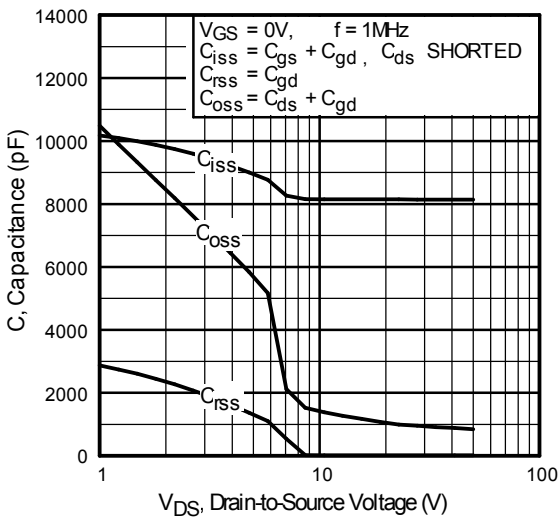
**Fig 6. Typical On-Resistance Vs Drain Current**



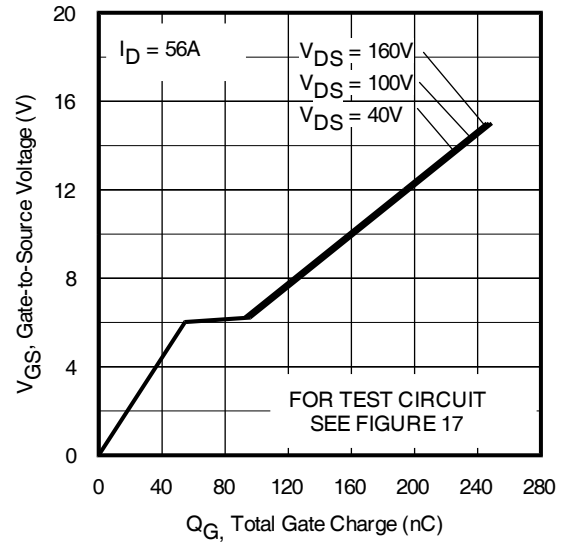
**Fig 7.** Typical Drain-to-Source Breakdown Voltage Vs Temperature



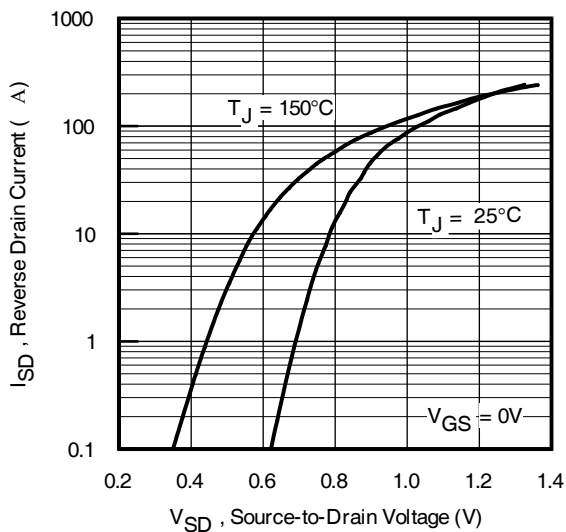
**Fig 8.** Typical Threshold Voltage Vs Temperature



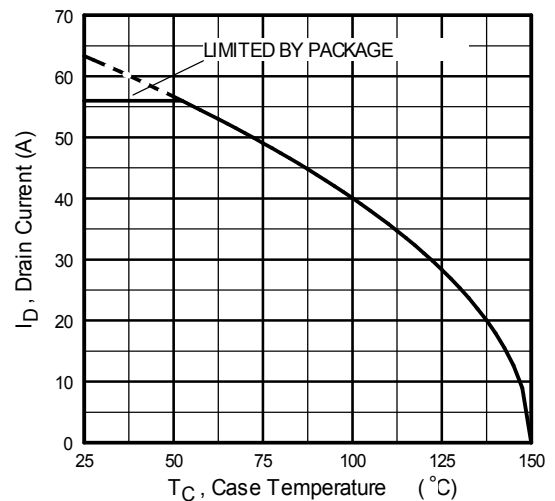
**Fig 9.** Typical Capacitance Vs. Drain-to-Source Voltage



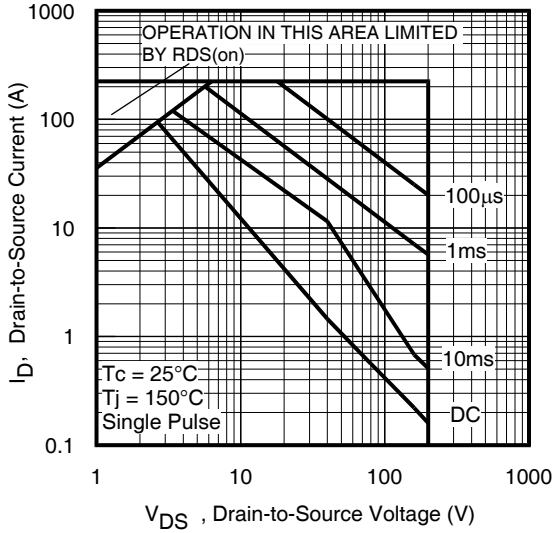
**Fig 10.** Typical Gate Charge Vs. Gate-to-Source Voltage



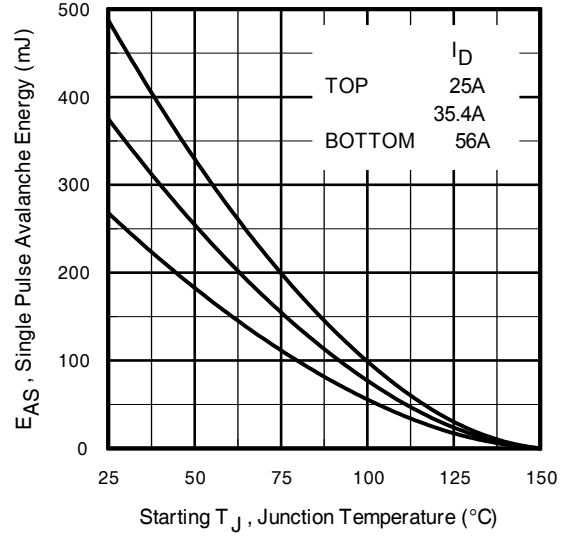
**Fig 11.** Typical Source-Drain Diode Forward Voltage



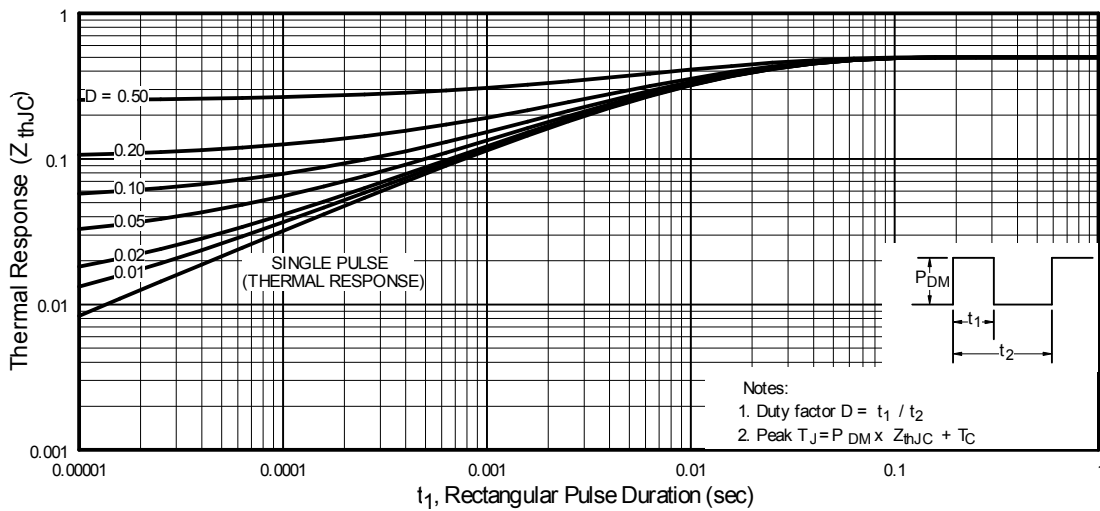
**Fig 12.** Maximum Drain Current Vs. Case Temperature



**Fig 13.** Maximum Safe Operating Area

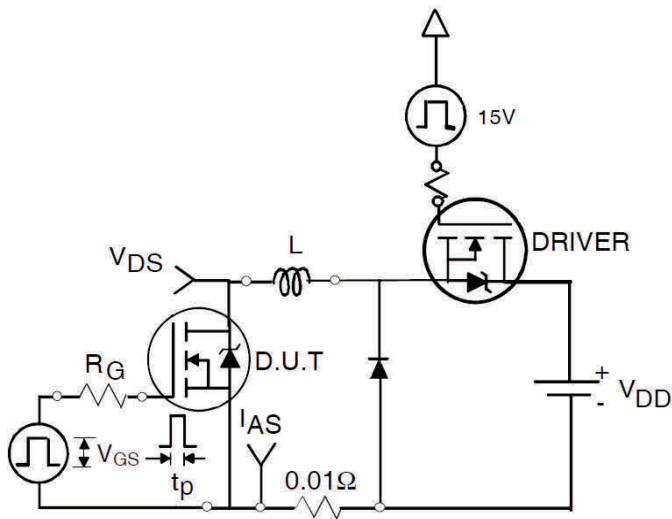


**Fig 14.** Maximum Avalanche Energy Vs. Drain Current

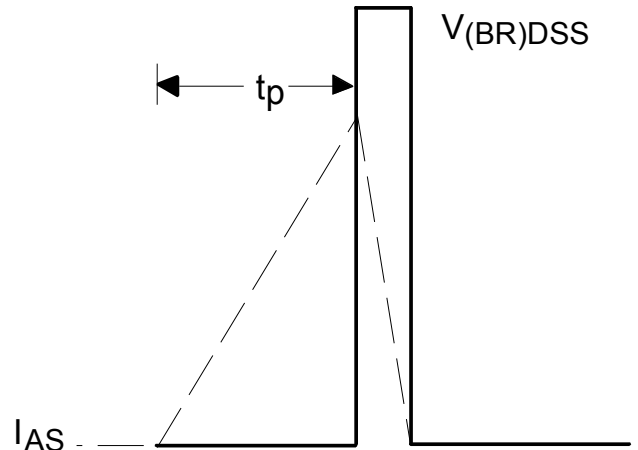


**Fig 15.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

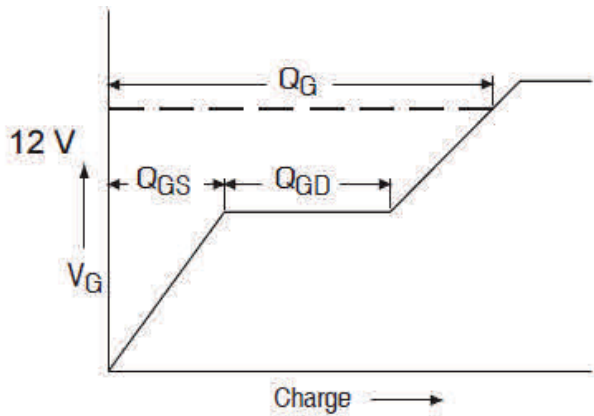
**Pre-Irradiation**



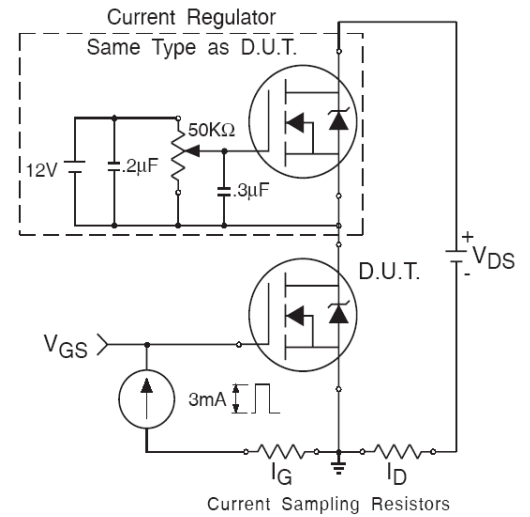
**Fig 16a.** Unclamped Inductive Test Circuit



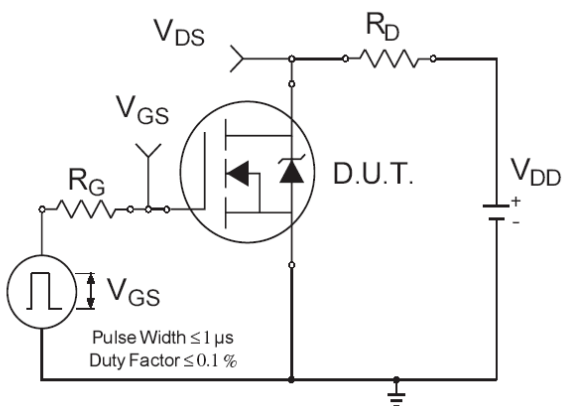
**Fig 16b.** Unclamped Inductive Waveforms



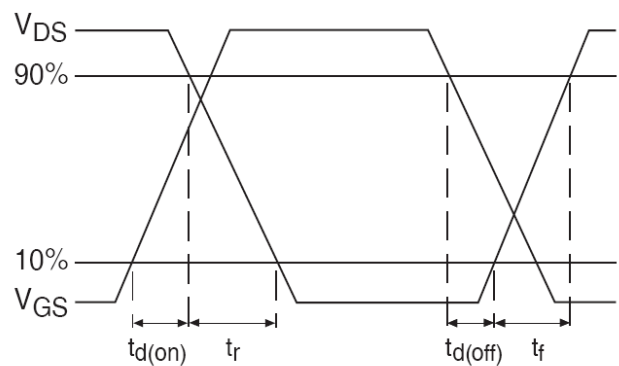
**Fig 17a.** Gate Charge Waveform



**Fig 17b.** Gate Charge Test Circuit

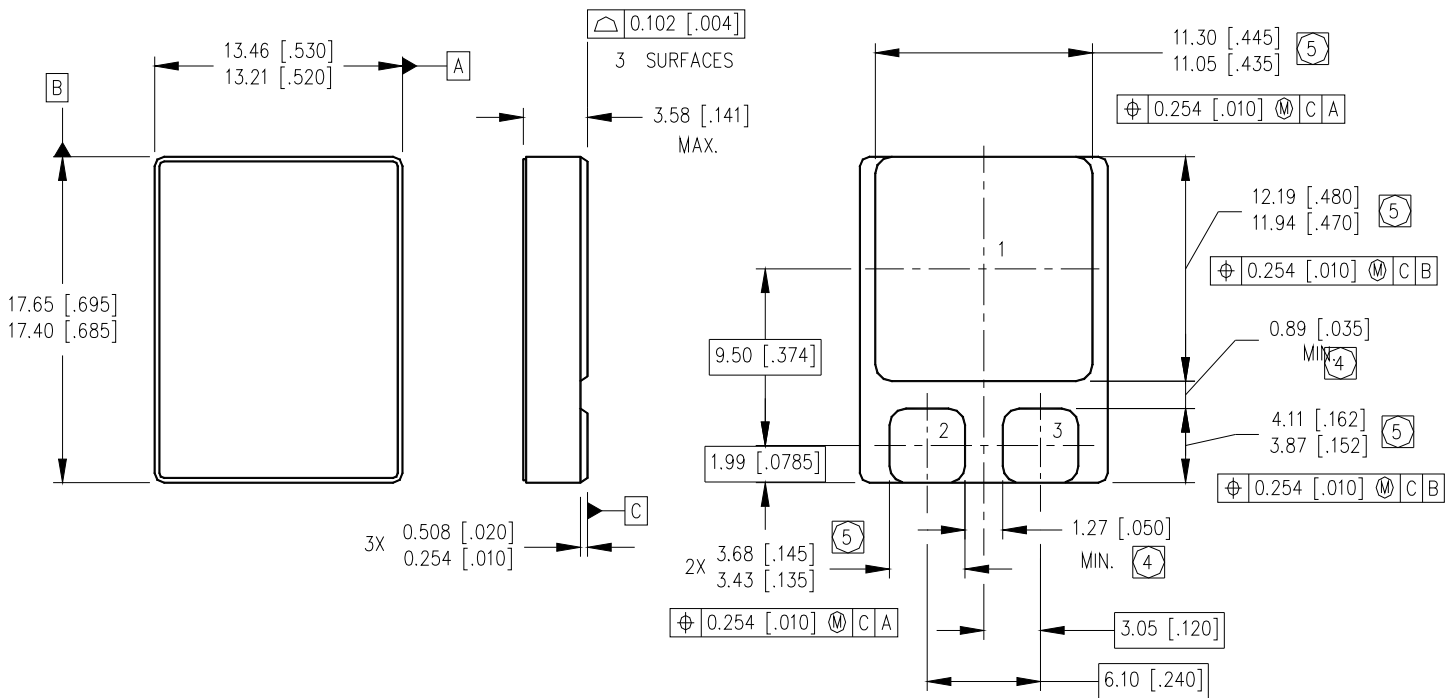


**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms

**Case Outline and Dimensions — SMD-2**



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSION INCLUDES METALLIZATION FLASH.
5. DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

**PAD ASSIGNMENTS**

MOSFET	
1	= DRAIN
2	= GATE
3	= SOURCE



### **IMPORTANT NOTICE**

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