

# IRHNA67264 (JANSR2N7585U2)

PD-96990E

## Radiation Hardened Power MOSFET Surface Mount (SMD-2) 250V, 50A, N-channel, R6 Technology

### Features

- Single event effect (SEE) hardened (up to LET of 85 MeV·cm<sup>2</sup>/mg)
- Low R<sub>DS(on)</sub>
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Light weight
- Surface mount
- ESD rating: Class 3A per MIL-STD-750, Method 1020

### Potential Applications

- DC-DC converter
- Motor drives

### Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications

### Description

IR HiRel R6 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 85 MeV·cm<sup>2</sup>/mg. Their combination of low R<sub>DS(on)</sub> and fast switching times will allow for better performance in applications such as DC-DC converters or motor drives. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

### Ordering Information

**Table 1** Ordering options

Part number	Package	Screening Level	TID Level
IRHNA67264	SMD-2	COTS	100 krad (Si)
IRHNA67264SCS	SMD-2	S-Level	100 krad (Si)
JANSR2N7585U2	SMD-2	JANS	100 krad (Si)
IRHNA63264	SMD-2	COTS	300 krad (Si)
JANSF2N7585U2	SMD-2	JANS	300 krad (Si)

### Product Summary

- **Part number:** IRHNA67264 (JANSR2N7585U2), IRHNA63264 (JANSR2N7585U2)
- **REF:** MIL-PRF-19500/760
- **Radiation level:** 100 krad (Si), 300 krad (Si)
- **R<sub>DS(on), max</sub>:** 40mΩ

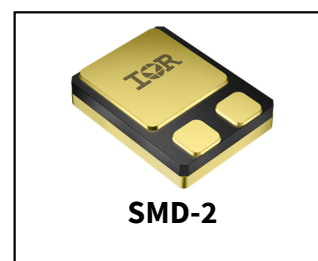


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**Absolute Maximum Ratings**

**1 Absolute Maximum Ratings**

**Table 2 Absolute Maximum Ratings (Pre-Irradiation)**

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 12V, T_C = 25^\circ C$	Continuous Drain Current	50	A
$I_{D2} @ V_{GS} = 12V, T_C = 100^\circ C$	Continuous Drain Current	31.5	A
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current <sup>1</sup>	200	A
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>2</sup>	240	mJ
$I_{AR}$	Avalanche Current <sup>1</sup>	50	A
$E_{AR}$	Repetitive Avalanche Energy <sup>1</sup>	25	mJ
dv/dt	Peak Diode Reverse Recovery <sup>3</sup>	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 ( for 5s)	
	Weight	3.3 (Typical)	

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup>  $V_{DD} = 50V$ , starting  $T_J = 25^\circ C$ ,  $L = 0.19mH$ , Peak  $I_L = 50A$ ,  $V_{GS} = 12V$

<sup>3</sup>  $I_{SD} \leq 50A$ ,  $di/dt \leq 900A/\mu s$ ,  $V_{DD} \leq 250V$ ,  $T_J \leq 150^\circ C$

**Device Characteristics**

**2 Device Characteristics**

**2.1 Electrical Characteristics (Pre-Irradiation)**

**Table 3 Static and Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	250	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.3	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	40	mΩ	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 31.5A <sup>1</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1mA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-10.1	—	mV/°C	
G <sub>fs</sub>	Forward Transconductance	37	—	—	S	V <sub>DS</sub> = 15V, I <sub>D2</sub> = 31.5A <sup>1</sup>
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	10	μA	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V
		—	—	25		V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>G</sub>	Total Gate Charge	—	—	220	nC	I <sub>D1</sub> = 50A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	50		V <sub>DS</sub> = 125V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	70		V <sub>GS</sub> = 12V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	50	ns	I <sub>D1</sub> = 50A ** V <sub>DD</sub> = 125V R <sub>G</sub> = 2.35Ω V <sub>GS</sub> = 12V
t <sub>r</sub>	Rise Time	—	—	150		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	100		
t <sub>f</sub>	Fall Time	—	—	50		
L <sub>s</sub> + L <sub>D</sub>	Total Inductance	—	2.8	—	nH	Measured from center of Drain pad to center of Source pad
C <sub>iss</sub>	Input Capacitance	—	6912	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>OSS</sub>	Output Capacitance	—	940	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	10.8	—		
R <sub>G</sub>	Gate Resistance	—	0.52	—	Ω	f = 1.0MHz, open drain

\*\* Switching speed maximum limits are based on manufacturing test equipment and capability.

<sup>1</sup> Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

**Device Characteristics**

**2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)**

**Table 4 Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	50	A	
$I_{SM}$	Pulsed Source Current (Body Diode) <sup>1</sup>	—	—	200	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$ , $I_S = 50\text{A}$ , $V_{GS} = 0\text{V}$ <sup>2</sup>
$t_{rr}$	Reverse Recovery Time	—	—	700	ns	$T_J = 25^\circ\text{C}$ , $I_F = 50\text{A}$ , $V_{DD} \leq 25\text{V}$ $di/dt = 100\text{A}/\mu\text{s}$ <sup>2</sup>
$Q_{rr}$	Reverse Recovery Charge	—	—	15	$\mu\text{C}$	
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

**2.3 Thermal Characteristics**

**Table 5 Thermal Resistance**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta J-PCB}$	Junction-to-PC Board (Soldered to 2" sq copper clad board)	—	1.6	—	

**2.4 Radiation Characteristics**

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**2.4.1 Electrical Characteristics — Post Total Dose Irradiation**

**Table 6 Electrical Characteristics @  $T_J = 25^\circ\text{C}$ , Post Total Dose Irradiation<sup>3, 4</sup>**

Symbol	Parameter	Up to 300 krad (Si) <sup>5</sup>		Unit	Test Conditions
		Min.	Max.		
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	250	—	V	$V_{GS} = 0\text{V}$ , $I_D = 1.0\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	$V_{DS} = V_{GS}$ , $I_D = 1.0\text{mA}$
$I_{GSS}$	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -20\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current	—	10	$\mu\text{A}$	$V_{DS} = 200\text{V}$ , $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) <sup>2</sup>	—	41	$\text{m}\Omega$	$V_{GS} = 12\text{V}$ , $I_{D2} = 31.5\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-2) <sup>2</sup>	—	40	$\text{m}\Omega$	$V_{GS} = 12\text{V}$ , $I_{D2} = 31.5\text{A}$
$V_{SD}$	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0\text{V}$ , $I_F = 50\text{A}$

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup> Pulse width  $\leq 300 \mu\text{s}$ ; Duty Cycle  $\leq 2\%$

<sup>3</sup> Total Dose Irradiation with  $V_{GS}$  Bias.  $V_{GS} = 12\text{V}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

<sup>4</sup> Total Dose Irradiation with  $V_{DS}$  Bias.  $V_{DS} = 200\text{V}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

<sup>5</sup> Part numbers IRHNA67264 (JANSR2N7585U2) and IRHNA63264 (JANSR2F7585U2)

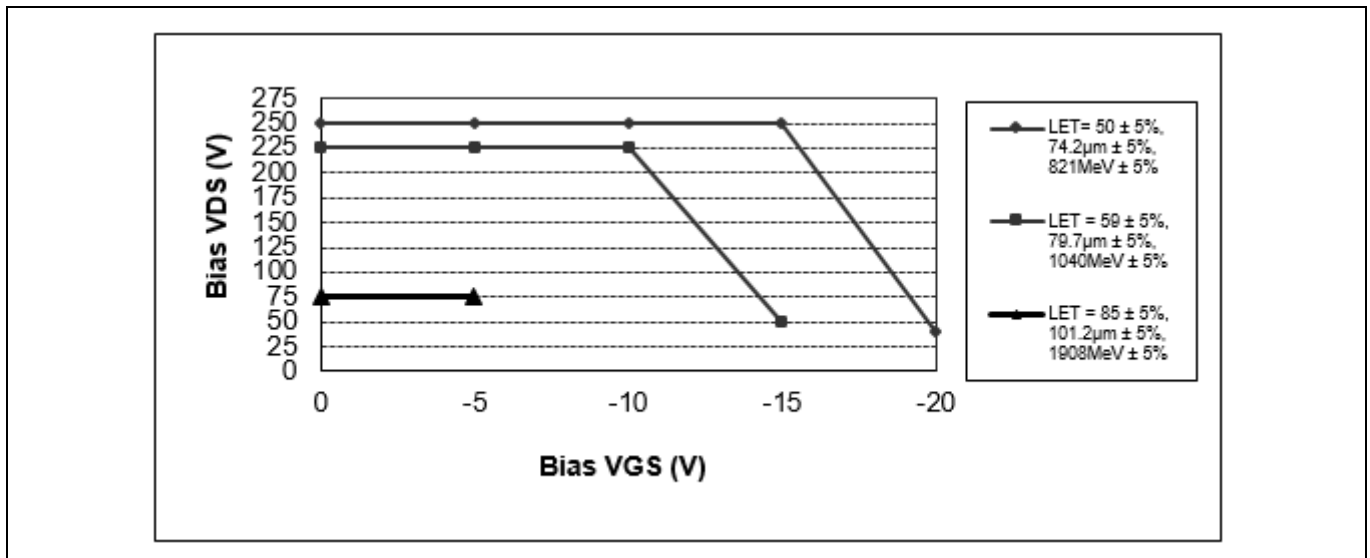
**Device Characteristics**

**2.4.2 Single Event Effects — Safe Operating Area**

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

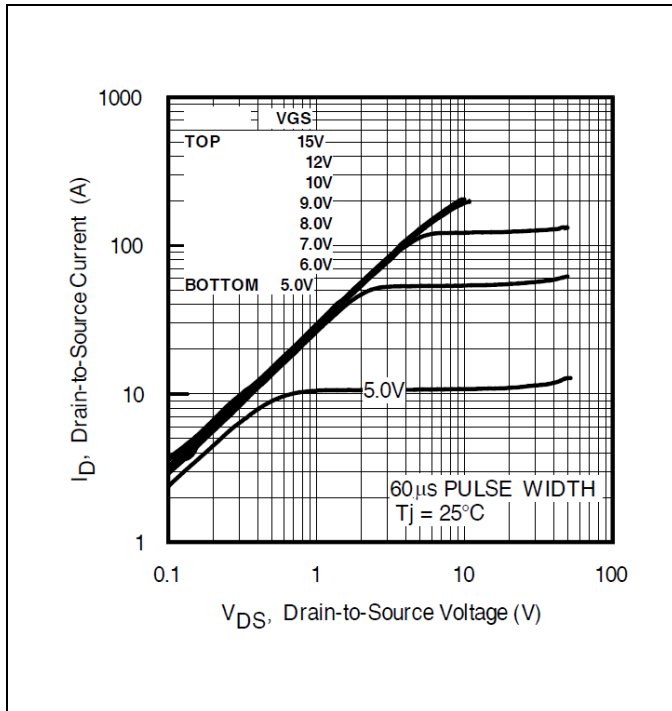
**Table 7 Typical Single Event Effects Safe Operating Area**

LET (MeV·cm <sup>2</sup> /mg)	Energy (MeV)	Range (μm)	V <sub>DS</sub> (V)				
			V <sub>GS</sub> = 0V	V <sub>GS</sub> = -5V	V <sub>GS</sub> = -10V	V <sub>GS</sub> = -15V	V <sub>GS</sub> = -20V
50 ± 5%	821 ± 5%	74.2 ± 5%	250	250	250	250	40
59 ± 5%	1040 ± 5%	79.7 ± 5%	225	225	225	50	—
85 ± 5%	1908 ± 5%	101.2 ± 5%	75	75	—	—	—

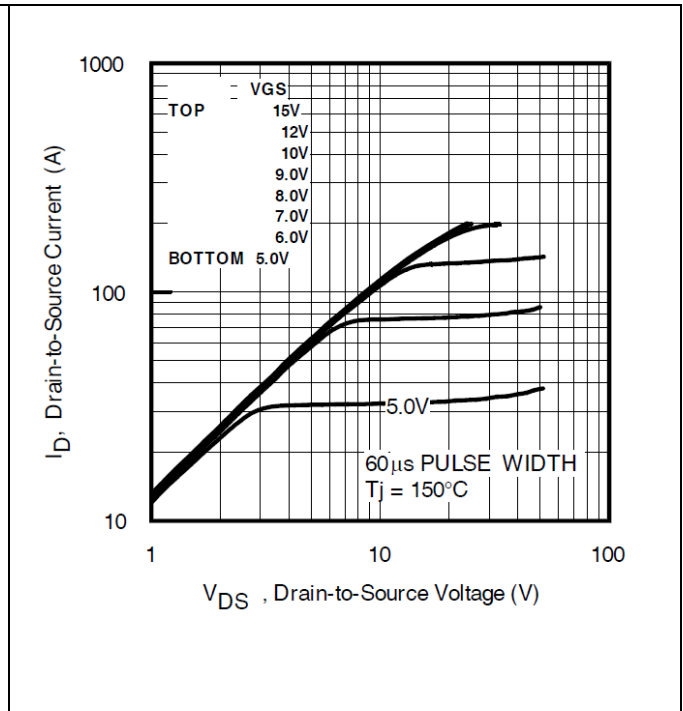


**Figure 1 Typical Single Event Effect, Safe Operating Area**

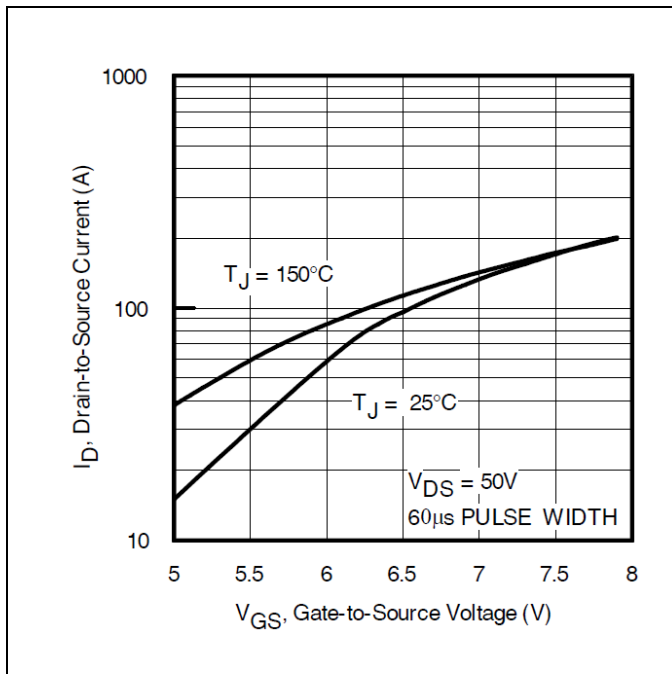
### 3 Electrical Characteristics Curves (Pre-irradiation)



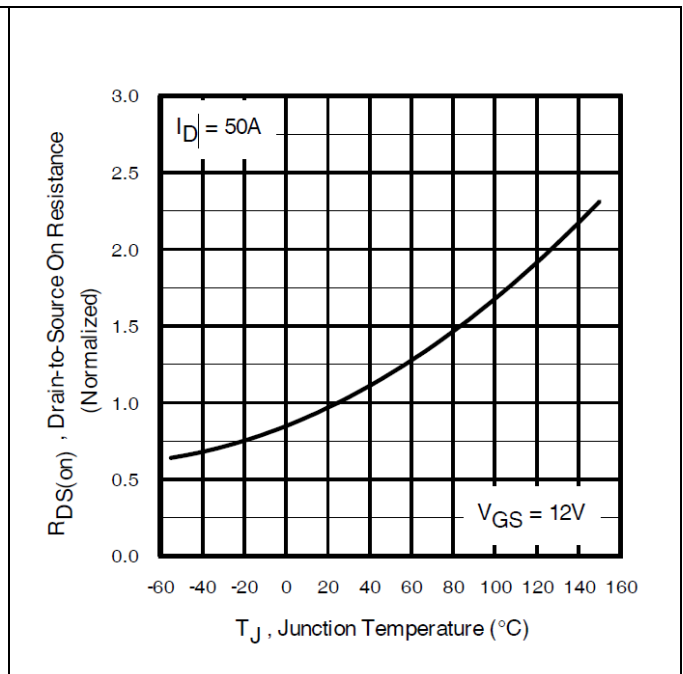
**Figure 2 Typical Output Characteristics**



**Figure 3 Typical Output Characteristics**

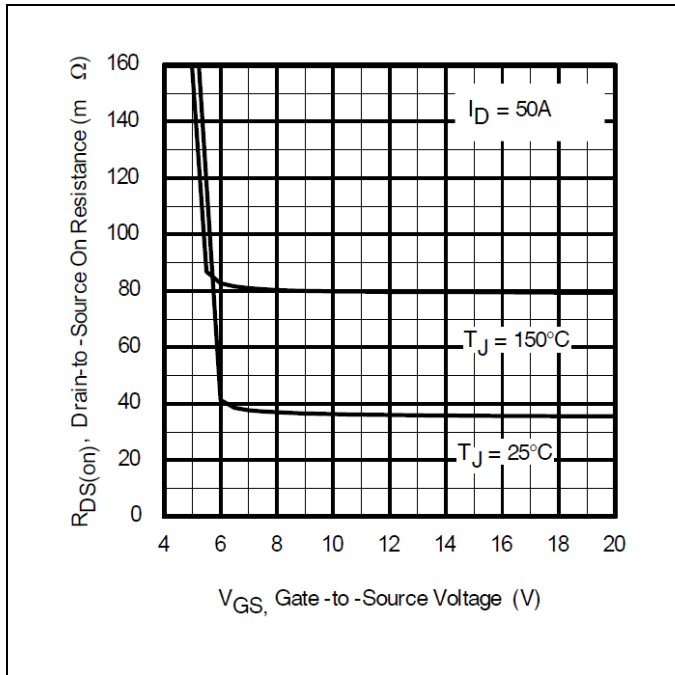


**Figure 4 Typical Transfer Characteristics**

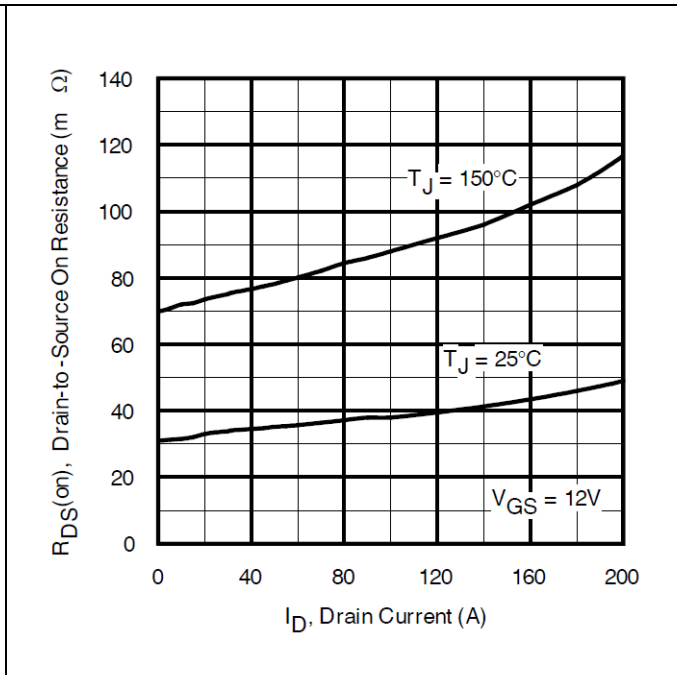


**Figure 5 Normalized On-Resistance Vs. Temperature**

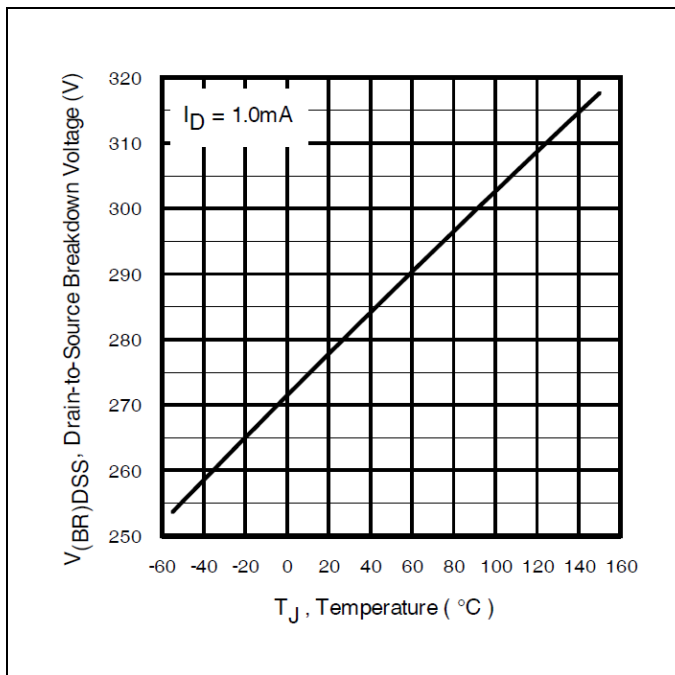
**IRHNA67264 (JANSR2N7585U2)**  
**Radiation Hardened Power MOSFET (SMD-2)**  
**Electrical Characteristics Curves (Pre-irradiation)**



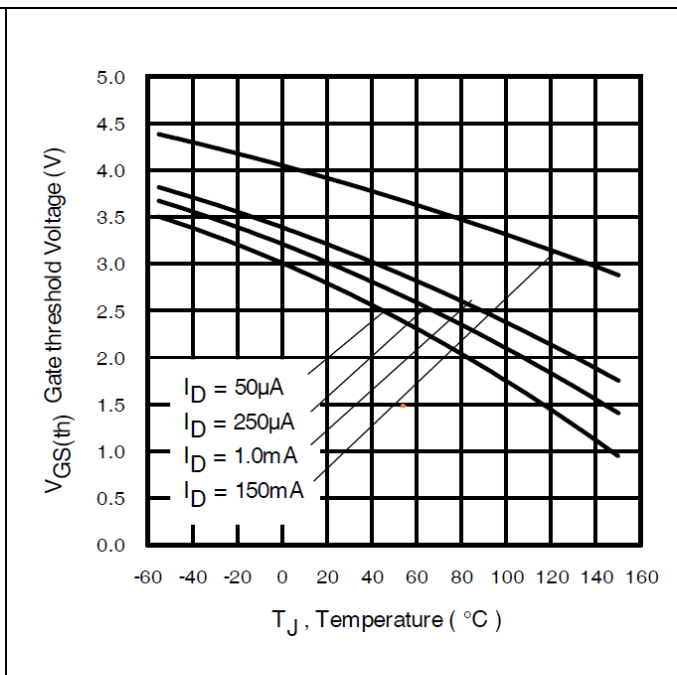
**Figure 6 Typical On-Resistance Vs Gate Voltage**



**Figure 7 Typical On-Resistance Vs Drain Current**



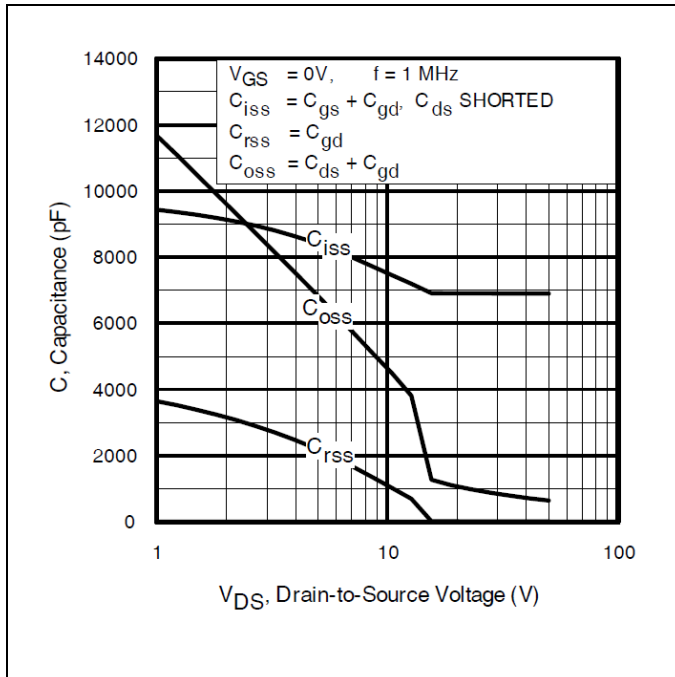
**Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature**



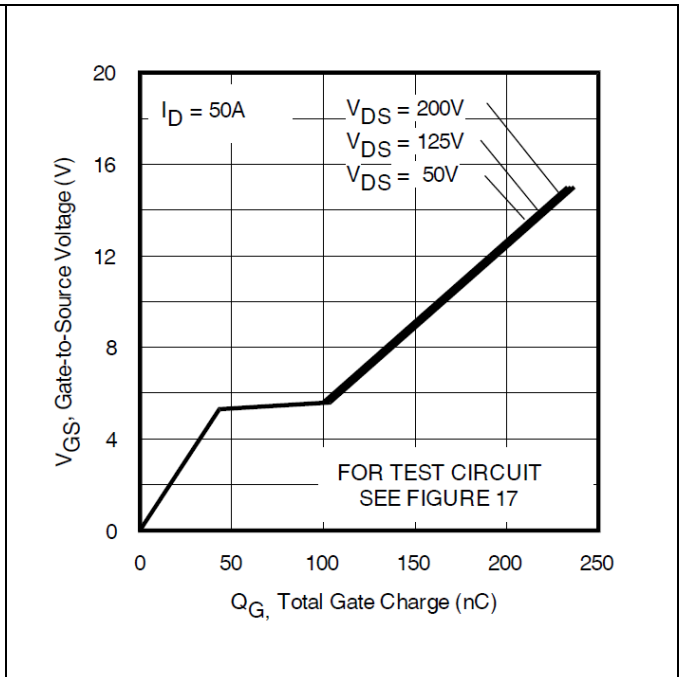
**Figure 9 Typical Gate-to-Source Voltage Vs. Temperature**



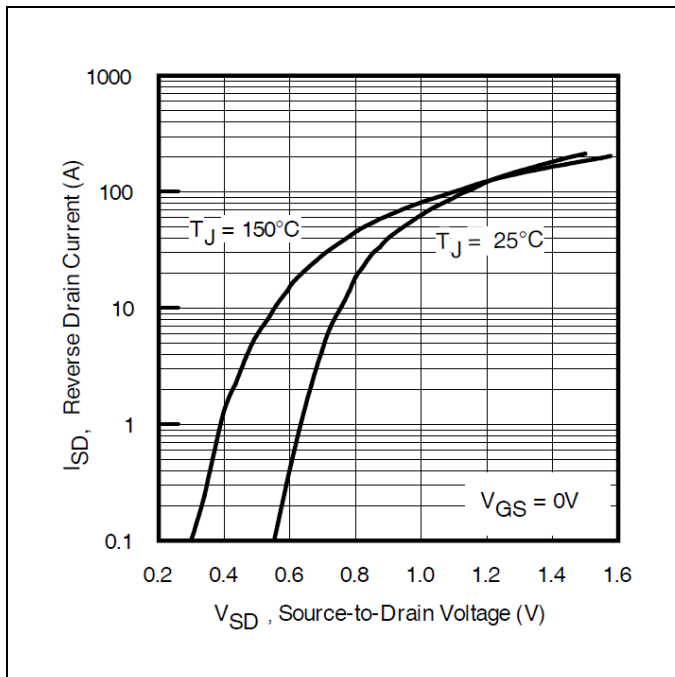
**IRHNA67264 (JANSR2N7585U2)**  
**Radiation Hardened Power MOSFET (SMD-2)**  
**Electrical Characteristics Curves (Pre-irradiation)**



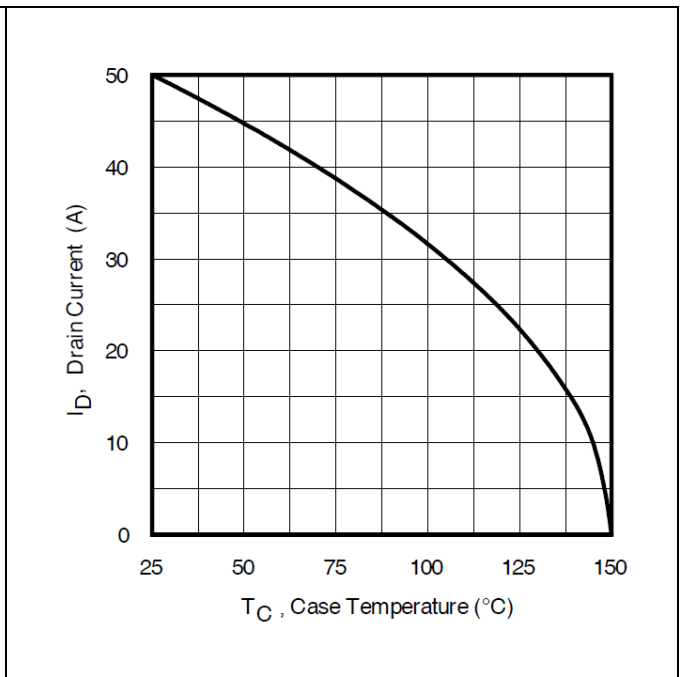
**Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage**



**Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge**

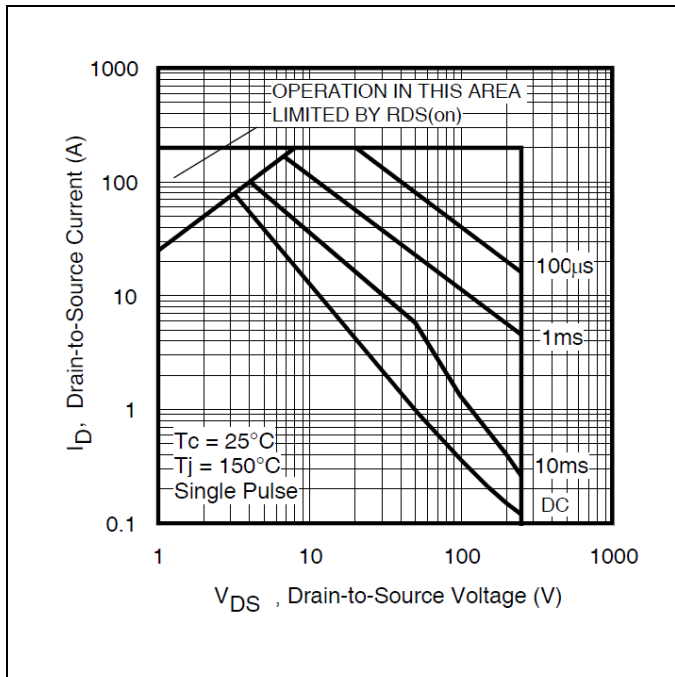


**Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage**

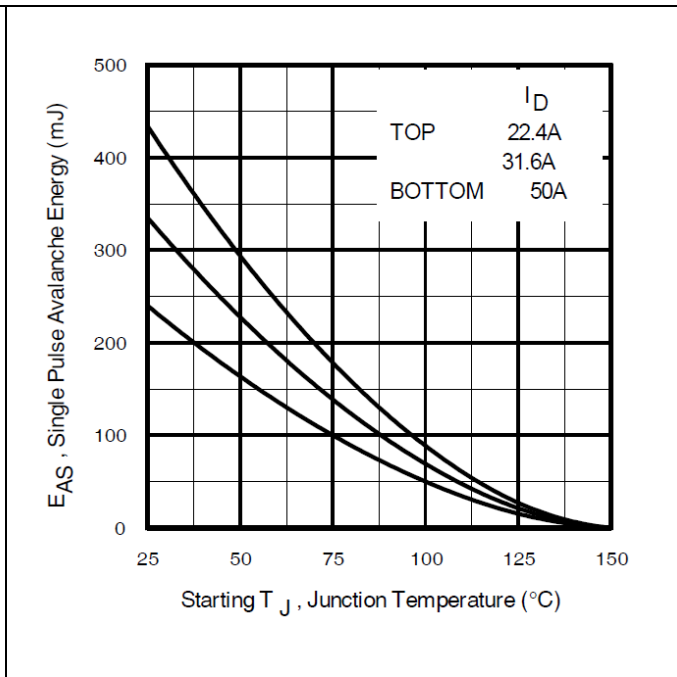


**Figure 13 Maximum Drain Current Vs. Temperature**

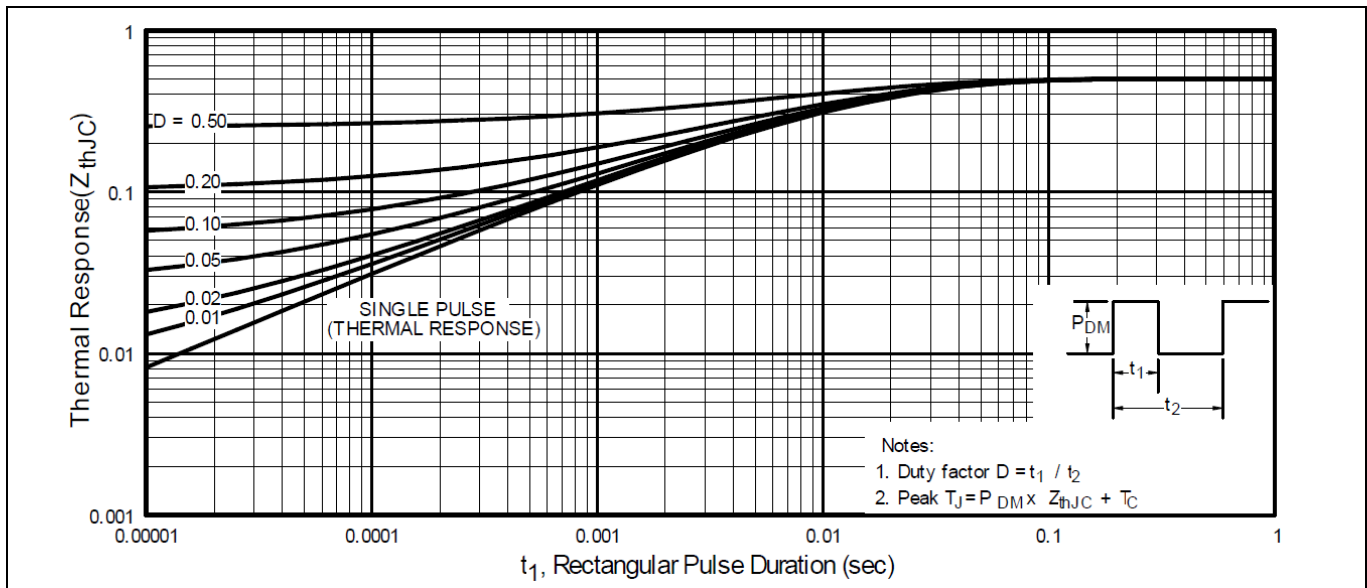
**IRHNA67264 (JANSR2N7585U2)**  
**Radiation Hardened Power MOSFET (SMD-2)**  
**Electrical Characteristics Curves (Pre-irradiation)**



**Figure 14 Maximum Safe Operating Area**



**Figure 15 Maximum Avalanche Energy Vs. Junction Temperature**

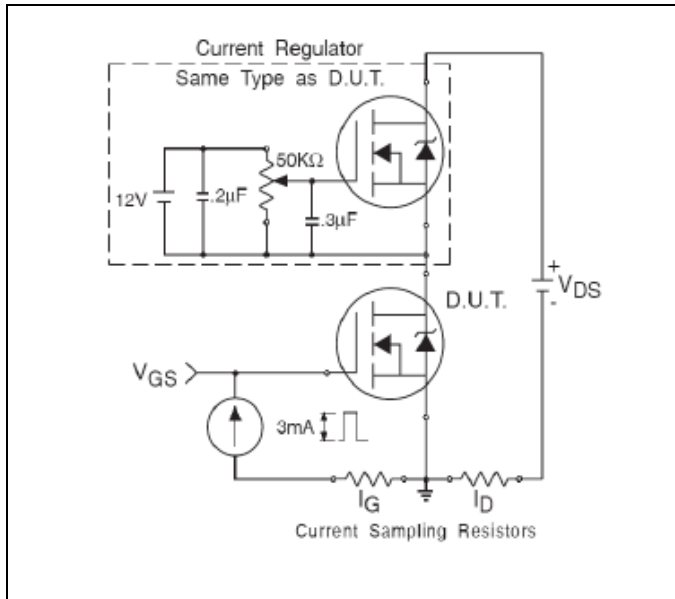


**Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case**

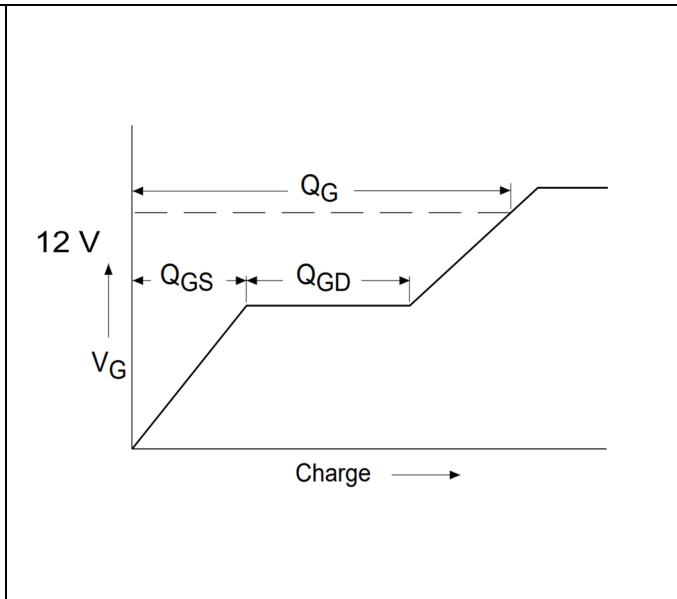
**IRHNA67264 (JANSR2N7585U2)**  
**Radiation Hardened Power MOSFET (SMD-2)**

**Test Circuits (Pre-irradiation)**

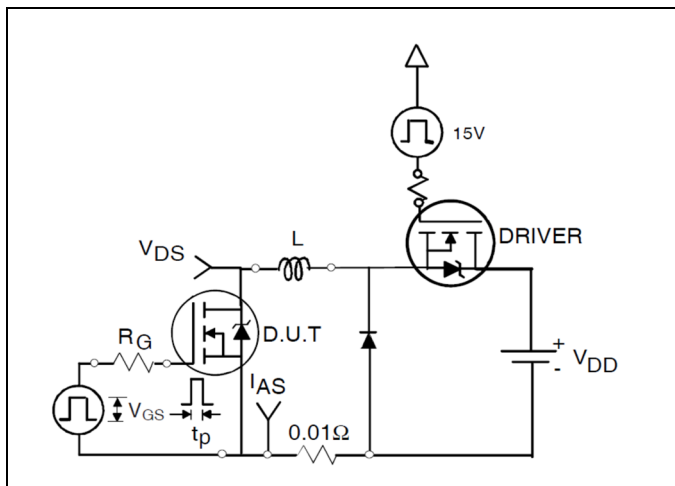
**4 Test Circuits (Pre-irradiation)**



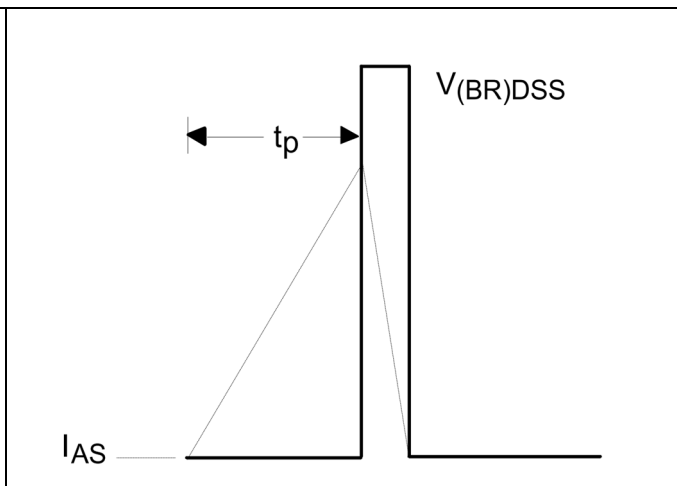
**Figure 17 Gate Charge Test Circuit**



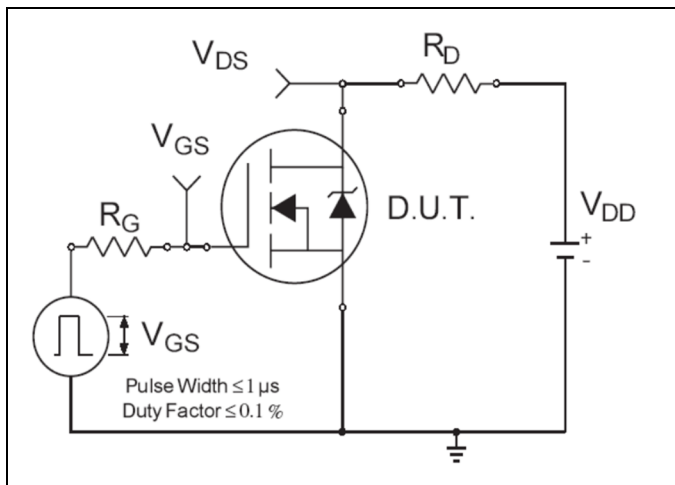
**Figure 18 Gate Charge Waveform**



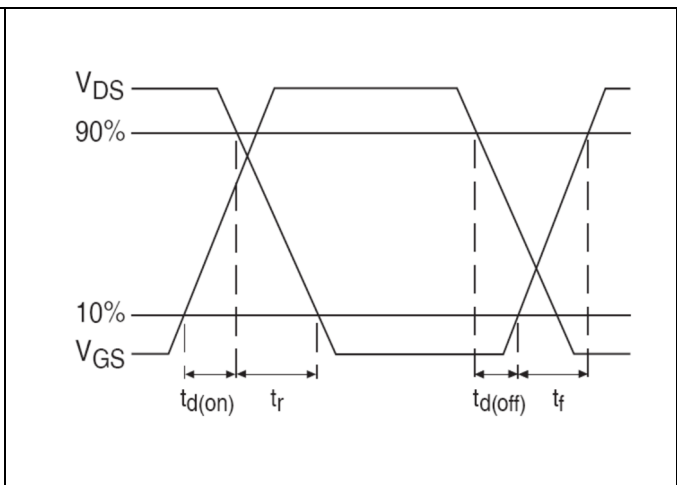
**Figure 19 Unclamped Inductive Test Circuit**



**Figure 20 Unclamped Inductive Waveform**



**Figure 21 Switching Time Test Circuit**

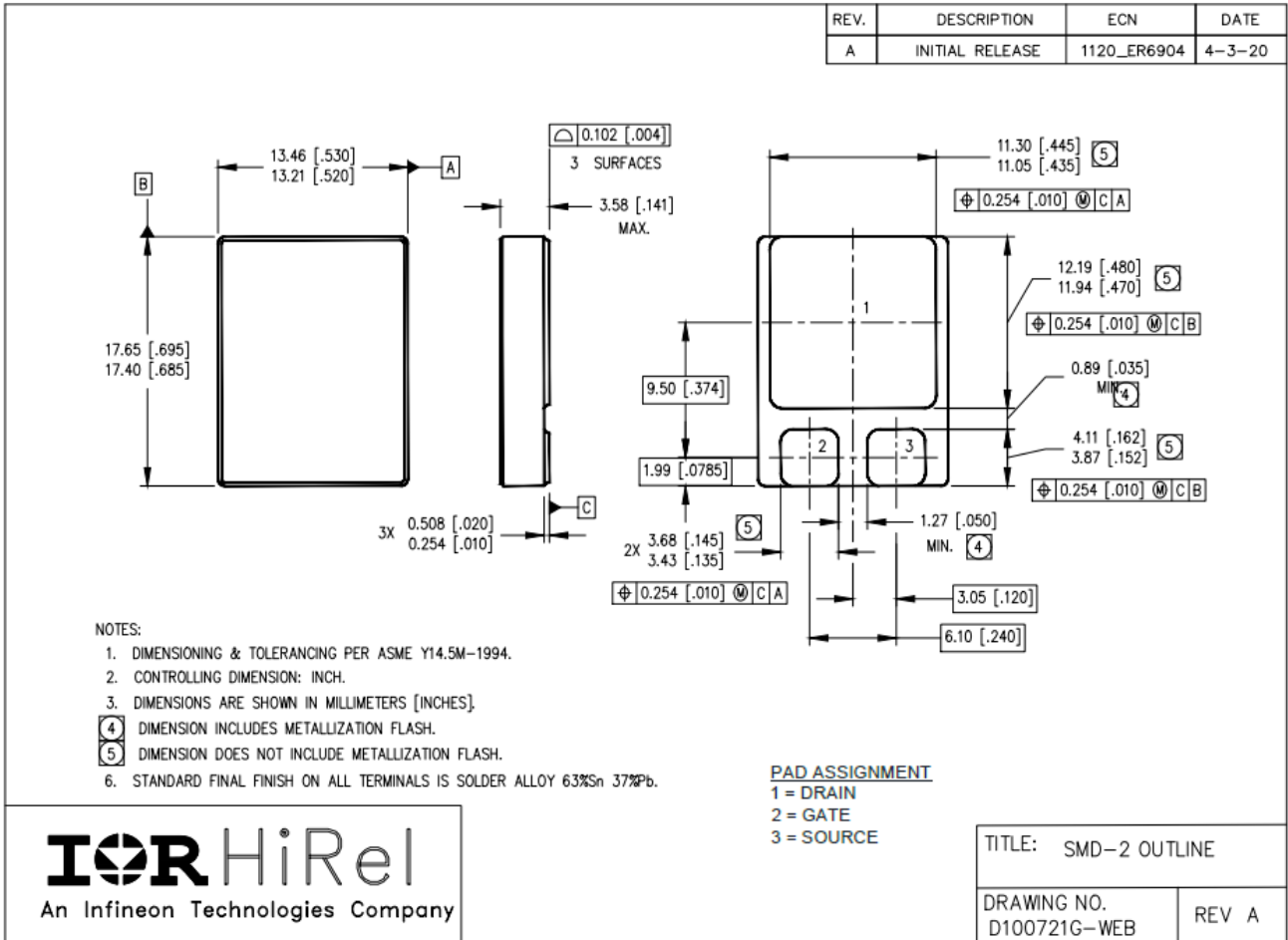


**Figure 22 Switching Time Waveforms**

**Package Outline**

**5 Package Outline**

**Note: For the most updated package outline, please see the website: [SMD-2](#)**



**IRHNA67264 (JANSR2N7585U2)**  
**Radiation Hardened Power MOSFET (SMD-2)**

**Revision history**

**Revision history**

<b>Document version</b>	<b>Date of release</b>	<b>Description of changes</b>
	06/28/2005	Final datasheet with PD number (PD-96990)
Rev A	12/22/2011	Updated based on ECN-18135
Rev B	04/28/2017	Updated based on ECN-1120_05333
Rev C	10/30/2018	Updated based on ECN-1120_06367-3
Rev D	11/09/2020	Updated based on ECN-1120_08235
Rev E	03/07/2022	Updated based on ECN-1120_08906

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