

IRHNA57163SE JANSR2N7472U2

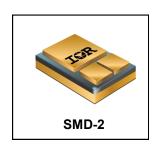
RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SMD-2)

130V, N-CHANNEL REF: MIL-PRF-19500/684

\$\mathcal{Z}_5\text{TECHNOLOGY}\$

Product Summary

Part Number	Radiation Level	RDS(on)	Ι _D	QPL Part Number
IRHNA57163SE	100 kRads(Si)	0.0135Ω	75A*	JANSR2N7472U2



Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- · Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	75*	
I _{D2} @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	57	A
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	300	
P _D @ T _C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	280	mJ
I _{AR}	Avalanche Current ①	75	Α
E _{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T _J	Operating Junction and	-55 to + 150	
T _{STG}	Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

For Footnotes, refer to the page 2.



Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	130			V	$V_{GS} = 0V, I_{D} = 1.0mA$
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.17		V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance			0.0135	Ω	V _{GS} = 12V, I _{D2} = 57A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.5		4.5	V	$V_{DS} = V_{GS}$, $I_D = 1.0 \text{mA}$
Gfs	Forward Transconductance	39			S	V _{DS} = 15V, I _{D2} = 57A ④
I _{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{DS} = 104V, V_{GS} = 0V$
	Zero Gate Voltage Brain Gurrent			25	μΛ	$V_{DS} = 104V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I _{GSS}	Gate-to-Source Leakage Forward			100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse			-100	ПА	V _{GS} = -20V
Q_{G}	Total Gate Charge			160		I _{D1} = 75A
Q_GS	Gate-to-Source Charge			55	nC	V _{DS} = 65V
Q_GD	Gate-to-Drain ('Miller') Charge			75		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time			35		$V_{DD} = 65V$
tr	Rise Time			125	no	I _{D1} = 75A
$t_{d(off)}$	Turn-Off Delay Time			80	ns	$R_G = 2.35\Omega$
t _f	Fall Time			50		V _{GS} = 12V
Ls +L _D	Total Inductance		4.0		nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance		5020			V _{GS} = 0V
C _{oss}	Output Capacitance		1490		pF	V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance		116			f = 1.0 MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current (Body Diode)			75*	^	
I _{SM}	Pulsed Source Current (Body Diode) ①			300	Α	
V_{SD}	Diode Forward Voltage			1.2	V	$T_J = 25^{\circ}C, I_S = 75A, V_{GS} = 0V$
t _{rr}	Reverse Recovery Time			300	ns	$T_J = 25^{\circ}C, I_F = 75A, V_{DD} \le 50V$
Q _{rr}	Reverse Recovery Charge			4.1	μC	di/dt = 100A/µs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Thermal Resistance

Symbol	Parameter		Тур.	Max.	Units
$R_{ heta JC}$	Junction-to-Case			0.50	°C/W
$R_{\theta ext{-PCB}}$	Junction-to-PC Board (soldered to 1 inch square cu clad board)		1.6		C/VV

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- $^{\circ}$ V_{DD} = 50V, starting T_J = 25°C, L = 0.1mH, Peak I_L = 75A, V_{GS} = 12V
- $\exists \quad I_{SD} \leq 75A, \ di/dt \leq 280A/\mu s, \ V_{DD} \leq 130V, \ T_J \leq 150^{\circ}C$
- \circ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- © Total Dose Irradiation with V_{DS} Bias. 104volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.



Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation \$6

Symbol	Parameter	100 kRa	ds (Si)	Units	Test Conditions	
		Min.	Max.			
BV _{DSS}	Drain-to-Source Breakdown Voltage	130		V	$V_{GS} = 0V, I_{D} = 1.0mA$	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	$V_{DS} = V_{GS}$, $I_D = 1.0 \text{mA}$	
I _{GSS}	Gate-to-Source Leakage Forward		100	nA	V _{GS} = 20V	
I _{GSS}	Gate-to-Source Leakage Reverse		-100	nA	V _{GS} = -20V	
I _{DSS}	Zero Gate Voltage Drain Current		10	μA	V _{DS} = 104V, V _{GS} = 0V	
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)		0.014	Ω	V _{GS} = 12V, I _{D2} = 57A	
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (SMD-2)		0.0135	Ω	V _{GS} = 12V, I _{D2} = 57A	
V _{SD}	Diode Forward Voltage ④		1.2	V	V _{GS} = 0V, I _S = 75A	

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

					VDS (V)		
LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	@ VGS = 0V	@ VGS = -5V	@ VGS = -10V	@ VGS = -15V	@ VGS = -20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	130	130	130	130	130
61 ± 5%	330 ±7. 5%	31 ± 10%	130	130	130	100	50
84 ± 5%	350 ± 10%	28 ± 7.5%	130	120	30		

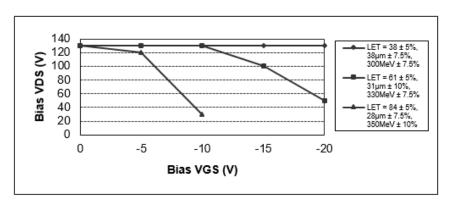


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

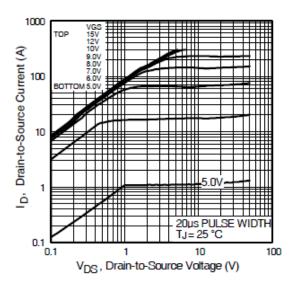


Fig 1. Typical Output Characteristics

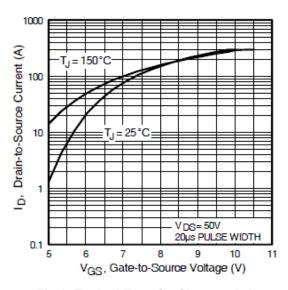


Fig 3. Typical Transfer Characteristics

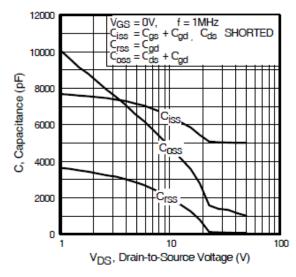


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

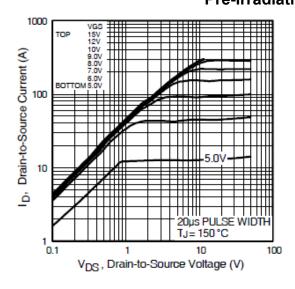


Fig 2. Typical Output Characteristics

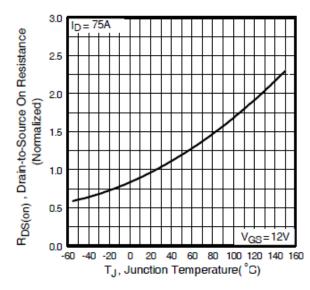


Fig 4. Normalized On-Resistance Vs. Temperature

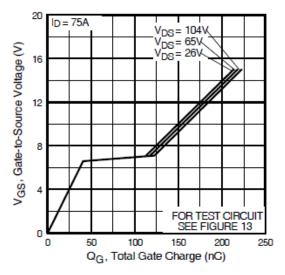


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



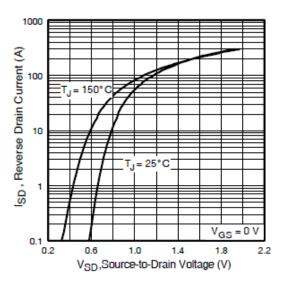


Fig 7. Typical Source-Drain Diode Forward Voltage

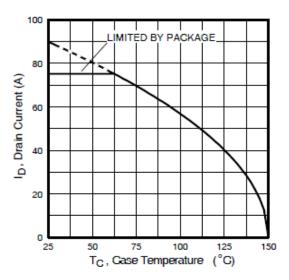


Fig 9. Maximum Drain Current Vs. Case Temperature

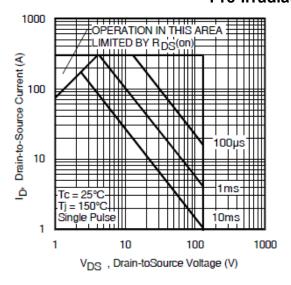


Fig 8. Maximum Safe Operating Area

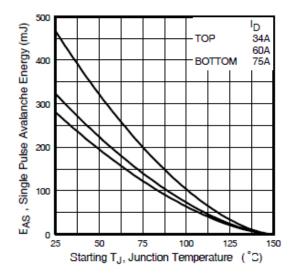


Fig 10. Maximum Avalanche Energy Vs. Drain Current

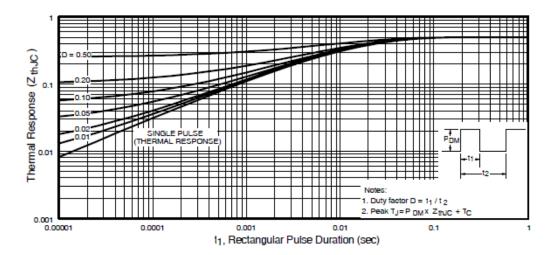


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



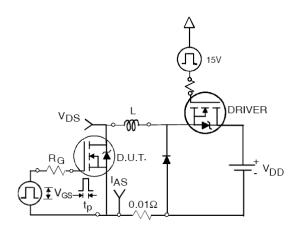


Fig 12a. Unclamped Inductive Test Circuit

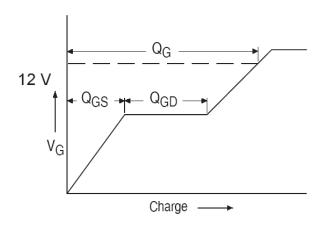


Fig 13a. Gate Charge Waveform

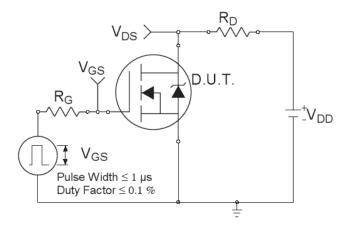


Fig 14a. Switching Time Test Circuit

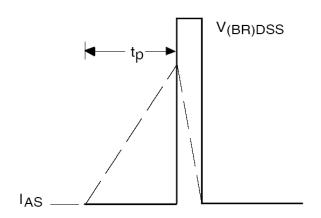


Fig 12b. Unclamped Inductive Wave-

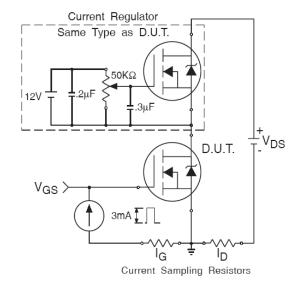


Fig 13b. Gate Charge Test Circuit

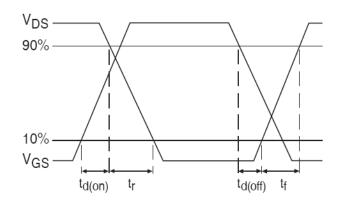
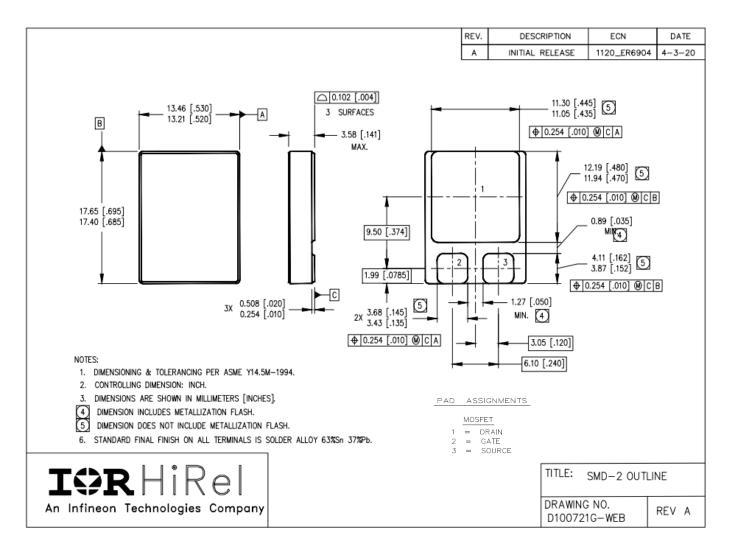


Fig 14b. Switching Time Waveforms



Note: For the most updated package outline, please see the website: SMD-2

Case Outline and Dimensions — SMD-2





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