

IRHMS57163SE JANSR2N7475T1

RADIATION HARDENED POWER MOSFET THRU-HOLE (Low-Ohmic TO-254AA)

130V, N-CHANNEL REF: MIL-PRF-19500/685

Product Summary

Part Number	Radiation Level	RDS(on)	Ι _D	QPL Part Number
IRHMS57163SE	100 kRads(Si)	0.0155Ω	45A*	JANSR2N7475T1



Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Eyelets
- · Electrically Isolated
- Light Weight
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 12V, T_{C} = 25°C	Continuous Drain Current	45*	
I _{D2} @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	45*	A
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	180	
P _D @ T _C = 25°C	Maximum Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	432	mJ
I _{AR} Avalanche Current ①		45	Α
E _{AR}	Repetitive Avalanche Energy ①	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt 3	11.3	V/ns
T _J	Operating Junction and	-55 to + 150	
T _{STG}	Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	g

^{*}Current is limited by package

For Footnotes refer to the page 2.

Pre-Irradiation

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	130			V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.16		V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance			0.0155	Ω	V _{GS} = 12V, I _{D2} = 45A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.5		4.5	V	$V_{DS} = V_{GS}$, $I_D = 1.0 \text{mA}$
Gfs	Forward Transconductance	36			S	V _{DS} = 15V, I _{D2} = 45A ④
I _{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{DS} = 104V, V_{GS} = 0V$
	Zero Gate Voltage Drain Current			25	μΛ	$V_{DS} = 104V, V_{GS} = 0V, T_{J} = 125$ °C
I _{GSS}	Gate-to-Source Leakage Forward			100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse			-100	117 ($V_{GS} = -20V$
Q_G	Total Gate Charge			160		$I_{D1} = 45A$
Q_{GS}	Gate-to-Source Charge			55	nC	$V_{DS} = 65V$
Q_GD	Gate-to-Drain ('Miller') Charge			75		$V_{GS} = 12V$
$t_{d(on)}$	Turn-On Delay Time			35		$V_{DD} = 65V$
tr	Rise Time			125	ns	I _{D1} = 45A
$t_{d(off)}$	Turn-Off Delay Time			80	115	$R_G = 2.35\Omega$
t _f	Fall Time			50		$V_{GS} = 12V$
Ls +L _D	Total Inductance		6.8		nΗ	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C _{iss}	Input Capacitance		5510			$V_{GS} = 0V$
C _{oss}	Output Capacitance		1490		pF	$V_{DS} = 25V$
C _{rss}	Reverse Transfer Capacitance		77			f = 1.0MHz
R_G	Gate Resistance		1.8		Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current (Body Diode)			45*		
I _{SM}	Pulsed Source Current (Body Diode) ①			180	A	
V_{SD}	Diode Forward Voltage			1.2	V	$T_J = 25^{\circ}C, I_S = 45A, V_{GS} = 0V$
t _{rr}	Reverse Recovery Time			300	ns	$T_J = 25^{\circ}C, I_F = 45A, V_{DD} \le 25V$
Q _{rr}	Reverse Recovery Charge			3.1	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

^{*} Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case			0.60	
$R_{\theta CS}$	Case -to-Sink		0.21		°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical Socket Mount)			48	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- \odot V_{DD} = 50V, starting T_J = 25°C, L = 0.43mH, Peak I_L = 45A, V_{GS} = 12V
- $\exists \quad I_{SD} \leq 45A, \ di/dt \leq 749A/\mu s, \ V_{DD} \leq 130V, \ T_J \leq 150^{\circ}C$
- \circ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- © Total Dose Irradiation with V_{DS} Bias. 104volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.



Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation \$6

Symbol	Parameter	100 kRa	ds (Si)	Units	Test Conditions	
		Min.	Max.			
BV _{DSS}	Drain-to-Source Breakdown Voltage	130		V	$V_{GS} = 0V, I_{D} = 1.0mA$	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	$V_{DS} = V_{GS}$, $I_D = 1.0 \text{mA}$	
I _{GSS}	Gate-to-Source Leakage Forward		100	nA	V _{GS} = 20V	
I _{GSS}	Gate-to-Source Leakage Reverse		-100	nA	V _{GS} = -20V	
I _{DSS}	Zero Gate Voltage Drain Current		10	μA	V _{DS} = 104V, V _{GS} = 0V	
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)		0.0140	Ω	V _{GS} = 12V, I _{D2} = 45A	
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-254AA)		0.0155	Ω	V _{GS} = 12V, I _{D2} = 45A	
V _{SD}	Diode Forward Voltage ④		1.2	V	V _{GS} = 0V, I _S = 45A	

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

		Range (μm)	VDS (V)					
LET (MeV/(mg/cm²))	Energy (MeV)		@ VGS = 0V	@ VGS = -5V	@ VGS = -10V	@ VGS = -15V	@ VGS = -20V	
38 ± 5%	300 ± 7.5%	38 ± 7.5%	130	130	130	130	130	
61 ± 5%	330 ±7. 5%	31 ± 10%	130	130	130	100	50	
84 ± 5%	350 ± 10%	28 ± 7.5%	130	120	30			

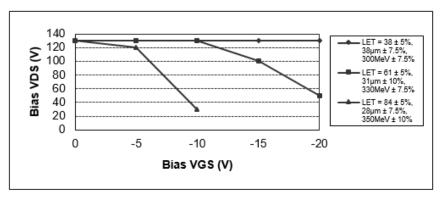


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.



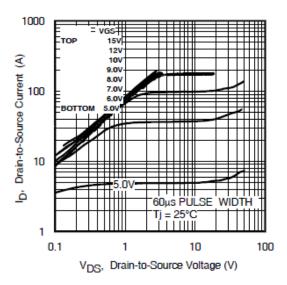


Fig 1. Typical Output Characteristics

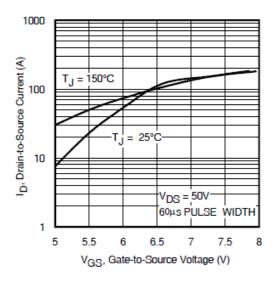


Fig 3. Typical Transfer Characteristics

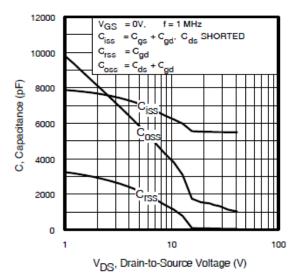


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

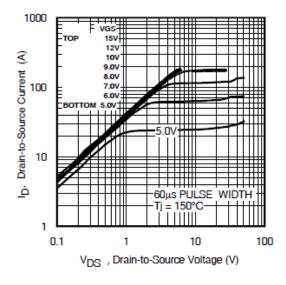


Fig 2. Typical Output Characteristics

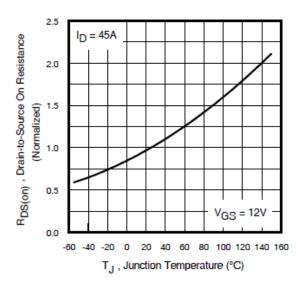


Fig 4. Normalized On-Resistance Vs. Temperature

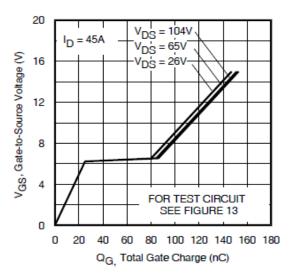


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage





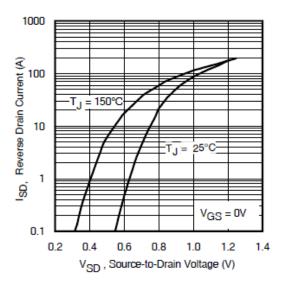


Fig 7. Typical Source-Drain Diode Forward Voltage

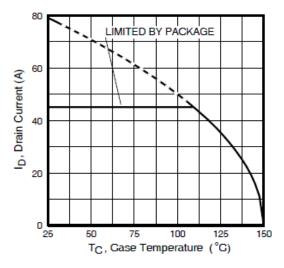


Fig 9. Maximum Drain Current Vs. Case Temperature

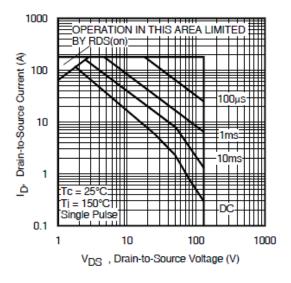


Fig 8. Maximum Safe Operating Area

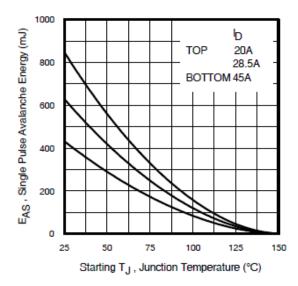


Fig 10. Maximum Avalanche Energy Vs. Drain Current

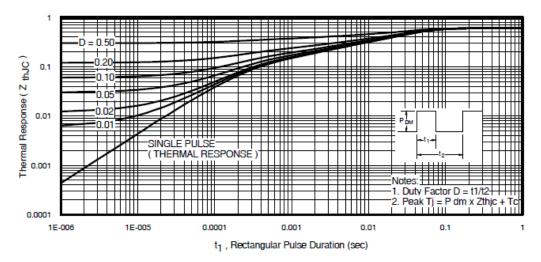


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



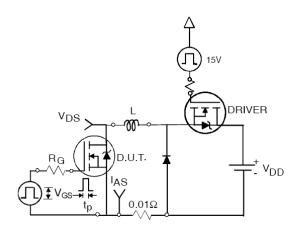


Fig 12a. Unclamped Inductive Test Circuit

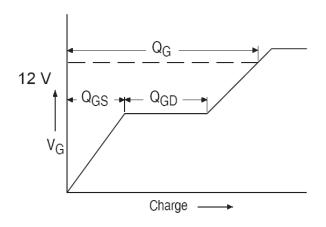


Fig 13a. Gate Charge Waveform

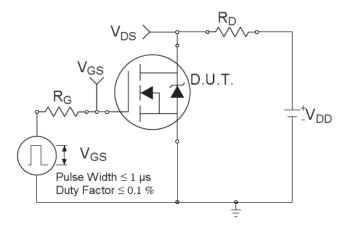


Fig 14a. Switching Time Test Circuit

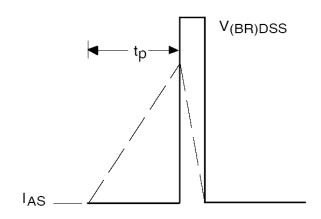


Fig 12b. Unclamped Inductive Wave-

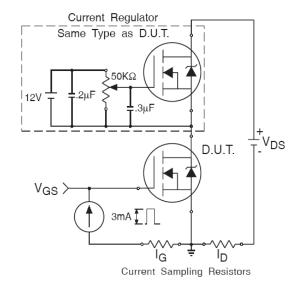


Fig 13b. Gate Charge Test Circuit

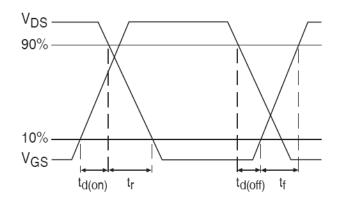
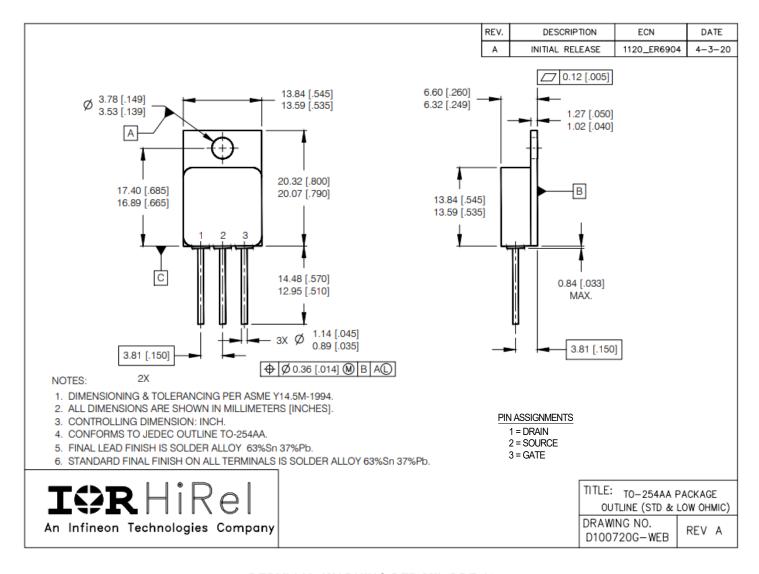


Fig 14b. Switching Time Waveforms



Note: For the most updated package outline, please see the website: Low-Ohmic TO-254AA

Case Outline and Dimensions - Low-Ohmic TO-254AA



BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.



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Data and specifications subject to change without notice.



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