IRHMB6S7160

PD-97992

Radiation Hardened Power MOSFET
Thru-Hole (Low Ohmic Tabless - TO-254AA)
100V, 45A, N-channel, R6 Technology

Features

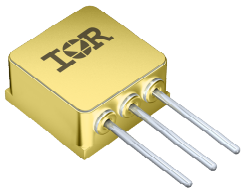
- Single event effect (SEE) hardened (up to LET of 60 MeV·cm²/mg)
- Low $R_{DS(on)}$
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- ESD rating: Class 3A per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Summary

- **Part number:** IRHMB6S7160
- **Radiation level:** 100 krad (Si)
- **$R_{DS(on),\ max}$:** 11mΩ
- **I_D:** 45A*



Low Ohmic Tabless - TO-254AA

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R6 S-line technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 60 MeV·cm²/mg. The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHMB6S7160	Low Ohmic Tabless - TO-254AA	COTS	100 krad (Si)
IRHMB6S7160SCS	Low Ohmic Tabless - TO-254AA	S-level	100 krad (Si)

*Current is limited by package

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	45*	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	45*	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	180	A
P_D @ T_C = 25°C	Maximum Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	512	mJ
I_{AR}	Avalanche Current [1]	45	A
E_{AR}	Repetitive Avalanche Energy [1]	20.8	mJ
dv/dt	Peak Diode Reverse Recovery [3]	6.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	g

*Current is limited by package

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = 25V, starting T_J = 25°C, L = 0.51mH, Peak I_L = 45A, V_{GS} = 12V

[3] $I_{SD} \leq$ 45A, di/dt ≤ 650A/µs, $V_{DD} \leq$ 100V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	11	mΩ	V_{GS} = 12V, I_{D2} = 45A [1]
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10.6	—	mV/°C	
Gfs	Forward Transconductance	45	—	—	S	V_{DS} = 15V, I_{D2} = 45A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V_{DS} = 80V, V_{GS} = 0V
		—	—	25		V_{DS} = 80V,V_{GS} = 0V,T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	170	nC	I_{D1} = 45A V_{DS} = 50V V_{GS} = 12V
Q_{GS}	Gate-to-Source Charge	—	—	60		
Q_{GD}	Gate-to-Drain (‘Miller’) Charge	—	—	80		
$t_{d(on)}$	Turn-On Delay Time	—	—	40	ns	I_{D1} = 45A ** V_{DD} = 50V R_G = 2.35Ω V_{GS} = 12V
t_r	Rise Time	—	—	125		
$t_{d(off)}$	Turn-Off Delay Time	—	—	85		
t_f	Fall Time	—	—	30		
L_s +L_D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in from package) to Source lead (6mm/0.25in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	8877	—	pF	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	1600	—		
C_{rss}	Reverse Transfer Capacitance	—	20.5	—		
R_G	Gate Resistance	—	1.05	—	Ω	f = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	45	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	180	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 45A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	500	ns	T_J = 25°C, I_F = 45A, V_{DD} ≤ 25V di/dt = 100A/µs [2]
Q_{rr}	Reverse Recovery Charge	—	—	6.4	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.6	°C/W
$R_{\theta CS}$	Junction-to-Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	48	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 100 krad (Si)		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	V_{DS} = V_{GS}, I_D = 6.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	—	10	µA	V_{DS} = 80V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [2]	—	0.011	Ω	V_{GS} = 12V, I_{D2} = 45A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-254AA) [2]	—	0.011	Ω	V_{GS} = 12V, I_{D2} = 45A
V_{SD}	Diode Forward Voltage	—	1.2	V	V_{GS} = 0V, I_F = 45A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = 12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = 80V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)						
			V_{GS} = 0V	V_{GS} = -5V	V_{GS} = -10V	V_{GS} = -15V	V_{GS} = -17V	V_{GS} = -19V	V_{GS} = -20V
37.7	380	46	100	100	100	100	100	100	40
60.5	697	56.7	100	100	100	30	—	—	—

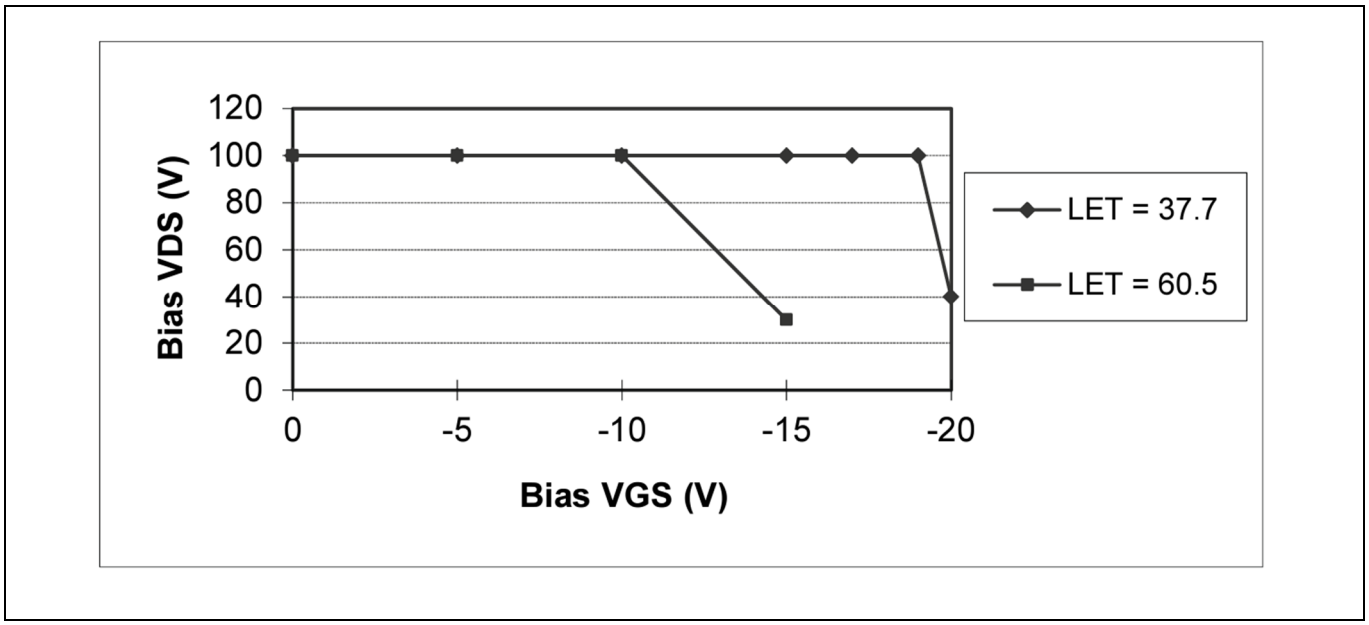


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

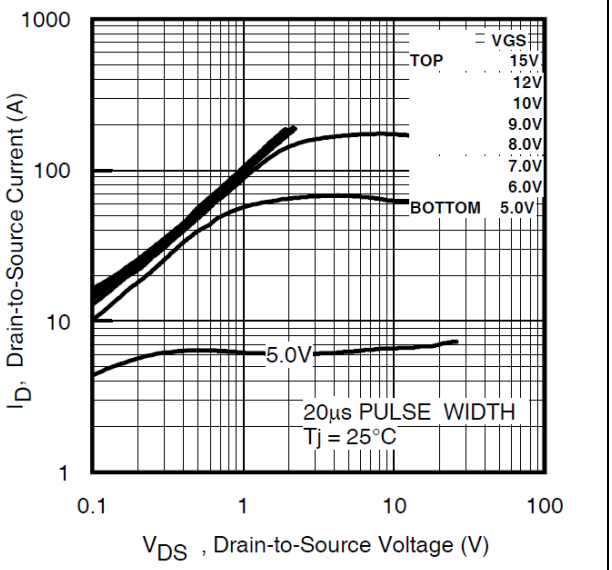


Figure 2 Typical Output Characteristics

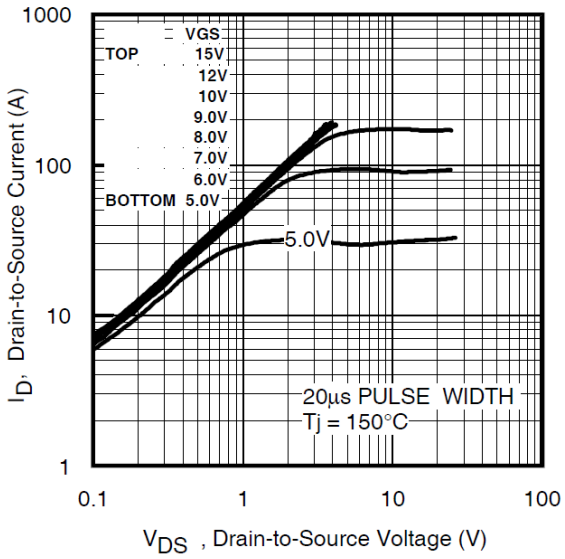


Figure 3 Typical Output Characteristics

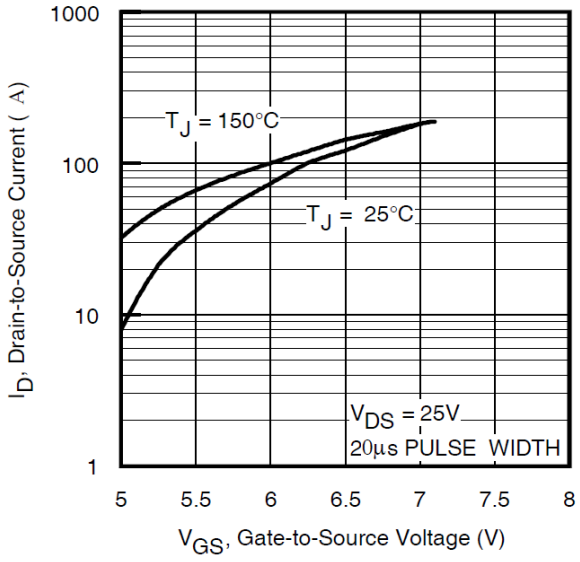


Figure 4 Typical Transfer Characteristics

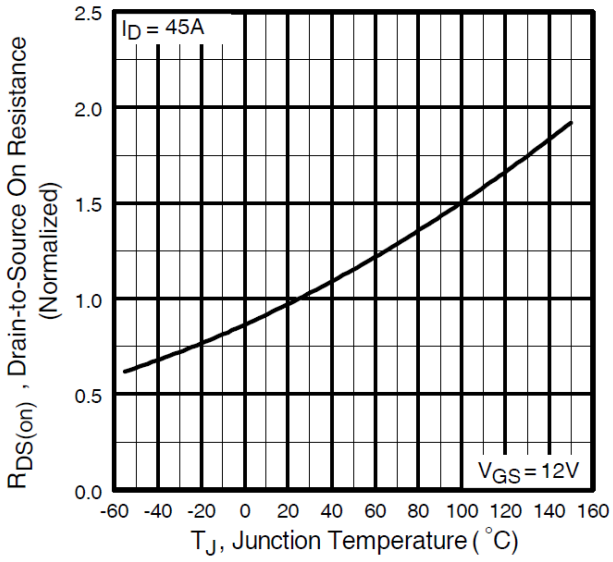


Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

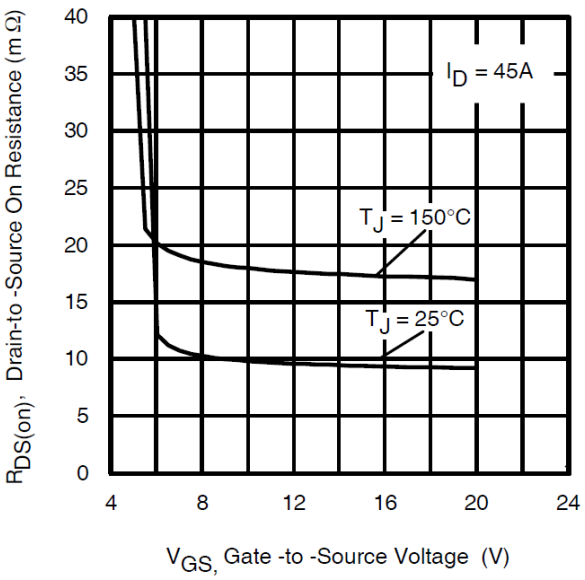


Figure 6 **Typical On-Resistance Vs Gate Voltage**

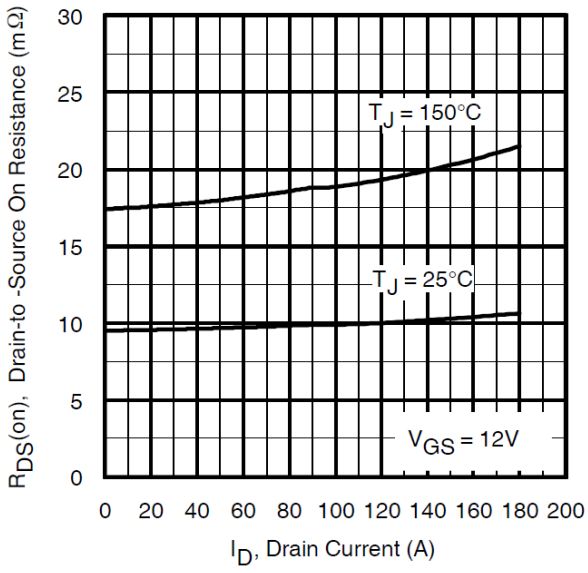


Figure 7 **Typical On-Resistance Vs Drain Current**

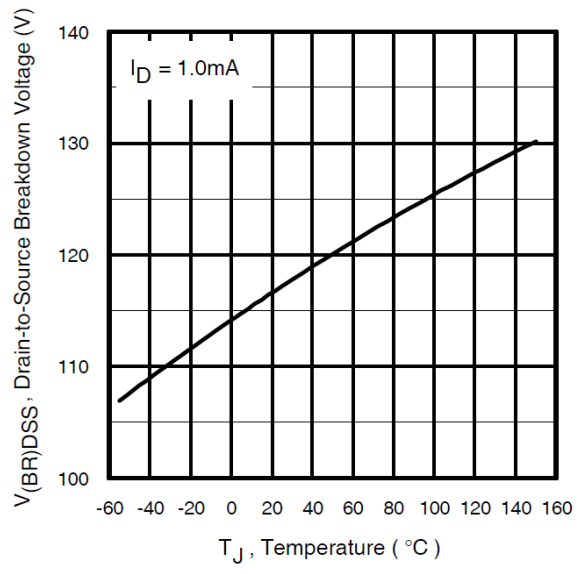


Figure 8 **Typical Drain-to-Source Breakdown Voltage Vs. Temperature**

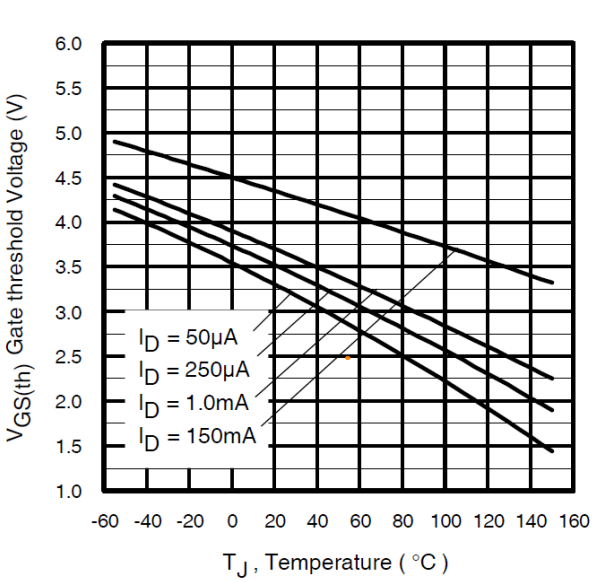


Figure 9 **Typical Gate-to-Source Voltage Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

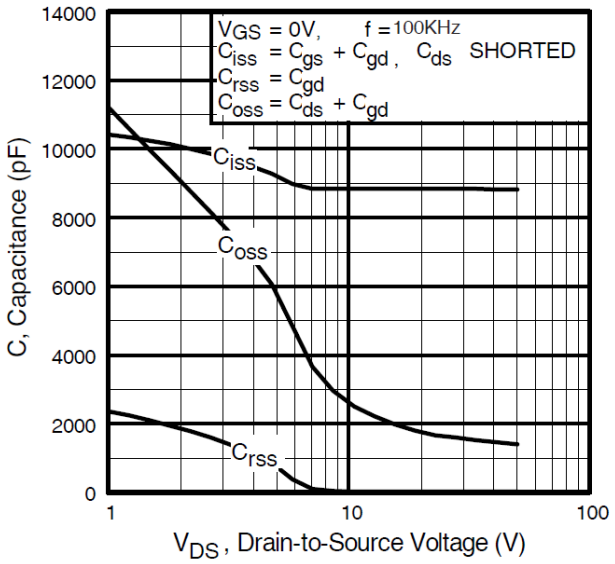


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

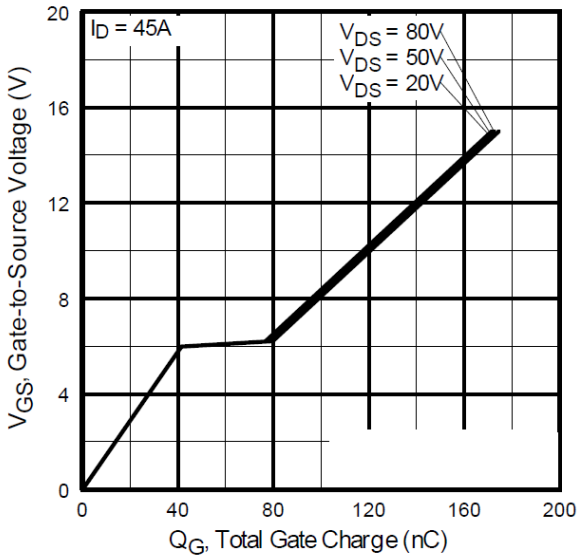


Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge

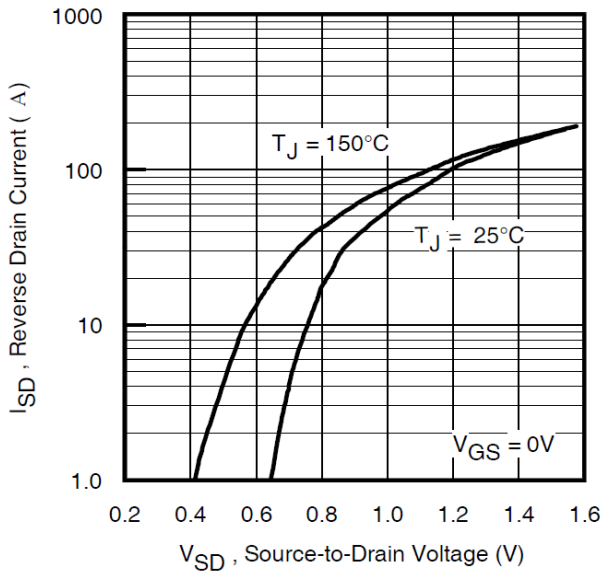


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

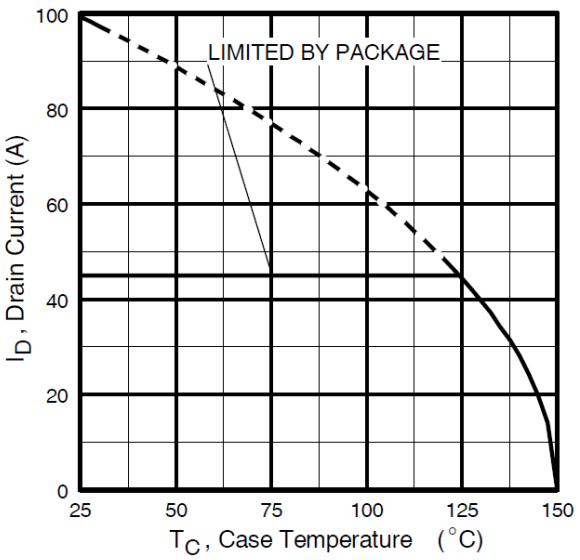


Figure 13 Maximum Drain Current Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

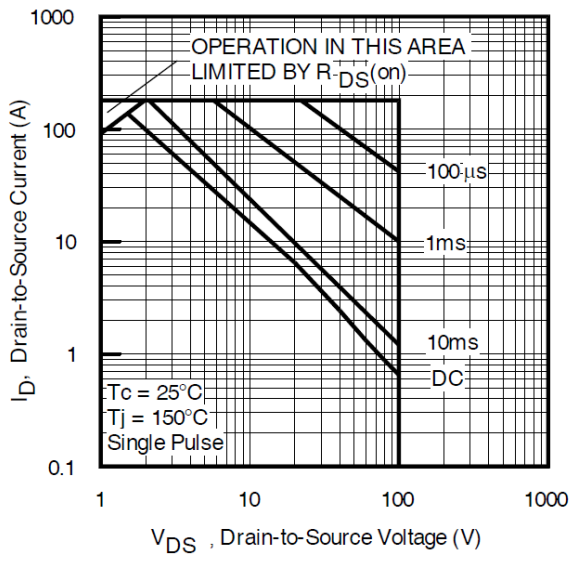


Figure 14 Maximum Safe Operating Area

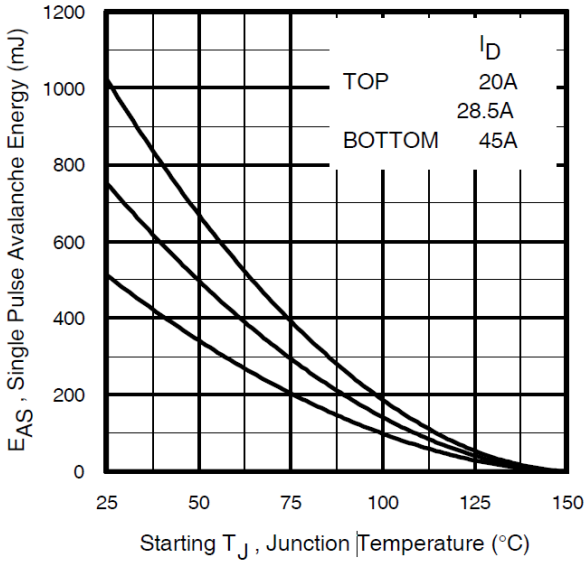


Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

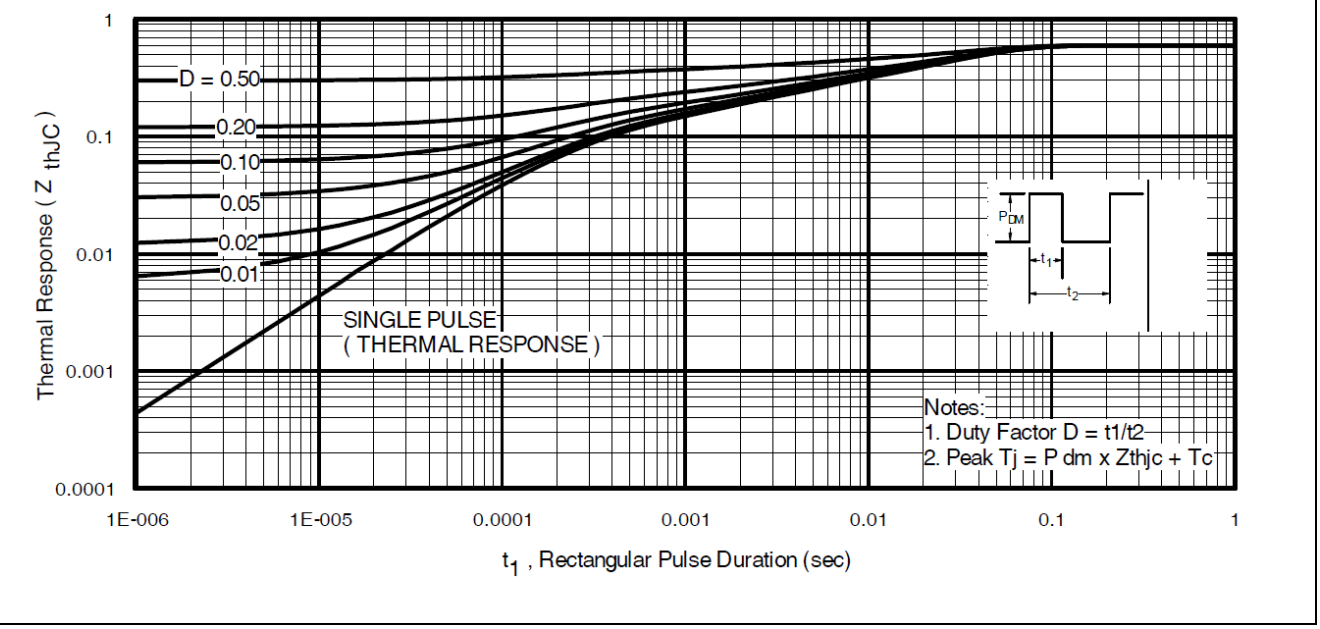


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

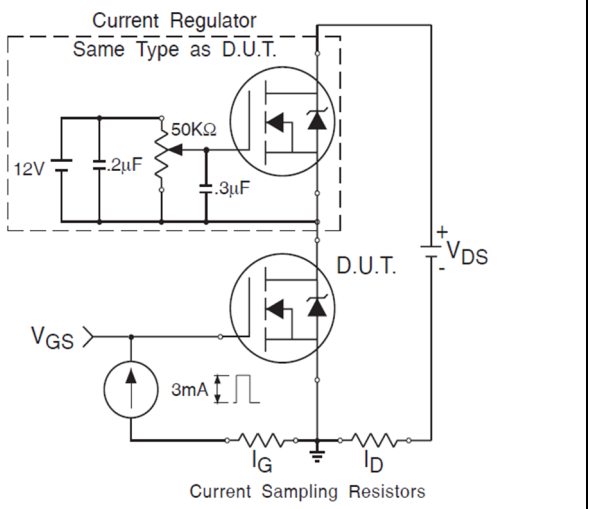


Figure 17 Gate Charge Test Circuit

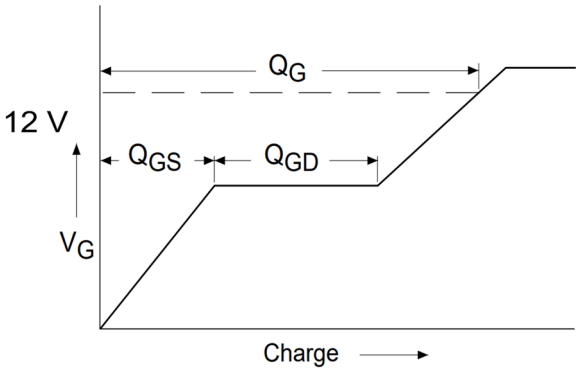


Figure 18 Gate Charge Waveform

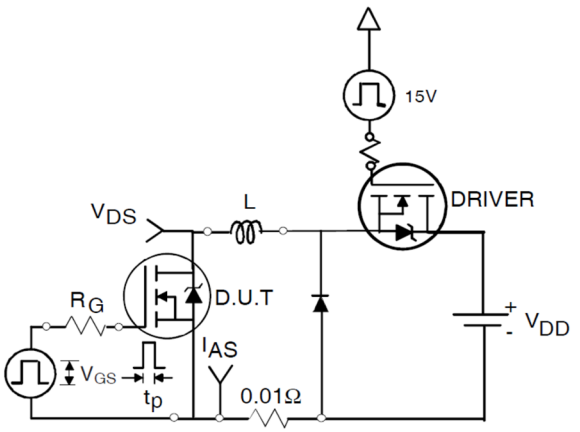


Figure 19 Unclamped Inductive Test Circuit

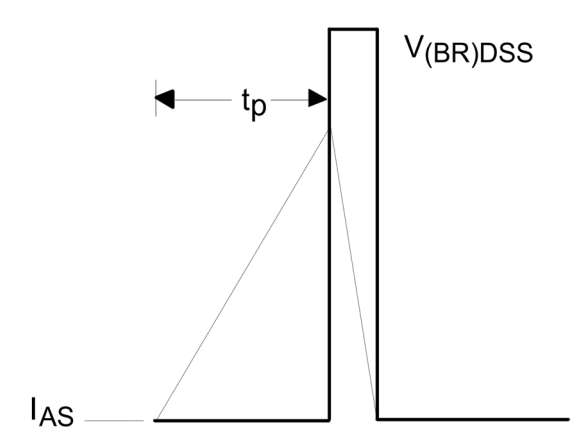


Figure 20 Unclamped Inductive Waveform

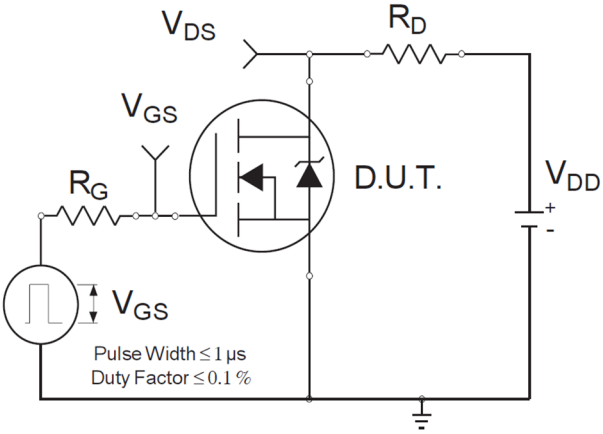


Figure 21 Switching Time Test Circuit

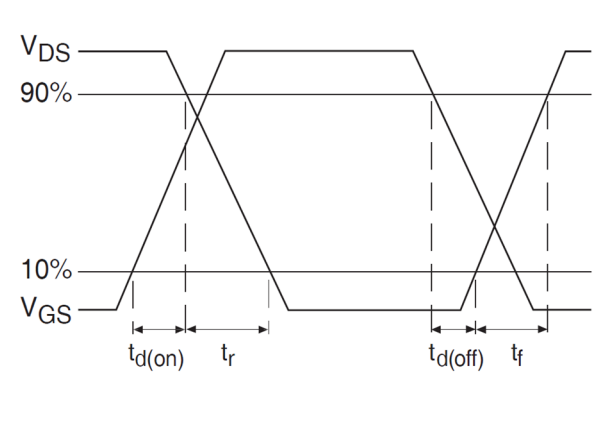
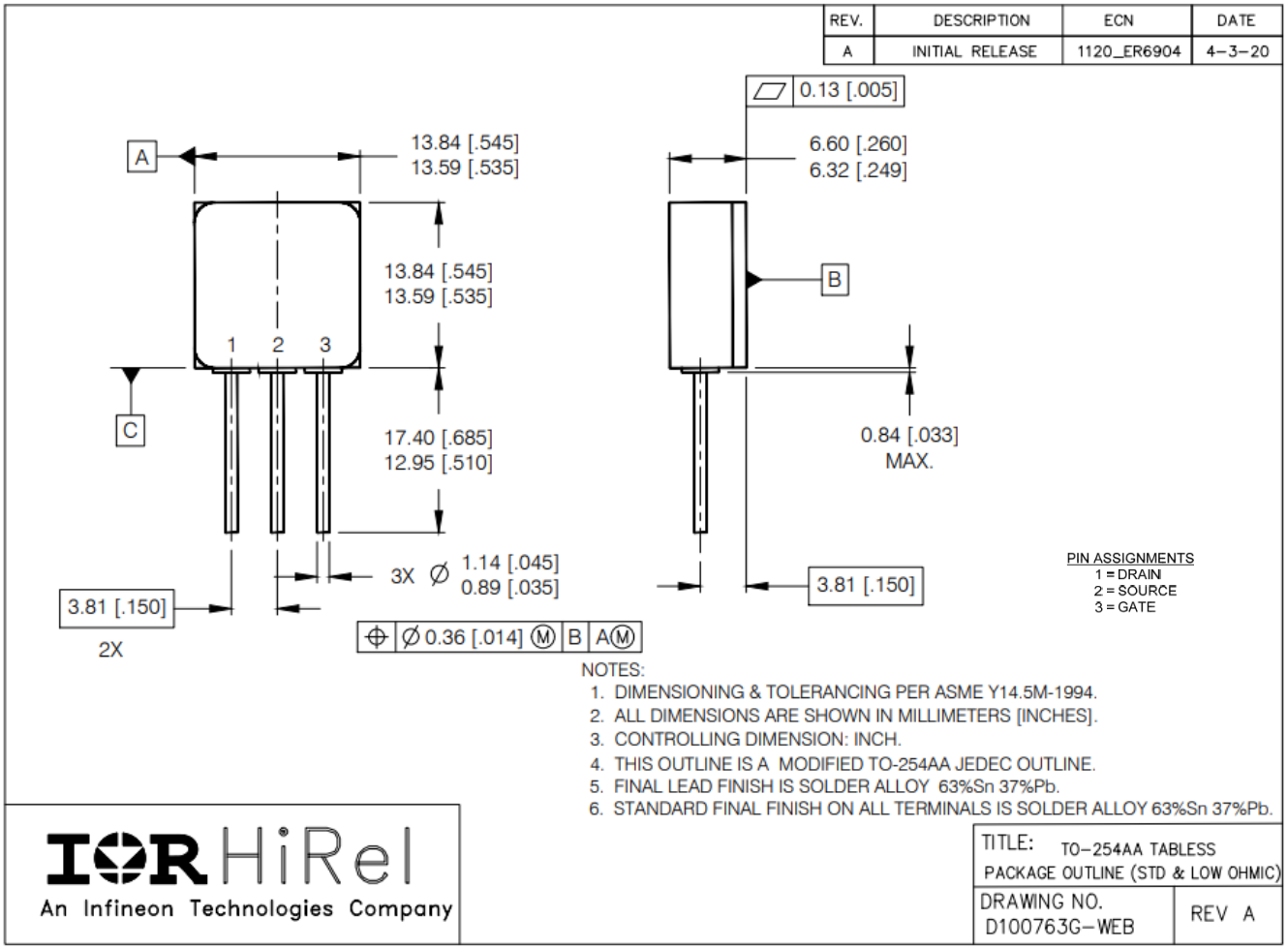


Figure 22 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: [Low Ohmic Tabless - TO-254AA]



BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

Revision history

Document version	Date of release	Description of changes
	10/29/2021	Final datasheet with PD number (PD-97992)

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Edition 2021-10-29

Published by

International Rectifier HiRel Products, Inc.

An Infineon Technologies company

El Segundo, California 90245 USA

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Document reference

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