IRHLNS87Y50

PD-97956A

Radiation Hardened Logic Power MOSFET
Surface-Mount (SupIR-SMD™)
20V, 75A, N-channel, R8 Technology

Features

- Single event effect (SEE) hardened (up to LET of 92 MeV·cm²/mg)
- 5V CMOS and TTL compatible
- Low $R_{DS(on)}$
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Surface mount
- Light weight
- ESD rating: class 2 per MIL-STD-750, Method 1020

Product Summary

- **Part number:** IRHLNS87Y50
- **Radiation level:** 100 krad(Si)
- $R_{DS(on),\,max}$**:** 2.5mΩ
- I_D**:** 75A*

SupIR-SMD™

Potential Applications

- Point-of-Load (PoL) converters for FPGA, ASIC and DSP core rails
- Synchronous rectification
- Redundant power distribution

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R8 Logic level power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHLNS87Y50	SupIR-SMD™	COTS	100krad(Si)
IRHLNS87Y50SCS	SupIR-SMD™	QIRL	100krad(Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 4.5V, T_C = 25°C	Continuous Drain Current	75*	A
I_{D2} @ V_{GS} = 4.5V, T_C = 100°C	Continuous Drain Current	75*	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	300	A
P_D @ T_C = 25°C	Maximum Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	+ 12/-10	V
E_{AS}	Single Pulse Avalanche Energy [2]	535	mJ
I_{AR}	Avalanche Current [1]	75	A
E_{AR}	Repetitive Avalanche Energy [1]	12.5	mJ
dv/dt	Peak Diode Reverse Recovery [3]	0.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

* Current is limited by package

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = 20V, starting T_J = 25°C, L = 0.19mH, Peak I_L = 75A, V_{GS} = 10V

[3] $I_{SD} \leq$ 75A, di/dt ≤ 450A/µs, $V_{DD} \leq$ 20V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	Reference to 25°C, I_D = 250µA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	2.5	mΩ	V_{GS} = 4.5V, I_{D2} = 75A [1]
		—	—	2.3		V_{GS} = 7.0V, I_{D2} = 75A [4]
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.3	V	$V_{DS} \geq V_{GS}$, I_D = 1.8mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.3	—	mV/°C	
Gfs	Forward Transconductance	75	—	—	S	V_{DS} = 15V, I_{D2} = 75A [4]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	µA	V_{DS} = 16V, V_{GS} = 0V
		—	—	50		V_{DS} = 16V,V_{GS} = 0V,T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 12V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_G	Total Gate Charge	—	—	130	nC	I_{D1} = 75A V_{DS} = 10V V_{GS} = 4.5V
Q_{GS}	Gate-to-Source Charge	—	—	50		
Q_{GD}	Gate-to-Drain (‘Miller’) Charge	—	—	35		
$t_{d(on)}$	Turn-On Delay Time	—	—	80	ns	I_{D1} = 75A ** V_{DD} = 10V R_G = 2.35Ω V_{GS} = 4.5V
t_r	Rise Time	—	—	130		
$t_{d(off)}$	Turn-Off Delay Time	—	—	100		
t_f	Fall Time	—	—	55		
$L_s + L_D$	Total Inductance	—	12	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	15330	—	pF	V_{GS} = 0V V_{DS} = 20V ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	3140	—		
C_{rss}	Reverse Transfer Capacitance	—	610	—		
R_G	Gate Resistance	—	0.4	—	Ω	ƒ = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	75	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	300	A	
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 75A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	100	ns	T_J = 25°C, I_F = 75A, V_{DD} ≤ 20V di/dt = -100A/µs [6]
Q_{rr}	Reverse Recovery Charge	—	—	155	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics - Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 100krads (Si)[5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	V	V_{GS} = 0V, I_D = 1mA
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.3	V	V_{DS} ≥ V_{GS}, I_D = 1.8mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 12V
	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -10V
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	µA	V_{DS} = 16V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [6]	—	3.0	mΩ	V_{GS} = 4.5V, I_{D2} = 75A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SupIR-SMD)[6]	—	2.5	m Ω	V_{GS} = 4.5V, I_{D2} = 75A
V_{SD}	Diode Forward Voltage	—	1.0	V	V_{GS} = 0V, I_F = 75A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = 12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = 16V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

2.4.2 Single Event Effects – Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)		
			V_{GS} = 0V	V_{GS} = -1V	V_{GS} = -2V
40 ± 5%	275 ± 5%	35.6 ± 5%	16	16	—
64 ± 7.5%	600 ± 12.5%	49 ± 10%	14	14	—
92 ± 5%	1150 ± 5%	65.1 ± 5%	12	12	—

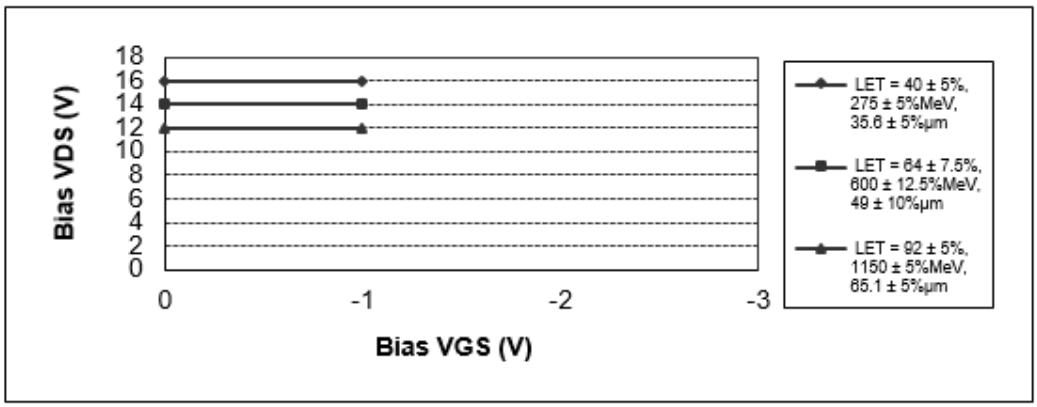


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

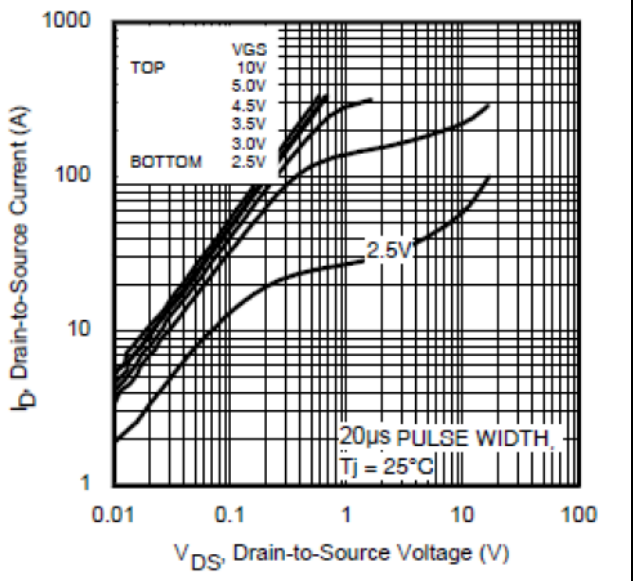


Figure 2 **Typical Output Characteristics**

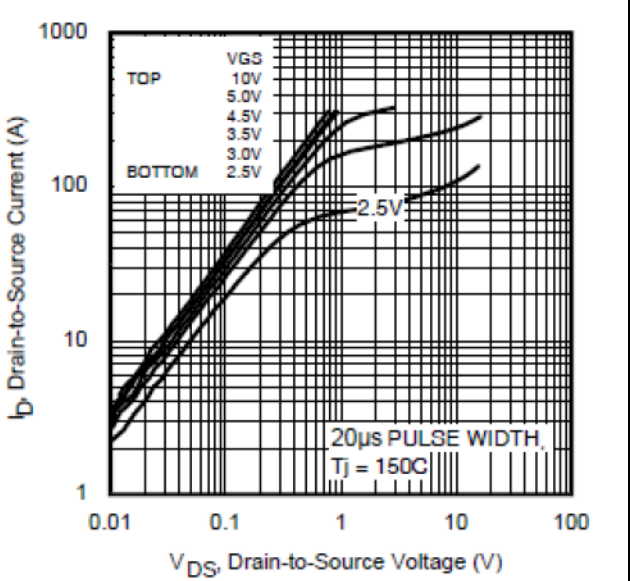


Figure 3 **Typical Output Characteristics**

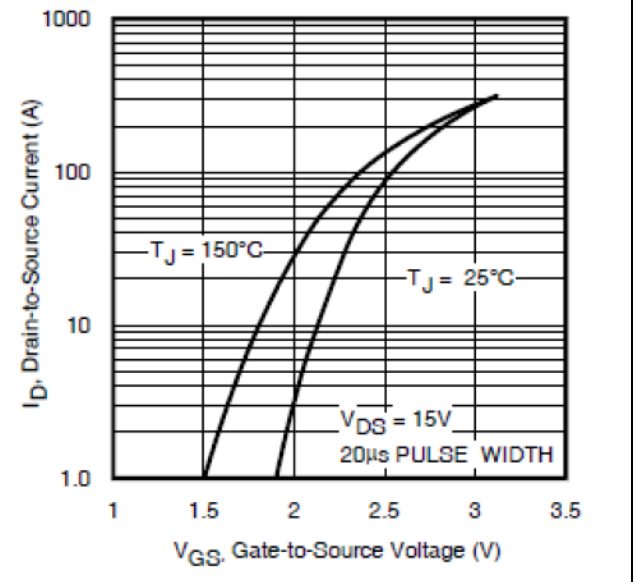


Figure 4 **Typical Transfer Characteristics**

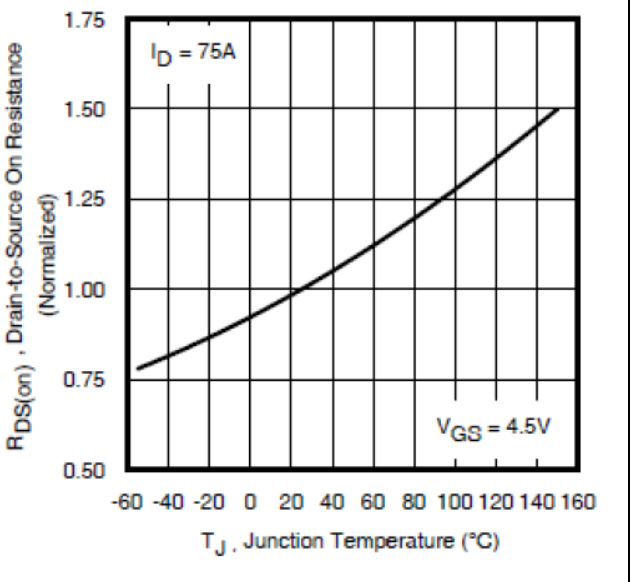


Figure 5 **Normalized On-Resistance Vs. Temperature**

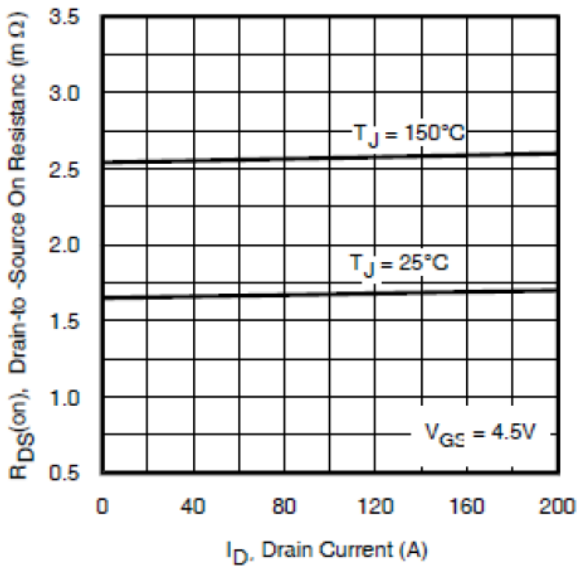


Figure 6 **Typical On-Resistance Vs. Gate Voltage**

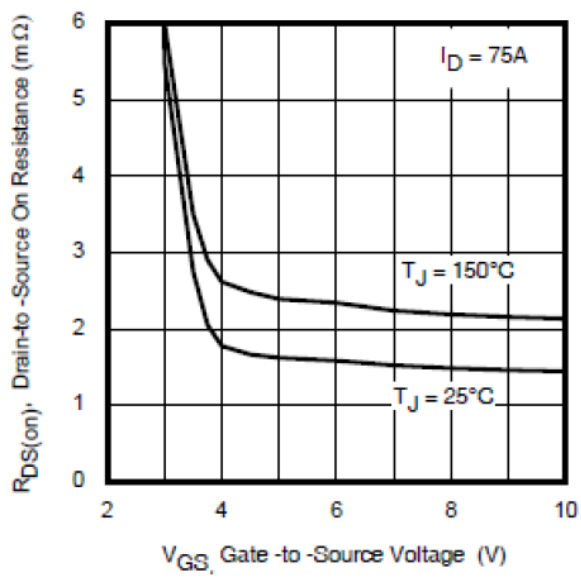


Figure 7 **Typical On-Resistance Vs. Drain Current**

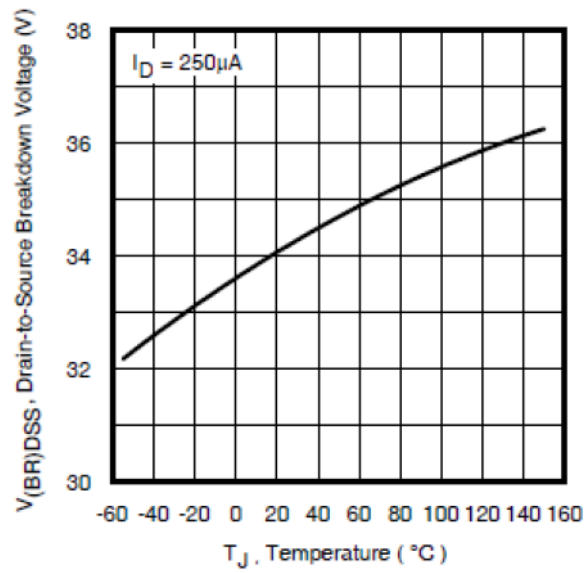


Figure 8 **Typical Drain-to-Source Breakdown Voltage Vs. Temperature**

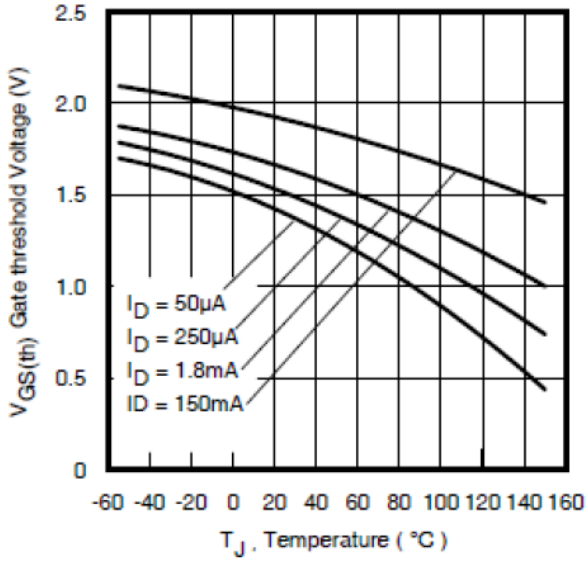


Figure 9 **Typical Threshold Voltage Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

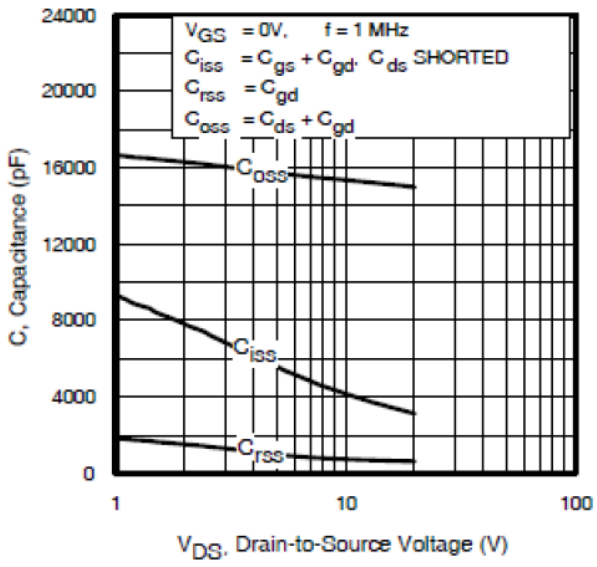


Figure 10 **Typical Capacitance Vs. Drain-to-Source Voltage**

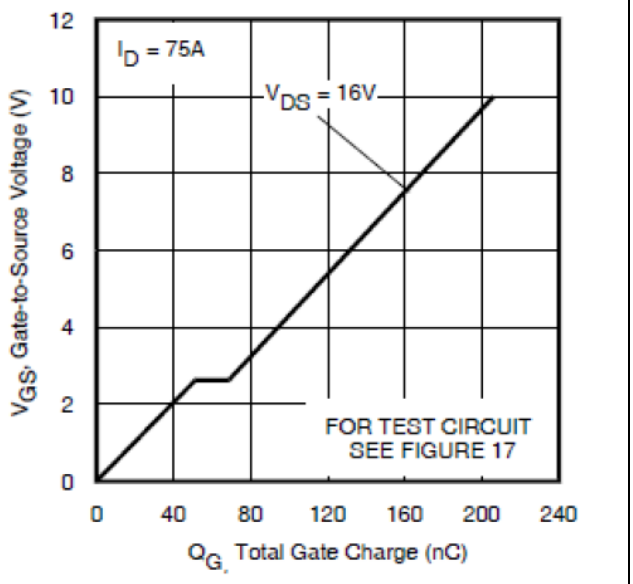


Figure 11 **Typical Gate Charge Vs. Gate-to-Source Voltage**

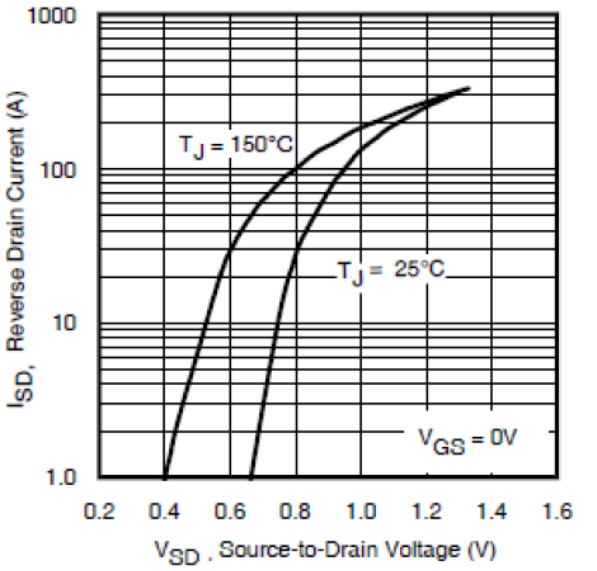


Figure 12 **Typical Source-Drain Vs. Diode Forward Voltage**

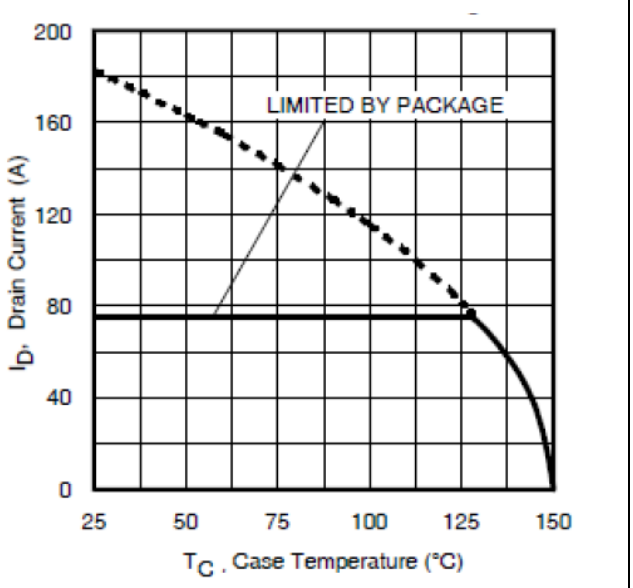


Figure 13 **Maximum Drain Current Vs.Case Temperature**

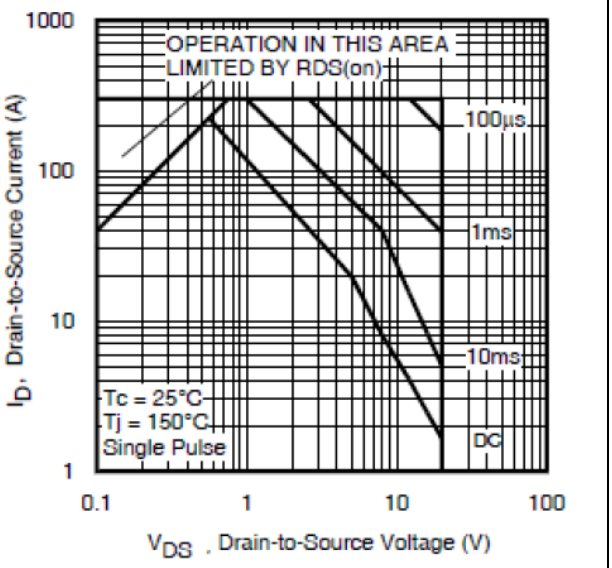


Figure 14 Maximum Safe Operating Area

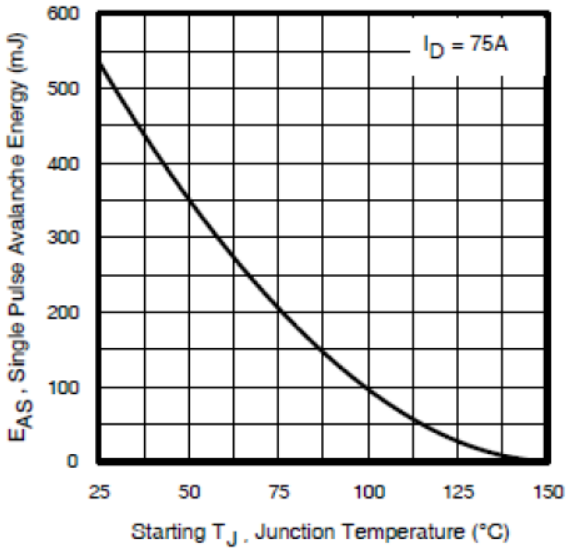


Figure 15 Maximum Avalanche Energy Vs. Drain Current

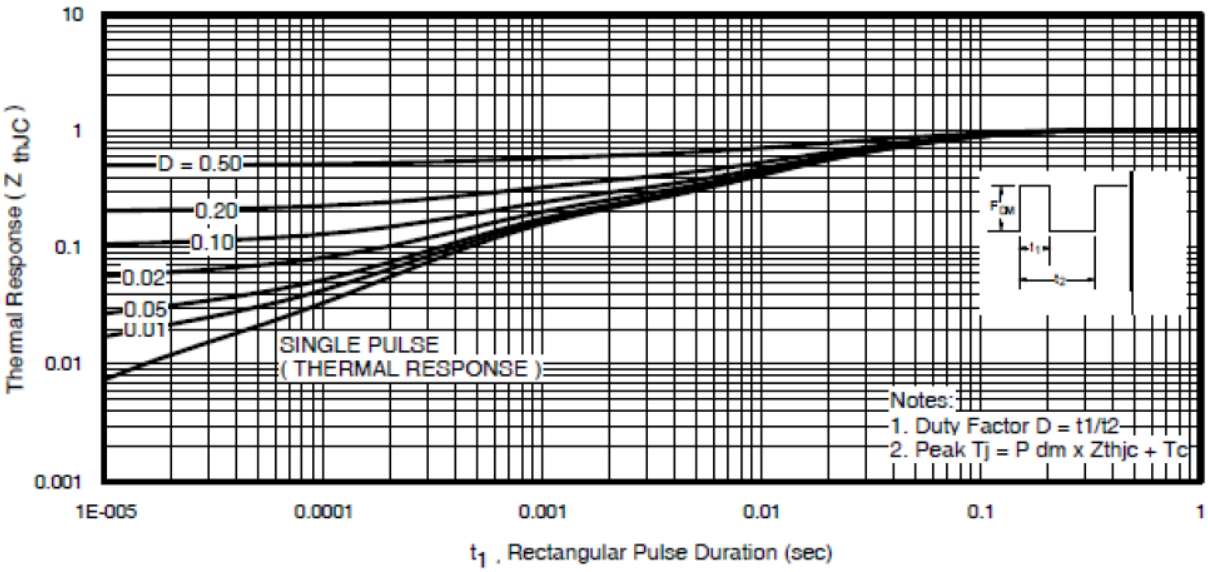


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

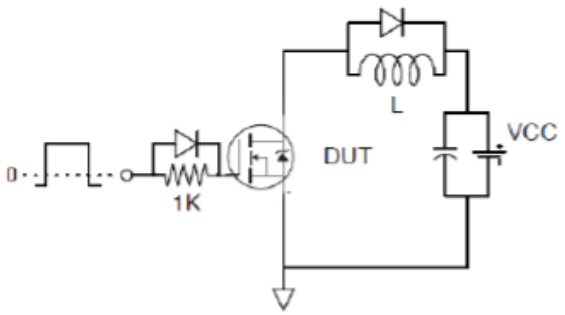


Figure 17 Gate Charge Test Circuit

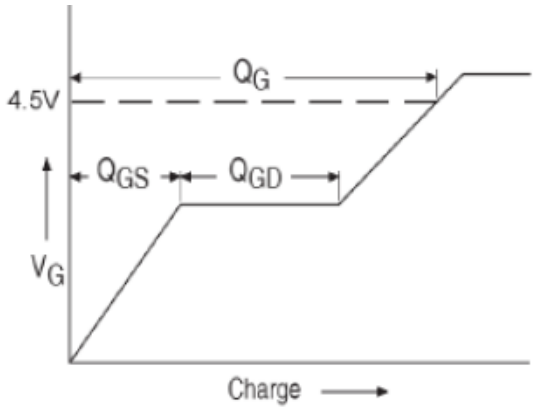


Figure 18 Gate Charge Waveform

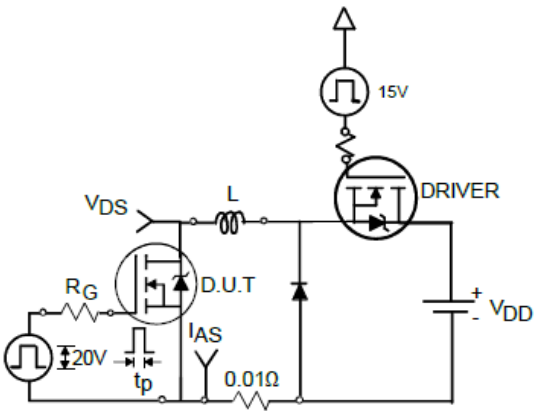


Figure 19 Unclamped Inductive Test Circuit

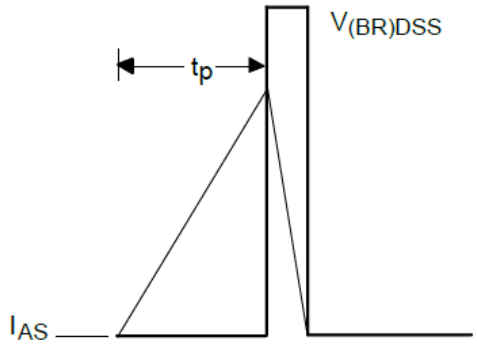


Figure 20 Unclamped Inductive Waveform

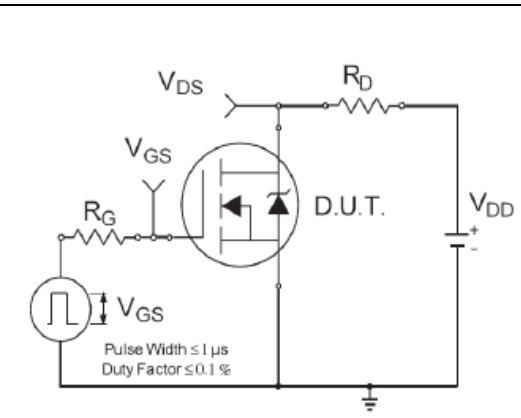


Figure 21 Switching Time Test Circuit

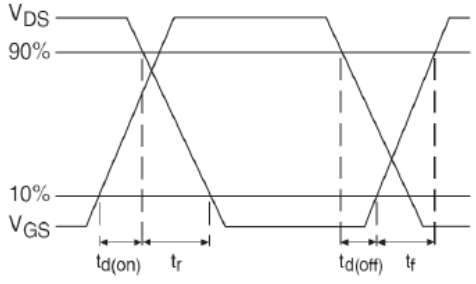
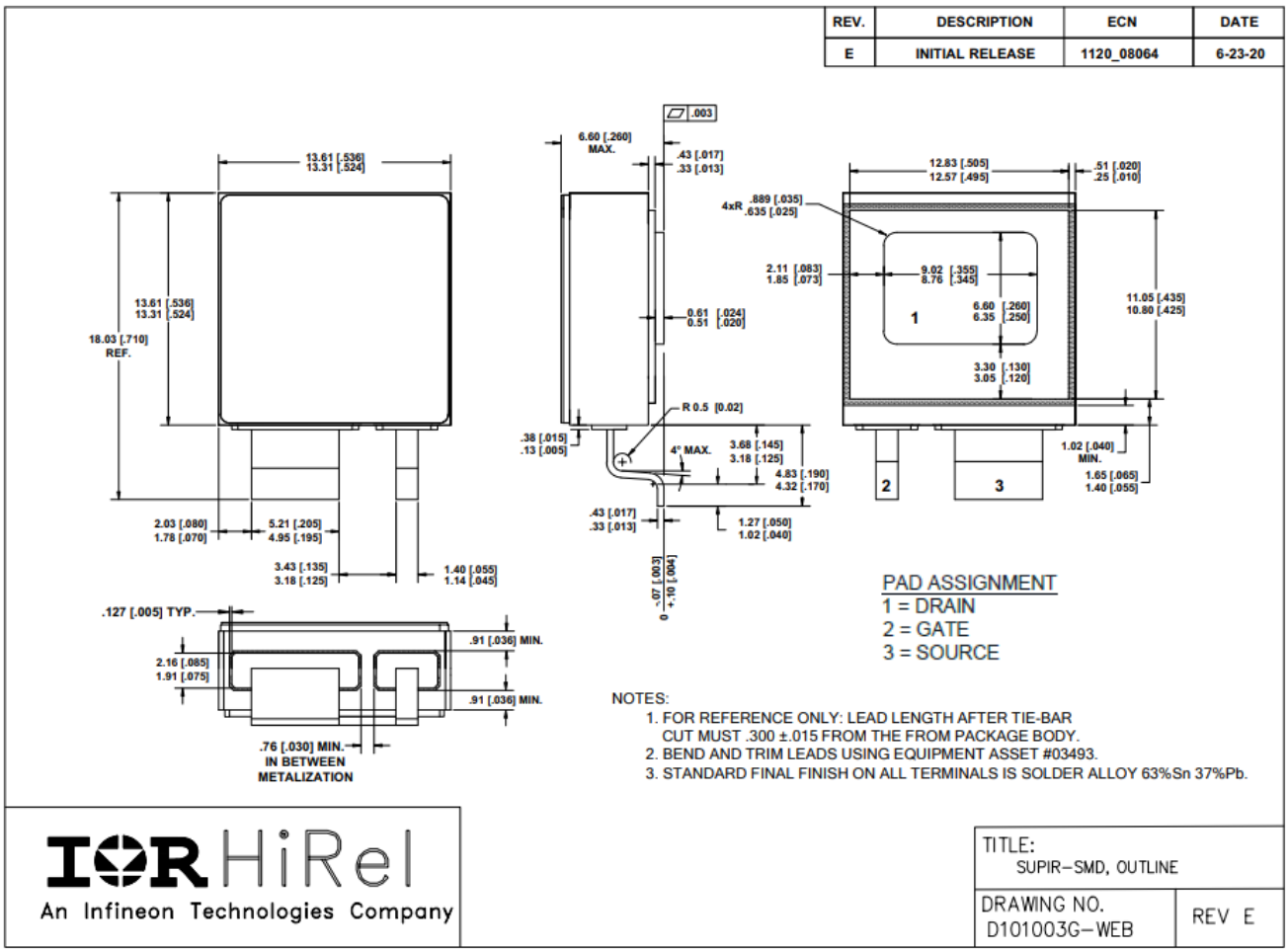


Figure 22 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: SupIR-SMD



Revision history

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Rev A	01/31/2022	Updated based on ECN-1120_8881

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