

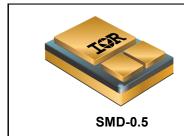


# RADIATION HARDENED LOGIC LEVEL POWER MOSFET SURFACE MOUNT (SMD-0.5)

**Product Summary** 

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Part Number	Radiation Level	RDS(on)	I <sub>D</sub>	QPL Part Number				
IRHLNJ797034	100 kRads(Si)	$0.072\Omega$	-22A*	JANSR2N7624U3				
IRHLNJ793034	300 kRads(Si)	0.072Ω	-22A*	JANSF2N7624U3				





## **Description**

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

## **Features**

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

## **Absolute Maximum Ratings**

## **Pre-Irradiation**

Symbol	Parameter	Value	Units	
I <sub>D1</sub> @ V <sub>GS</sub> = -4.5V, T <sub>C</sub> = 25°C	Continuous Drain Current	-22*		
<sub>D2</sub> @ V <sub>GS</sub> = -4.5V, T <sub>C</sub> = 100°C	Continuous Drain Current	-14.9	A	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C Pulsed Drain Current ①		-88		
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	57	W	
	Linear Derating Factor	0.45	W/°C	
$V_{GS}$	Gate-to-Source Voltage	± 10	V	
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	79	mJ	
I <sub>AR</sub>	Avalanche Current ①	-22	А	
$E_{AR}$	Repetitive Avalanche Energy ①	5.7	mJ	
dv/dt	Peak Diode Recovery dv/dt ③	-12.3	V/ns	
T <sub>J</sub>	Operating Junction and	-55 to + 150		
$T_{STG}$	Storage Temperature Range		°C	
	Pckg. Mounting Surface Temp.	300 (for 5s)		
	Weight	1.0 (Typical)	g	

<sup>\*</sup> Current is limited by package

For Footnotes refer to the page 2.



## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-60			V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		-0.055		V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance			0.072	Ω	V <sub>GS</sub> = -4.5V, I <sub>D2</sub> = -14.9A ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-2.0	V	V - V I - 050··A
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient		3.5		mV/°C	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
Gfs	Forward Transconductance	16			S	V <sub>DS</sub> = -10V, I <sub>D2</sub> = -14.9A ④
I <sub>DSS</sub>	Zero Ceta Voltago Draig Comment			-1.0		V <sub>DS</sub> = -48V, V <sub>GS</sub> = 0V
	Zero Gate Voltage Drain Current			-15	μA	$V_{DS} = -48V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I <sub>GSS</sub>	Gate-to-Source Leakage Forward			-100	nA	V <sub>GS</sub> = -10V
	Gate-to-Source Leakage Reverse			100	ΠA	V <sub>GS</sub> = 10V
$Q_G$	Total Gate Charge			36		$I_{D1} = -22A$
$Q_{GS}$	Gate-to-Source Charge	l		10	nC	V <sub>DS</sub> = -30V
$Q_{GD}$	Gate-to-Drain ('Miller') Charge			18		V <sub>GS</sub> = -4.5V
t <sub>d(on)</sub>	Turn-On Delay Time			32		V <sub>DD</sub> = -30V
tr	Rise Time			250		$I_{D1} = -22A$
t <sub>d(off)</sub>	Turn-Off Delay Time			100	ns	$R_G = 7.5\Omega$
t <sub>f</sub>	Fall Time			102		$V_{GS} = -5.0V$
Ls +L <sub>D</sub>	Total Inductance		4.0		nH	Measured from the center of drain pad to center of source pad
C <sub>iss</sub>	Input Capacitance		2261			V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance		583		pF	$V_{DS} = -25V$
C <sub>rss</sub>	Reverse Transfer Capacitance		91			f = 1.0MHz
$R_G$	Gate Resistance			20	Ω	f = 1.0MHz,open drain

## **Source-Drain Diode Ratings and Characteristics**

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Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions		
Is	Continuous Source Current (Body Diode)			-22*	Α			
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①			-88				
$V_{SD}$	Diode Forward Voltage			-5.0	V	$T_J = 25^{\circ}C, I_S = -22A, V_{GS} = 0V$		
t <sub>rr</sub>	Reverse Recovery Time			110	ns	$T_J = 25^{\circ}C, I_F = -22A,$		
Q <sub>rr</sub>	Reverse Recovery Charge			132	nC	V <sub>DD</sub> ≤ -50V, di/dt = -100A/μs ④		
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )						

<sup>\*</sup> Current is limited by package

### **Thermal Resistance**

Symbol	Parameter	Min.	Тур.	Max.	Units
$R_{ heta JC}$	Junction-to-Case			2.2	°C/W

#### Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- $^{\circ}$  V<sub>DD</sub> = -25V, starting T<sub>J</sub> = 25°C, L = 0.32mH, Peak I<sub>L</sub> = -22A, V<sub>GS</sub> = -10V
- $\label{eq:local_spectrum} \mbox{ } \$
- 4 Pulse width  $\leq 300 \ \mu s$ ; Duty Cycle  $\leq 2\%$
- $\odot$  Total Dose Irradiation with  $V_{GS}$  Bias. -10 volt  $V_{GS}$  applied and  $V_{DS}$  = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- $\odot$  Total Dose Irradiation with V<sub>DS</sub> Bias. -48 volt V<sub>DS</sub> applied and V<sub>GS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.



#### **Radiation Characteristics**

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation \$6

Symbol	Parameter	Up to 300	kRads (Si) <sup>1</sup>	Units	Test Conditions	
		Min.	Max.	010		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-60		V	$V_{GS} = 0V, I_D = -250\mu A$	
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0	-2.0	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
I <sub>GSS</sub>	Gate-to-Source Leakage Forward		-100	nA	V <sub>GS</sub> = -10V	
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse		100	nA	V <sub>GS</sub> = 10V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current		-1.0	μA	$V_{DS} = -48V, V_{GS} = 0V$	
R <sub>DS(on)</sub>	Static Drain-to-Source @ On-State Resistance (TO-3)		0.076	Ω	V <sub>GS</sub> = -4.5V, I <sub>D2</sub> = -14.9A	
R <sub>DS(on)</sub>	Static Drain-to-Source @ On-State Resistance (SMD-0.5)		0.072	Ω	V <sub>GS</sub> = -4.5V, I <sub>D2</sub> = -14.9A	
V <sub>SD</sub>	Diode Forward Voltage ④		-5.0	V	$V_{GS} = 0V, I_{S} = -22A$	

Part numbers IRHLNJ797034 (JANSR2N7624U3) and IRHLNJ793034 (JANSF2N7624U3)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET	Energy	Range	V <sub>DS</sub> (V)					
(MeV/(mg/cm²))	(MeV)	(µm)	@VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-40
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	
85 ± 5%	380 ± 10%	29± 7.5%	-60	-60	-60	-60		

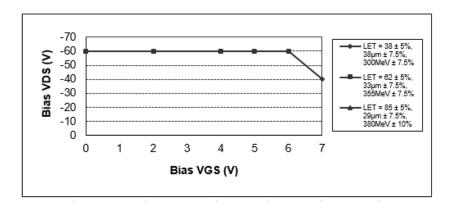


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.



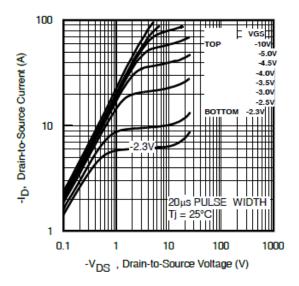


Fig 1. Typical Output Characteristics

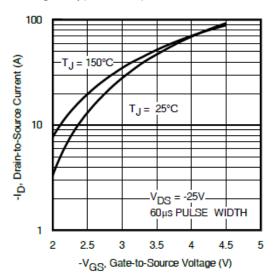
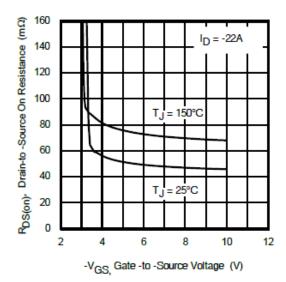


Fig 3. Typical Transfer Characteristics



**Fig 5.** Typical On-Resistance Vs Gate Voltage

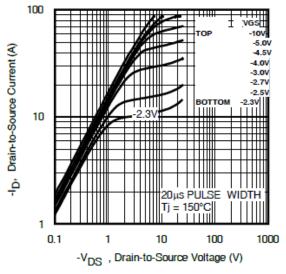


Fig 2. Typical Output Characteristics

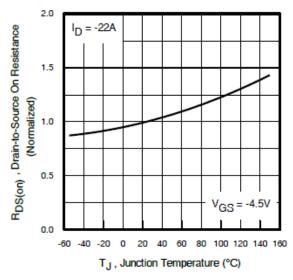


Fig 4. Normalized On-Resistance Vs. Temperature

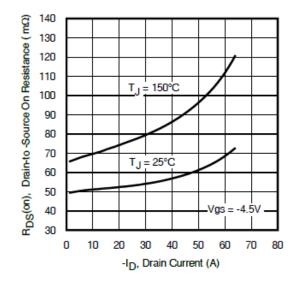
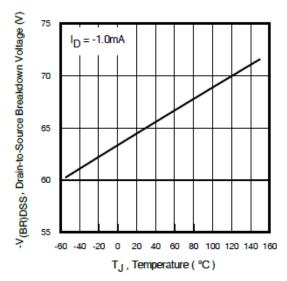
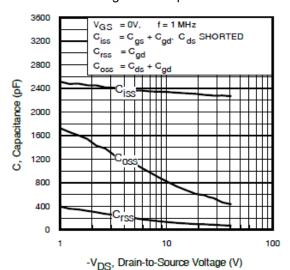


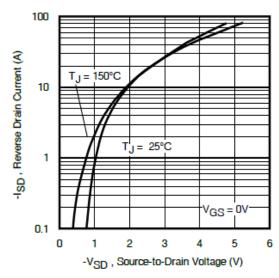
Fig 6. Typical On-Resistance Vs Drain Current



**Fig 7.** Typical Drain-to-Source Breakdown Voltage Vs Temperature



**Fig 9.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 11.** Typical Source-to-Drain Diode Forward Voltage

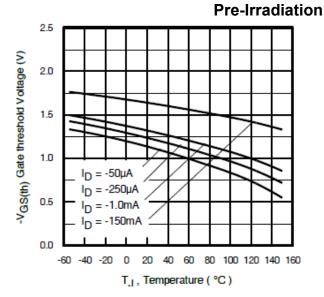
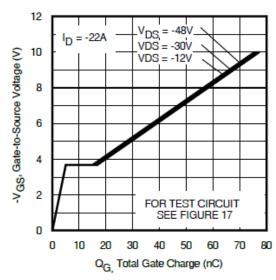
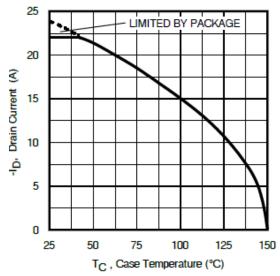


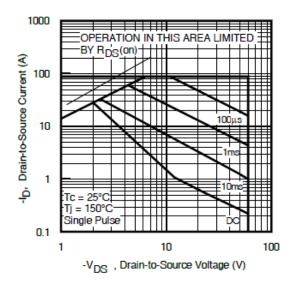
Fig 8. Typical Threshold Voltage Vs Temperature

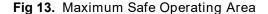


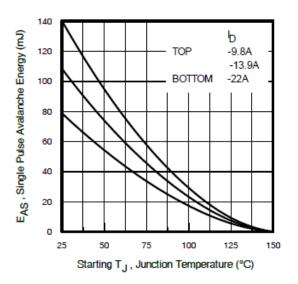
**Fig 10.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 12.** Maximum Drain Current Vs. Case Temperature







**Fig 14.** Maximum Avalanche Energy Vs. Drain Current

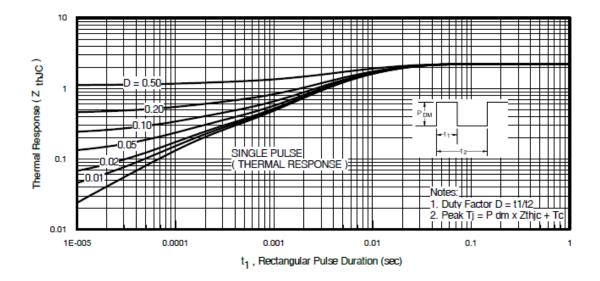


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

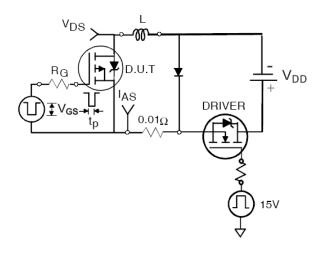


Fig 16a. Unclamped Inductive Test Circuit

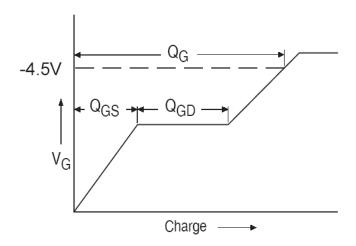


Fig 17a. Basic Gate Charge Waveform

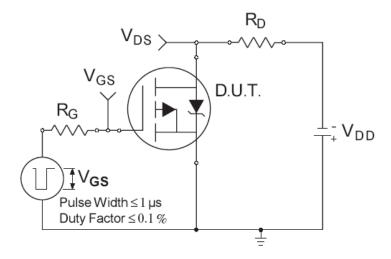


Fig 18a. Switching Time Test Circuit

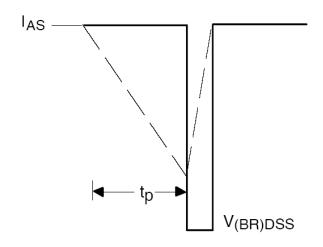


Fig 16b. Unclamped Inductive Wave-

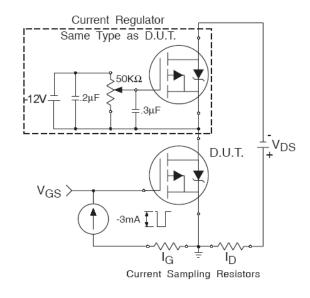


Fig 17b. Gate Charge Test Circuit

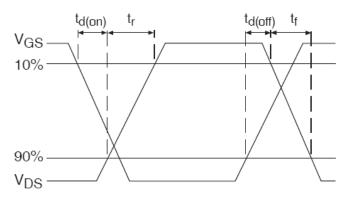
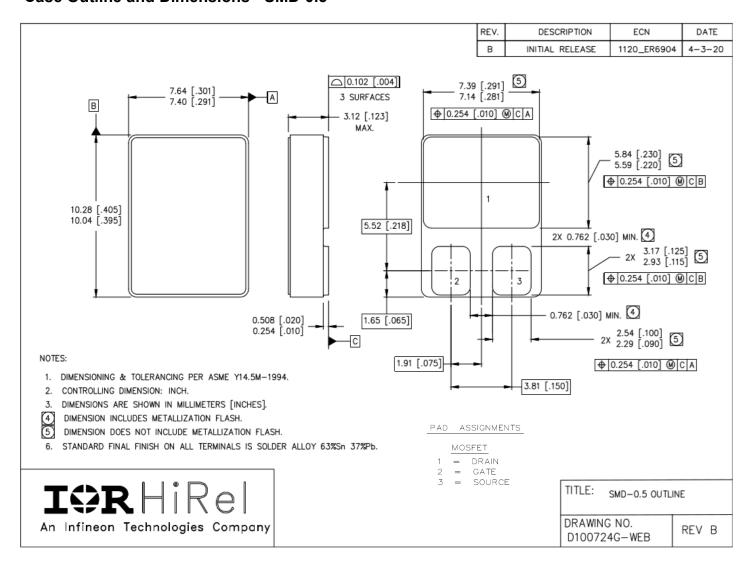


Fig 18b. Switching Time Waveforms



Note: For the most updated package outline, please see the website: <u>SMD - 0.5</u>

#### Case Outline and Dimensions - SMD-0.5





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