

**RADIATION HARDENED
POWER MOSFET
THRU-HOLE (TO-259AA)**

**500V, N-CHANNEL
RAD-Hard HEXFET TECHNOLOGY**

Product Summary

Part Number	Radiation Level	RDS(on)	I _D
IRHI7460SE	100 kRads(Si)	0.32Ω	20A



Description

IRHI7460SE is part of the International Rectifier HiRel family of products. IR HiRel RAD-Hard HEXFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low R_{dson} and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Light Weight
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I _D @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	20	A
I _D @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	12	
I _{DM}	Pulsed Drain Current ①	80	
P _D @T _C = 25°C	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.4	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	500	mJ
I _{AR}	Avalanche Current ①	20	A
E _{AR}	Repetitive Avalanche Energy ①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	10.9 (Typical)	

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.68	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.32	Ω	V _{GS} = 12V, I _D = 12A ④
		—	—	0.36		V _{GS} = 12V, I _D = 20A ④
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
G _{fs}	Forward Transconductance	3.5	—	—	S	V _{DS} = 15V, I _D = 12A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	50	μA	V _{DS} = 400V, V _{GS} = 0V
		—	—	250		V _{DS} = 400V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	260	nC	I _D = 20A
Q _{GS}	Gate-to-Source Charge	—	—	40		V _{DS} = 250V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	200		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time	—	—	45	ns	V _{DD} = 250V
t _r	Rise Time	—	—	140		I _D = 20A
t _{d(off)}	Turn-Off Delay Time	—	—	140		R _G = 2.35Ω
t _f	Fall Time	—	—	110		V _{GS} = 12V
L _S + L _D	Total Inductance	—	8.7	—	nH	Measured from Drain lead (6mm / 0.25in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C _{iss}	Input Capacitance	—	6400	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1100	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	375	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	20	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	80		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _J = 25°C, I _S = 20A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	1200	ns	T _J = 25°C, I _F = 20A, V _{DD} ≤ 50V
Q _{rr}	Reverse Recovery Charge	—	—	16	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	0.42	°C/W
R _{θCS}	Case -to-Sink	—	0.21	—	
R _{θJA}	Junction-to-Ambient (Typical socket mount)	—	—	30	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 50V, starting T_J = 25°C, L = 2.5mH, Peak I_L = 20A, V_{GS} = 12V
- ③ I_{SD} ≤ 20A, di/dt ≤ 170A/μs, V_{DD} ≤ 500V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.** 400 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 100 kRads (Si)		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	$V_{DS} = V_{GS}, I_D = 1.0mA$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	50	μA	$V_{DS} = 400V, V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.32	Ω	$V_{GS} = 12V, I_D = 12A$
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-259AA)	—	0.32	Ω	$V_{GS} = 12V, I_D = 12A$
V_{SD}	Diode Forward Voltage	—	1.8	V	$V_{GS} = 0V, I_D = 20A$

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)				
				@VGS=0V	@VGS=-5V	@VGS=-10V	@VGS=-20V	@VGS=-25V
Cu	28	285	43	375	375	375	375	375
Br	36.8	305	39	350	350	350	325	300
Ni	26.8	265	42	—	375	—	—	—

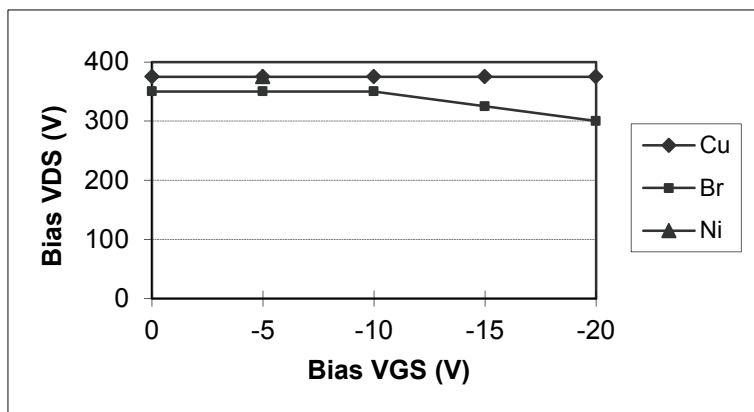


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

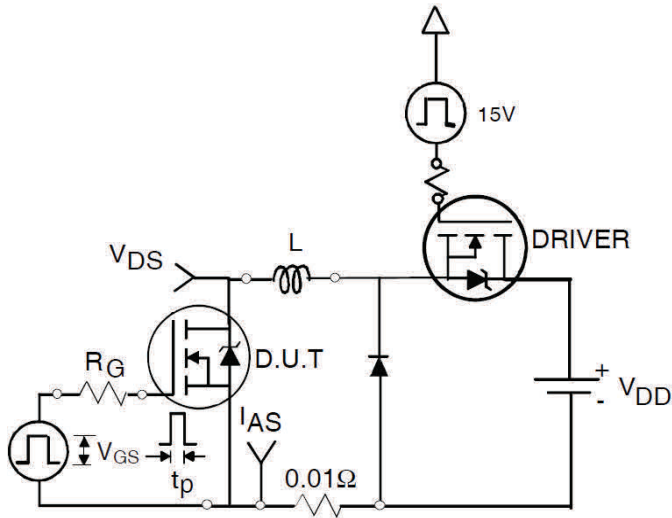


Fig 1a. Unclamped Inductive Test Circuit

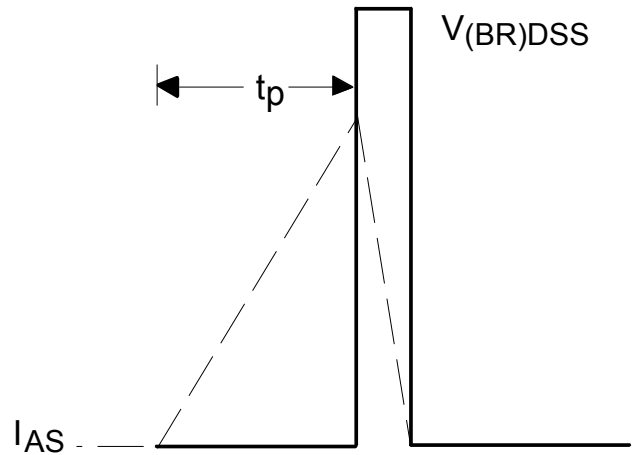


Fig 1b. Unclamped Inductive Waveforms

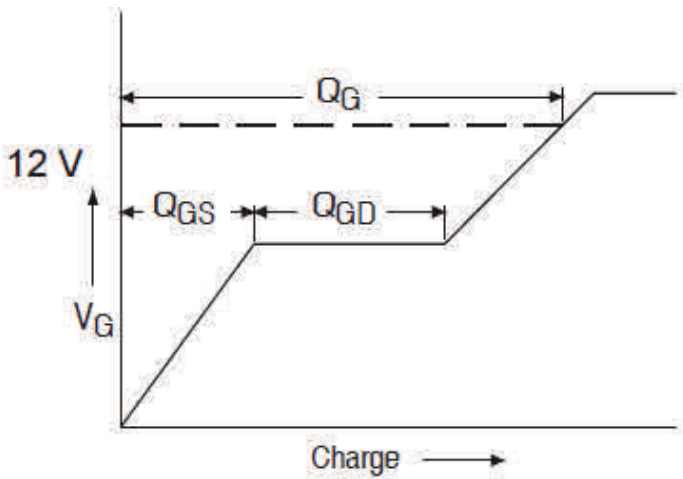


Fig 2a. Gate Charge Waveform

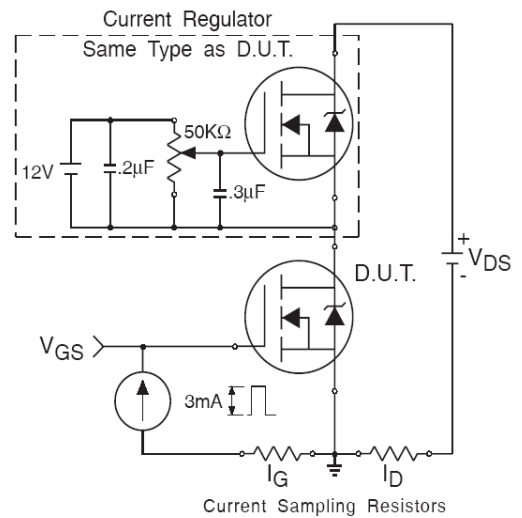


Fig 2b. Gate Charge Test Circuit

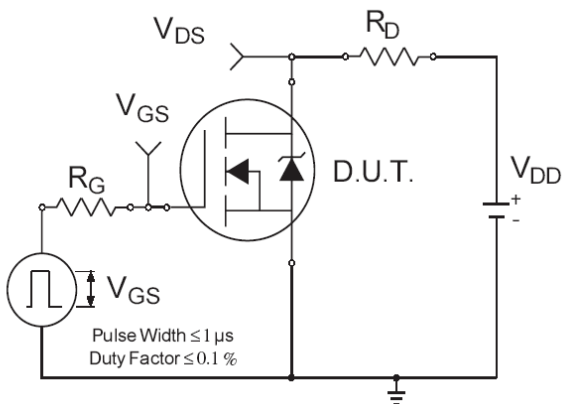


Fig 3a. Switching Time Test Circuit

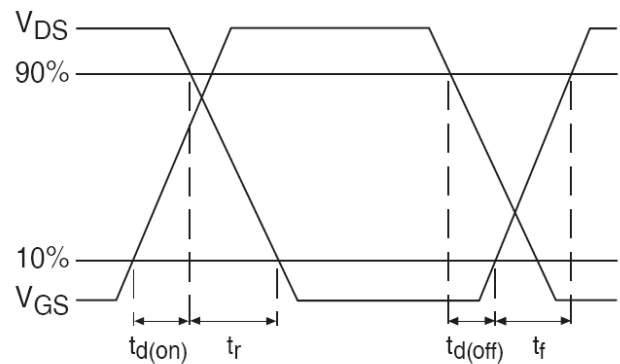
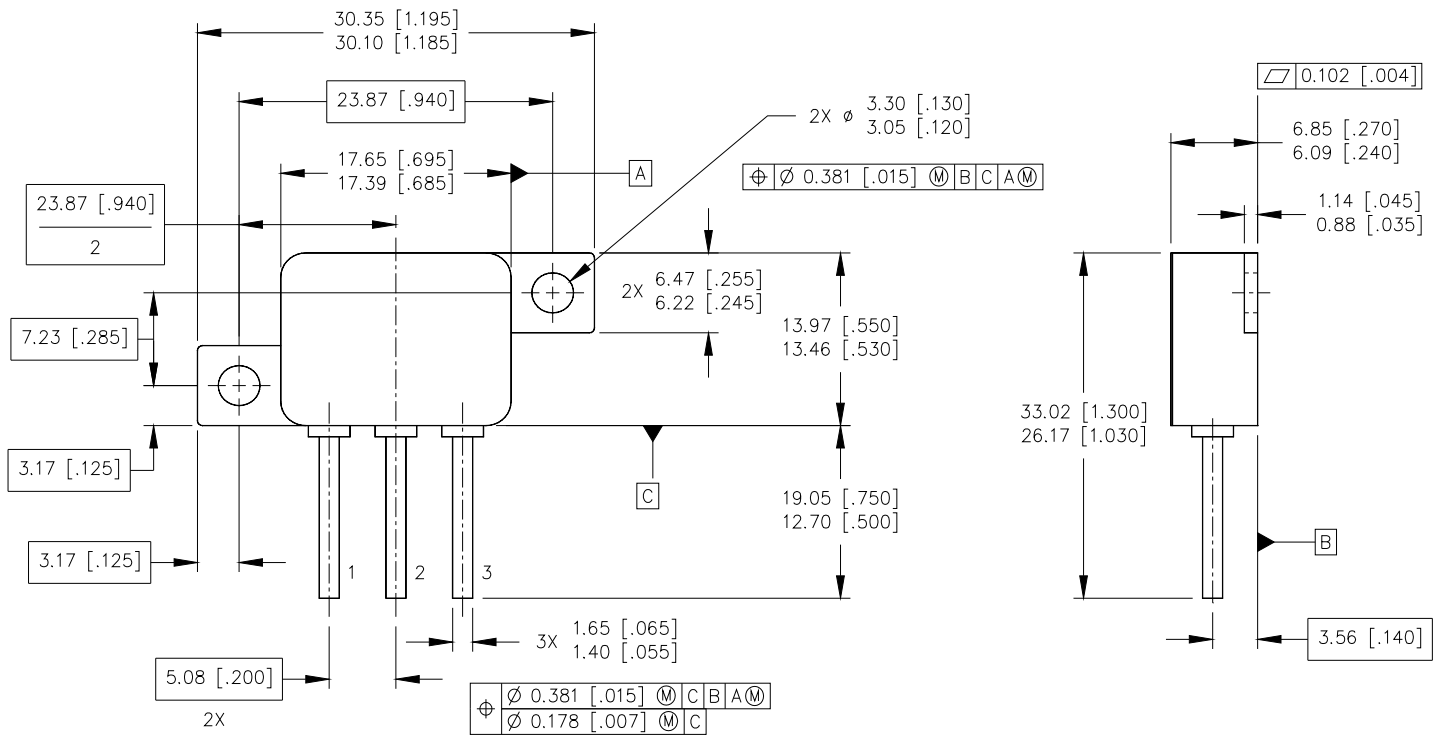


Fig 3b. Switching Time Waveforms

Case Outline and Dimensions — TO-259AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-259AA.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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