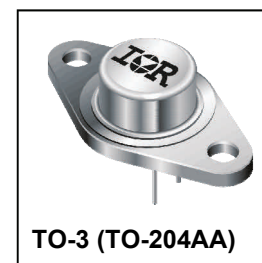


REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS THRU-HOLE (TO-204AA)

800V, N-CHANNEL

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRFAE50	800V	1.2 Ω	7.1A



Description

HEXFET[®] MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest “State of the Art” design achieves: very low on-state resistance combined with high trans conductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Features

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$I_{D1} @ V_{GS} = 10V, T_C = 25^\circ C$	Continuous Drain Current	7.1	A
$I_{D2} @ V_{GS} = 10V, T_C = 100^\circ C$	Continuous Drain Current	4.5	
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current ①	28.4	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	150	W
	Linear Derating Factor	1.2	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	830	mJ
I_{AR}	Avalanche Current ①	7.1	A
E_{AR}	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery ③	2.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	$^\circ C$
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5 (Typical)	

For footnotes refer to the page 2.

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	800	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.98	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	V _{GS} = 10V, I _{D2} = 4.5A ④
		—	—	1.4		V _{GS} = 10V, I _{D1} = 7.1A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 640V, V _{GS} = 0V
		—	—	250		V _{DS} = 640V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	84	—	190	nC	I _{D1} = 7.1A
Q _{GS}	Gate-to-Source Charge	6.6	—	15		V _{DS} = 400V
Q _{GD}	Gate-to-Drain ('Miller') Charge	48	—	110		V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	—	32	ns	V _{DD} = 400V
t _r	Rise Time	—	—	68		I _{D1} = 7.1A
t _{d(off)}	Turn-Off Delay Time	—	—	78		R _G = 2.35Ω
t _f	Fall Time	—	—	24		V _{GS} = 10V
L _S + L _D	Total Inductance	—	6.1	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package)
C _{iss}	Input Capacitance	—	2800	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	400	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	200	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	7.1	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	28.4		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _J = 25°C, I _S = 7.1A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	1600	ns	T _J = 25°C, I _F = 7.1A, V _{DD} ≤ 50V
Q _{rr}	Reverse Recovery Charge	—	—	13	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	0.83	°C/W
R _{θJA}	Junction-to-Ambient (Typical socket mount)	—	—	30	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 50V, starting T_J = 25°C, L = 32.9mH, Peak I_L = 7.1A, V_{GS} = 10V.
- ③ I_{SD} ≤ 7.1A, di/dt ≤ 120A/μs, V_{DD} ≤ 800V, T_J ≤ 150°C. Suggested R_G = 2.35 Ω
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

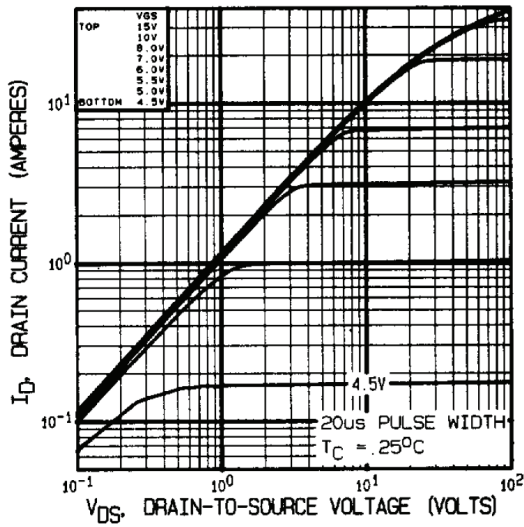


Fig 1. Typical Output Characteristics

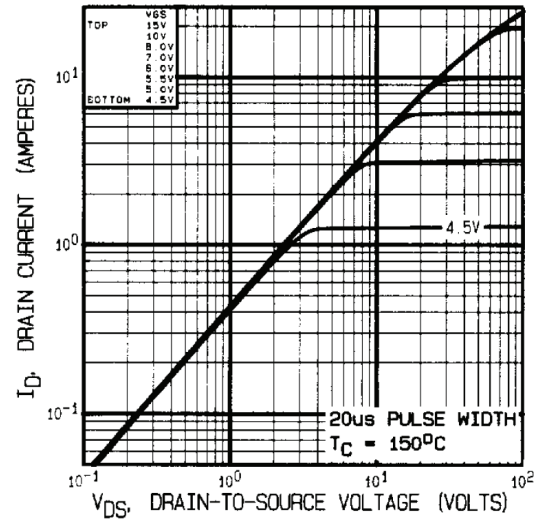


Fig 2. Typical Output Characteristics

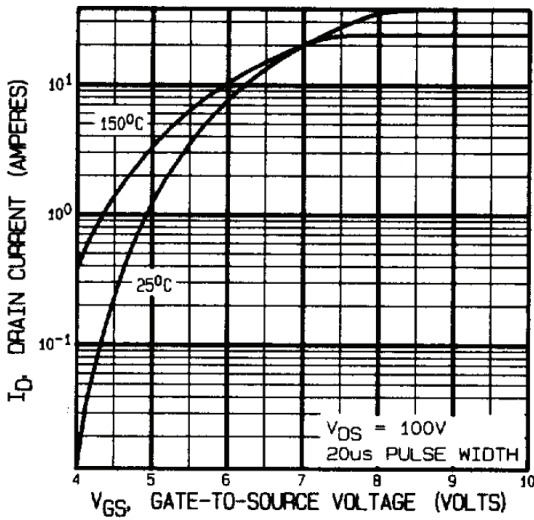


Fig 3. Typical Transfer Characteristics

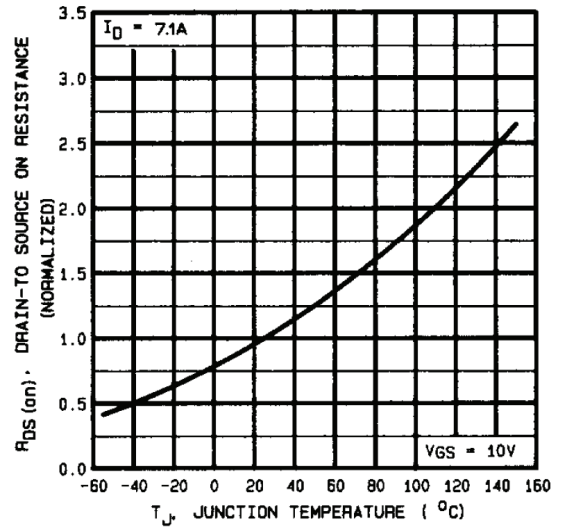


Fig 4. Normalized On-Resistance Vs. Temperature

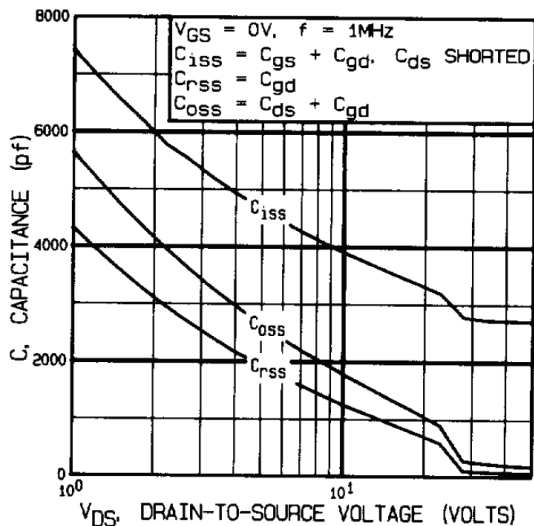


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

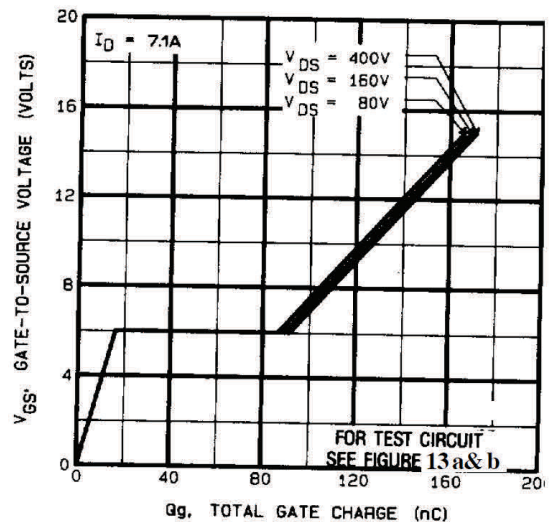


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

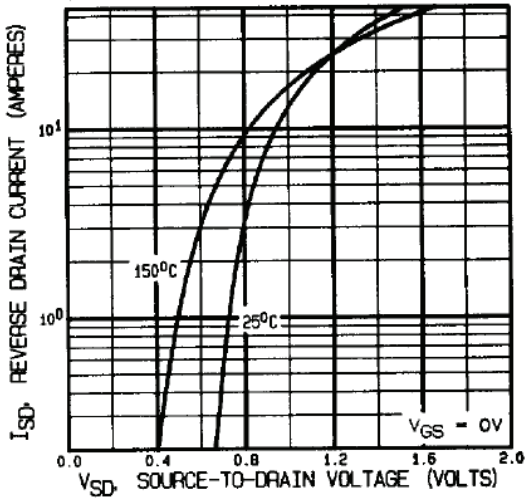


Fig 7. Typical Source-Drain Diode Forward Voltage

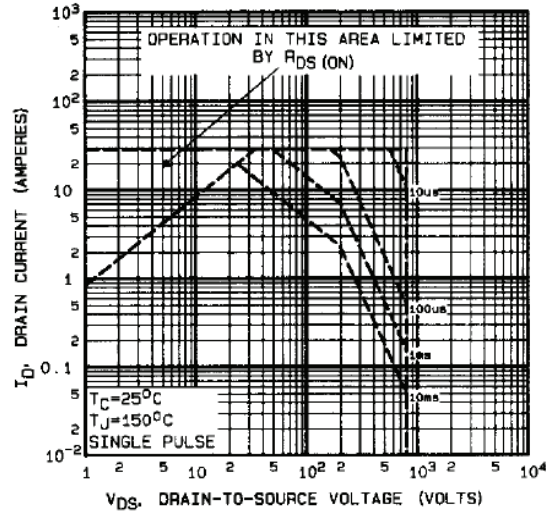


Fig 8. Maximum Safe Operating Area

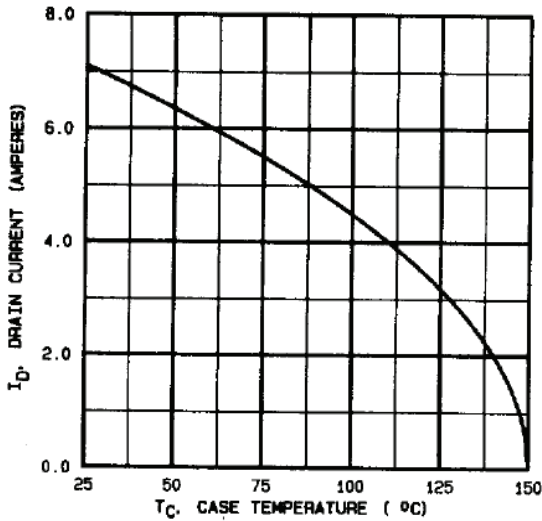


Fig 9. Maximum Drain Current Vs. Case Temperature

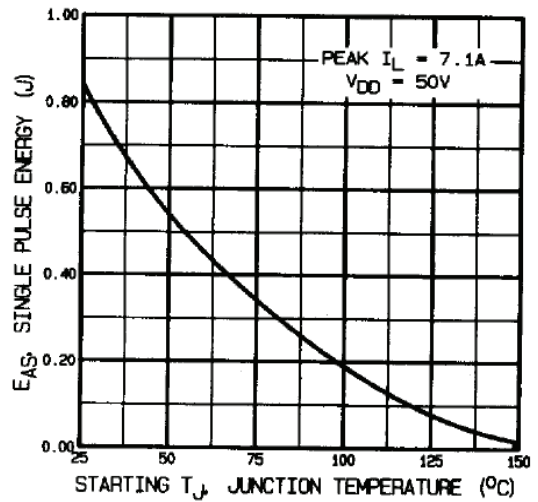


Fig 10. Maximum Avalanche Energy Vs. Drain Current

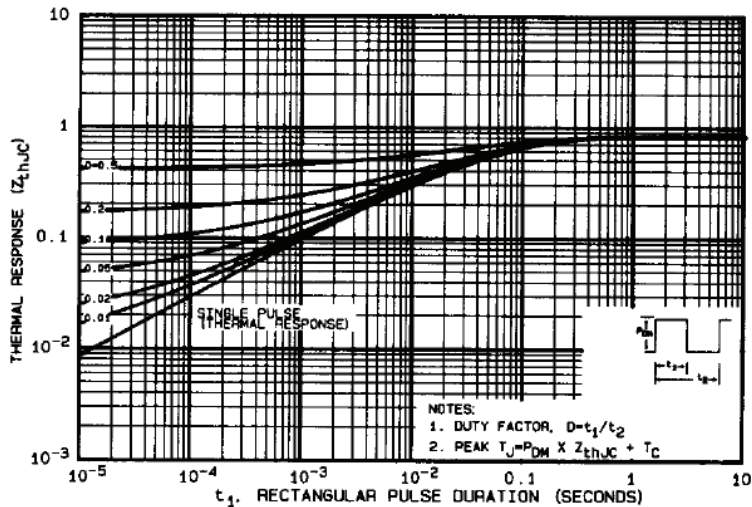


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

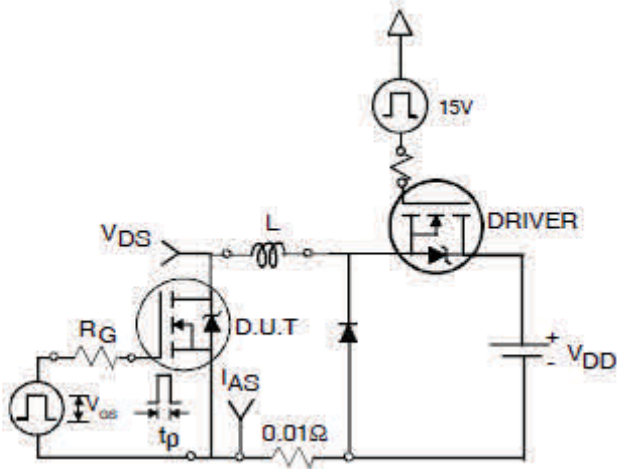


Fig 12a. Unclamped Inductive Test Circuit

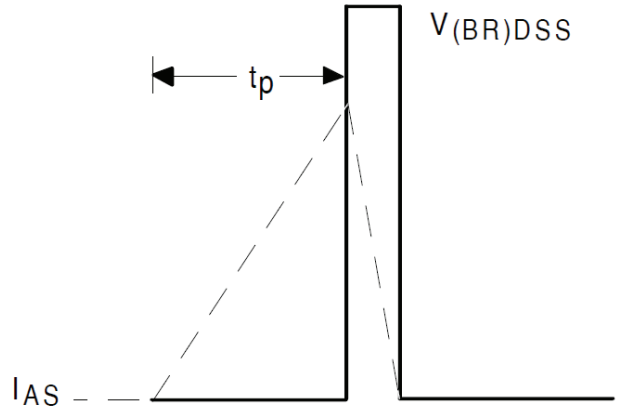


Fig 12b. Unclamped Inductive Waveforms

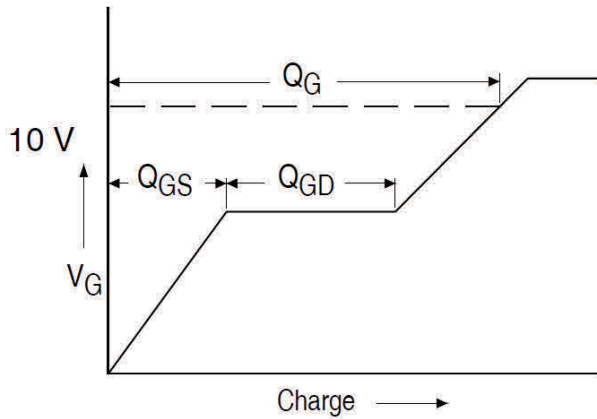


Fig 13a. Gate Charge Waveform

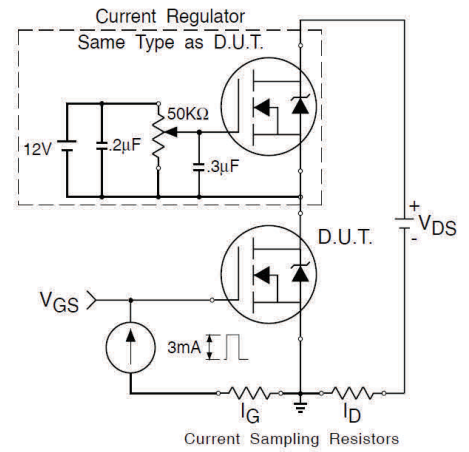


Fig 13b. Gate Charge Test Circuit

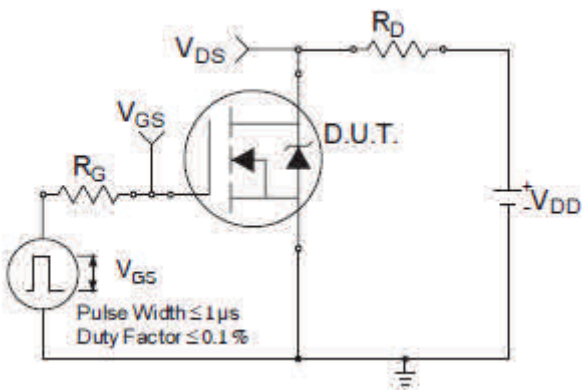


Fig 14a. Switching Time Test Circuit

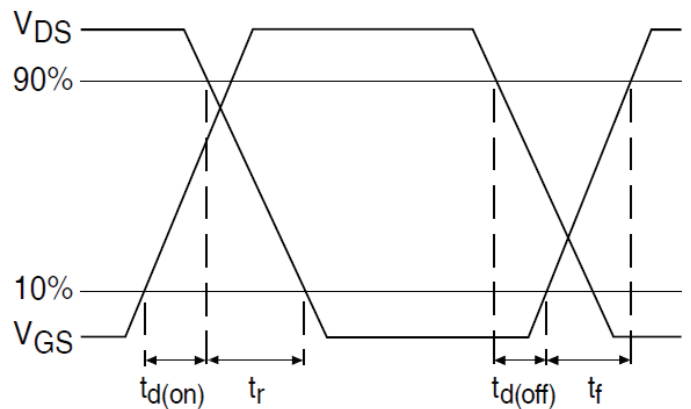
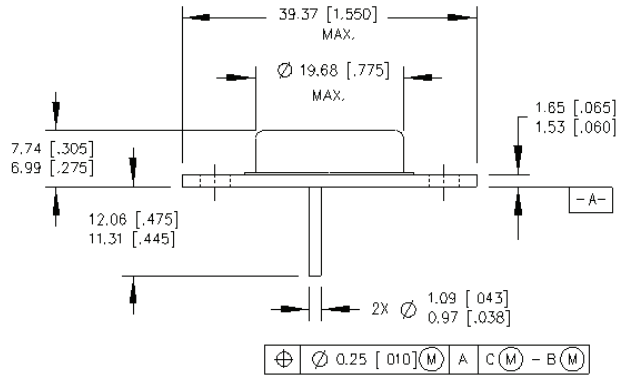


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions - TO-204AA (Modified TO-3)



PIN ASSIGNMENTS

HEXFET

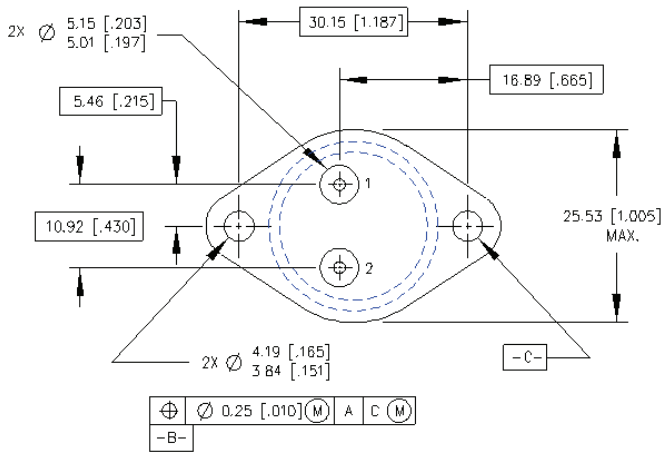
- 1 - SOURCE
- 2 - GATE
- 3 - DRAIN (CASE)

SCHOTTKY

- 1 - ANODE 1
- 2 - ANODE 2
- 3 - COMMON CATHOD (CASE)

IGBT

- 1 - GATE
- 2 - EMITTER
- 3 - COLLECTOR (CASE)



- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
 2. CONTROLLING DIMENSION : INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 4. OUTLINE CONFORMS TO JEDEC OUTLINE TO -204-AA.

IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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