IR HiRel
An Infineon Technologies Company

IRF5M3205

POWER MOSFET
THRU-HOLE (TO-254AA)

55V, N-CHANNEL
HEXFET® MOSFET TECHNOLOGY

Product Summary

Part Number	BV_{DSS}	RDS(on)	I_D
IRF5M3205	55V	0.015Ω	35A*


TO-254AA

Description

Fifth Generation HEXFET® power MOSFET technology is the key to IR Hirel utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.
These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.

Features

- Low RDS(on)
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Hermetically Sealed
- Light Weight

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	35*	A
I_{D2} @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	35*	
I_{DM} @T_C = 25°C	Pulsed Drain Current ①	140	
P_D @T_C = 25°C	Maximum Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	475	mJ
I_{AR}	Avalanche Current ①	35	A
E_{AR}	Repetitive Avalanche Energy ①	12.5	mJ
dv/dt	Peak Diode Recovery ③	2.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063in./1.6mm from case for 10s)	
	Weight	9.3 (Typical)	g

*Current is limited by package
For footnotes refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.056	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.015	Ω	V_{GS} = 10V, I_{D2} = 35A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
Gfs	Forward Transconductance	34	—	—	S	V_{DS} = 15V, I_{D2} = 35A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	170	nC	I_{D1} = 35A
Q_{GS}	Gate-to-Source Charge	—	—	32		V_{DS} = 44V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	74		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	—	—	22	ns	V_{DD} = 28V
tr	Rise Time	—	—	80		I_{D1} = 35A
$t_{d(off)}$	Turn-Off Delay Time	—	—	70		R_G = 2.5Ω
t_f	Fall Time	—	—	55		V_{GS} = 10V
Ls +L_D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package)
C_{iss}	Input Capacitance	—	3600	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1200	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	445	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	35*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	140		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 35A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	—	130	ns	T_J = 25°C ,I_F = 35A,V_{DD} ≤ 25V
Q_{rr}	Reverse Recovery Charge	—	—	410	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = 25V, starting T_J = 25°C, L = 0.8mH, Peak I_L = 35A, V_{GS} = 10V, R_G =25Ω.
③ I_{SD} ≤ 35A, di/dt ≤ 230A/µs, V_{DD} ≤ 55V, T_J ≤ 150°C.
④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

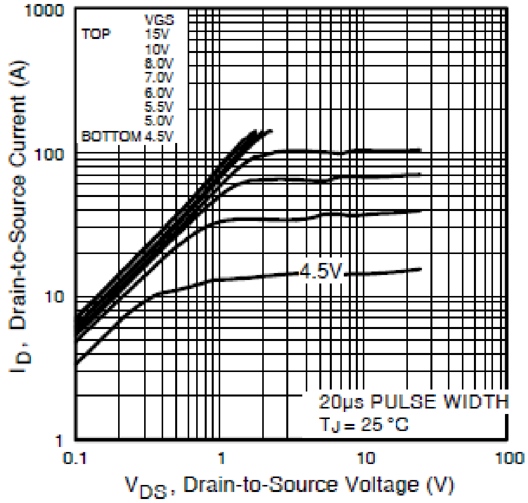


Fig 1. Typical Output Characteristics

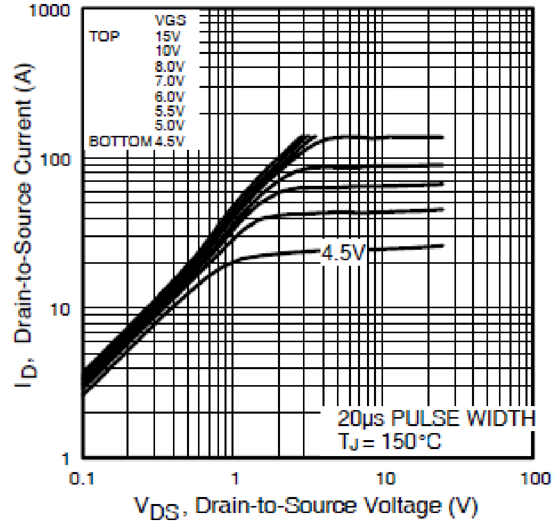


Fig 2. Typical Output Characteristics

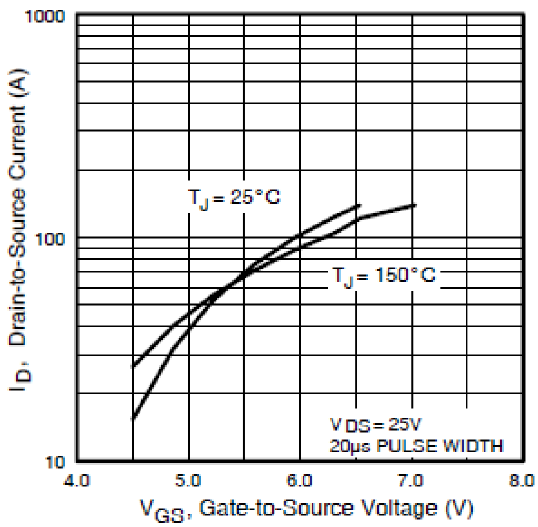


Fig 3. Typical Transfer Characteristics

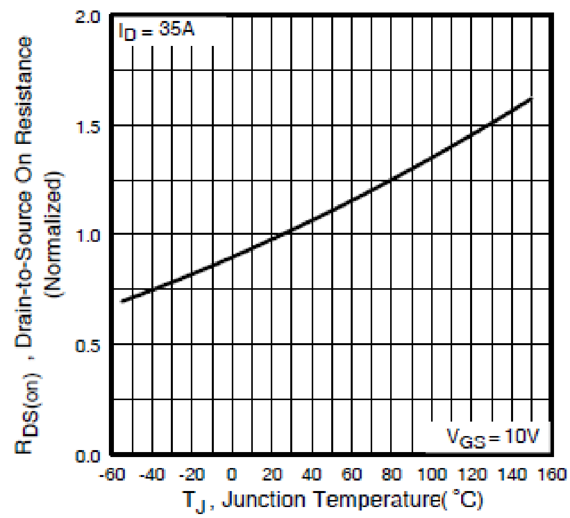


Fig 4. Normalized On-Resistance Vs. Temperature

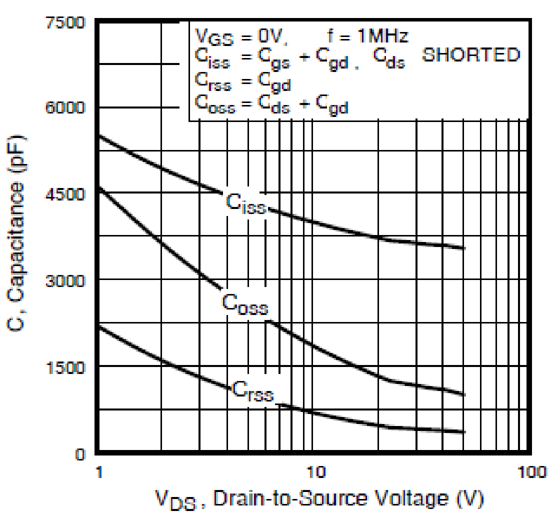


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

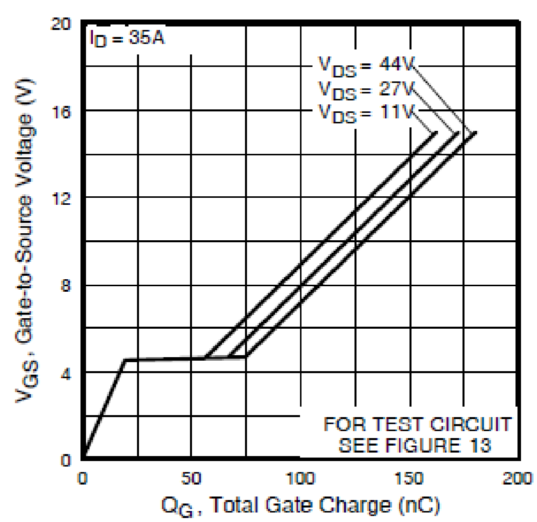


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

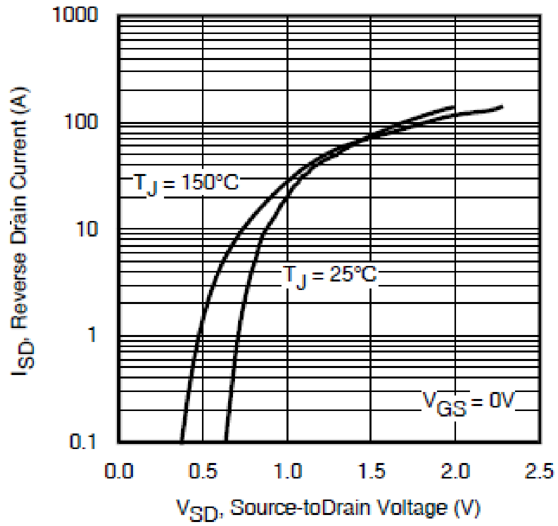


Fig 7. Typical Source-Drain Diode Forward Voltage

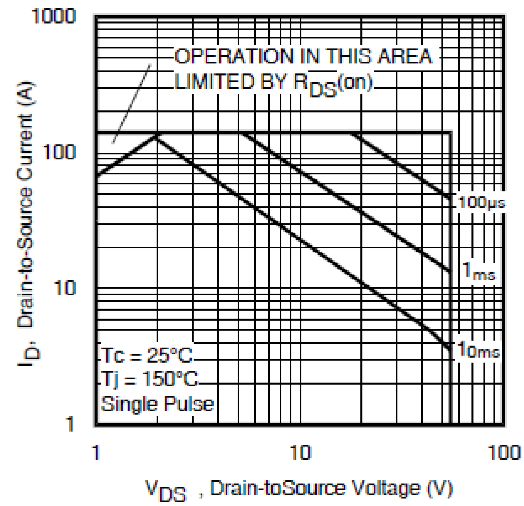


Fig 8. Maximum Safe Operating Area

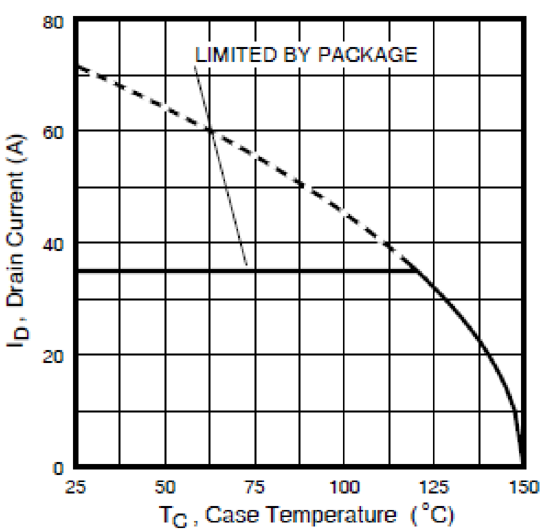


Fig 9. Maximum Drain Current Vs.Case Temperature

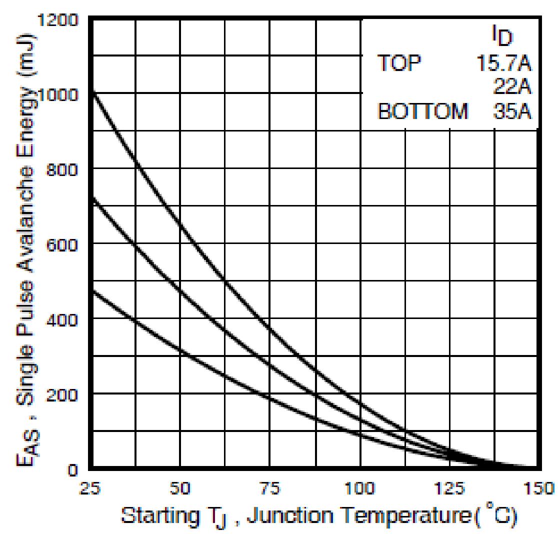


Fig 10. Maximum Avalanche Energy Vs. Drain Current

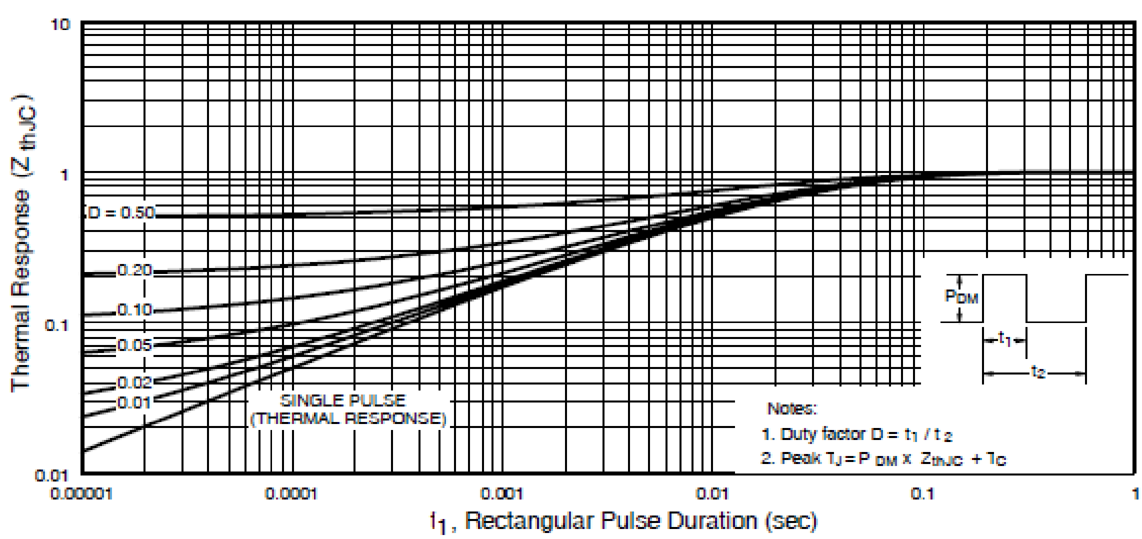


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

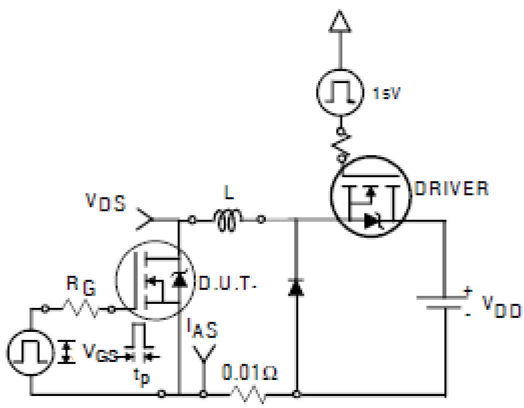


Fig 12a. Unclamped Inductive Test Circuit

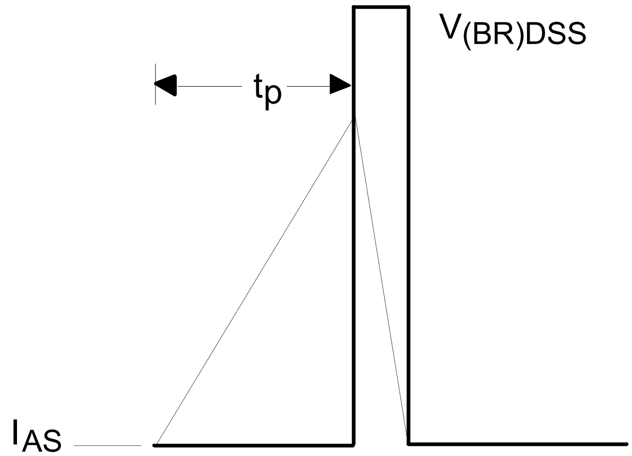


Fig 12b. Unclamped Inductive Waveforms

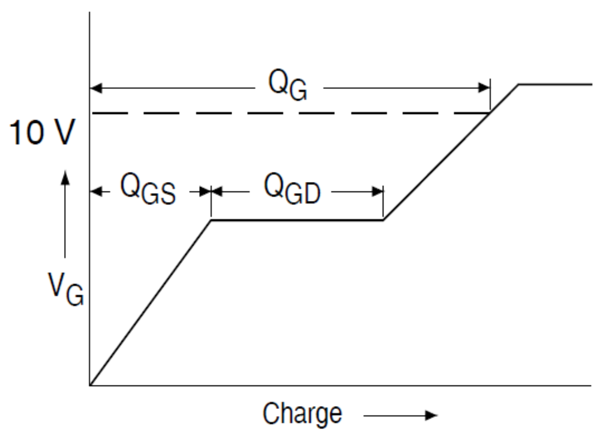


Fig 13a. Gate Charge Waveform

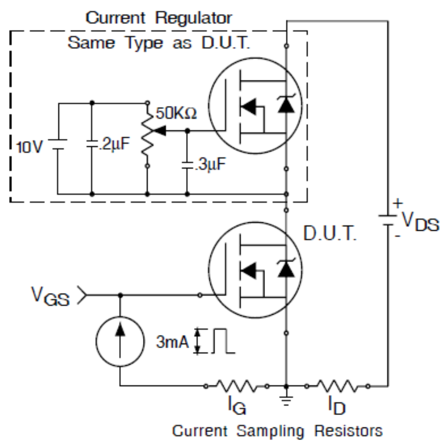


Fig 13b. Gate Charge Test Circuit

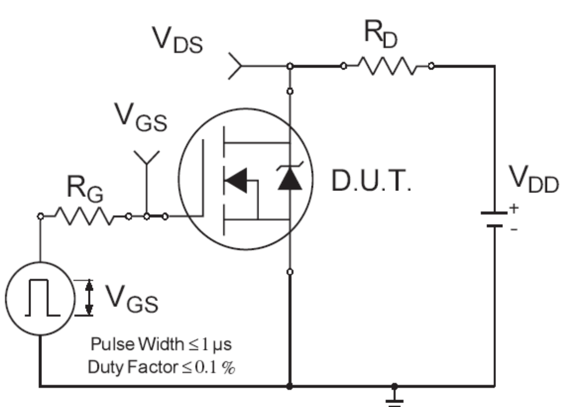


Fig 14a. Switching Time Test Circuit

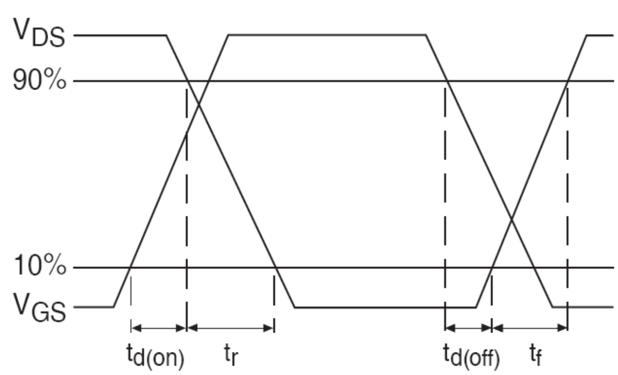
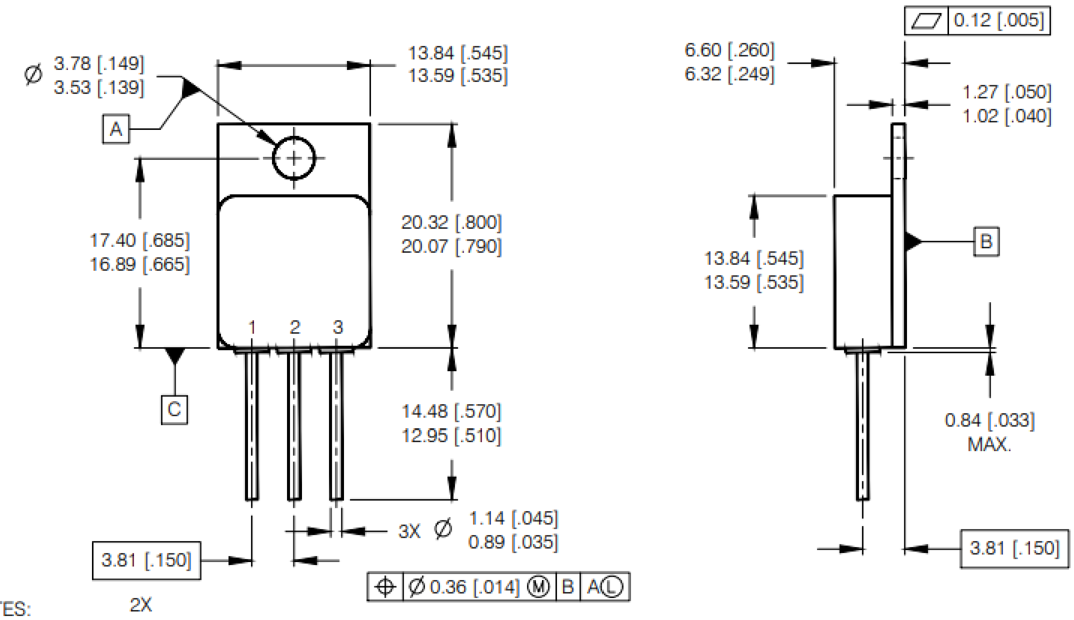


Fig 14b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [TO-254AA](TO-254AA)

Case Outline and Dimensions - Low-Ohmic TO-254AA

REV.	DESCRIPTION	ECN	DATE
A	INITIAL RELEASE	1120_ER6904	4-3-20



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.
5. FINAL LEAD FINISH IS SOLDER ALLOY 63%Sn 37%Pb.
6. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

LEGEND
1- DRAIN
2- SOURCE
3- GATE

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TITLE: TO-254AA PACKAGE OUTLINE (STD & LOW OHMIC)
DRAWING NO. D100720G-WEB
REV A

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

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