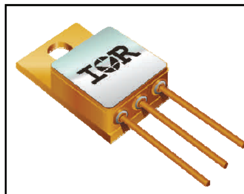
IR HiRel
An Infineon Technologies Company

PD-97842A

IRF3CMS17N80

POWER MOSFET
THRU-HOLE (Low-Ohmic TO-254AA)

800V, N-CHANNEL



Low-Ohmic
TO-254AA

Product Summary

Part Number	$R_{DS(on)}$	I_D
IRF3CMS17N80	0.34Ω	15A

Description

The MOSFET uses Infineon 800V C3 CoolMOS™ advanced technology to deliver high performance with low R_{DS}(on) and fast switching in a low ohmic hermetic package. The 800V C3 CoolMOS™ technology uses proven Super Junction design and is implemented with ease of use in mind.

Features

- New Revolutionary High Voltage Technology
- Extreme dv/dt Rated
- High Peak Current Capability
- Ultra Low Gate Charge
- Ultra Low Effective Capacitance
- Ceramic Eyelets
- Electrically Isolated
- Light Weight
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	15	A
I_{D2} @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	10	
I_{DM} @T_C = 25°C	Pulsed Drain Current ①	60	
P_D @T_C = 25°C	Maximum Power Dissipation	200	W
	Linear Derating Factor	1.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	196	mJ
I_{AR}	Avalanche Current ①	15	A
E_{AR}	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery ③	14	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	g

For footnotes refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	800	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.87	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.34	Ω	V_{GS} = 10V, I_{D2} = 10A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-7.6	—	mV/°C	
Gfs	Forward Transconductance	9.3	—	—	S	V_{DS} = 15V, I_{D2} = 10A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V_{DS} = 800V, V_{GS} = 0V
		—	—	25		V_{DS} = 800V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	135	nC	I_{D1} = 15A
Q_{GS}	Gate-to-Source Charge	—	—	20		V_{DS} = 400V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	60		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	—	—	18	ns	V_{DD} = 400V
tr	Rise Time	—	—	26		I_{D1} = 15A
$t_{d(off)}$	Turn-Off Delay Time	—	—	83		R_G = 2.4Ω
t_f	Fall Time	—	—	23		V_{GS} = 10V
Ls +L_D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package)
C_{iss}	Input Capacitance	—	2300	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	100	—		V_{DS} = 100V
C_{rss}	Reverse Transfer Capacitance	—	3.3	—		f = 1.0MHz
R_G	Gate Resistance	—	1.0	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	15	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	60		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 15A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	—	990	ns	T_J = 25°C, I_F = 15A, V_{DD} ≤ 50V
Q_{rr}	Reverse Recovery Charge	—	—	24	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.63	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical Socket Mount)	—	—	48	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 150V, starting T_J = 25°C, L = 1.7mH, Peak I_L = 15A, R_G = 25Ω, V_{GS} = 20V.

③ I_{SD} ≤ 15A, di/dt ≤ 2060A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C.

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

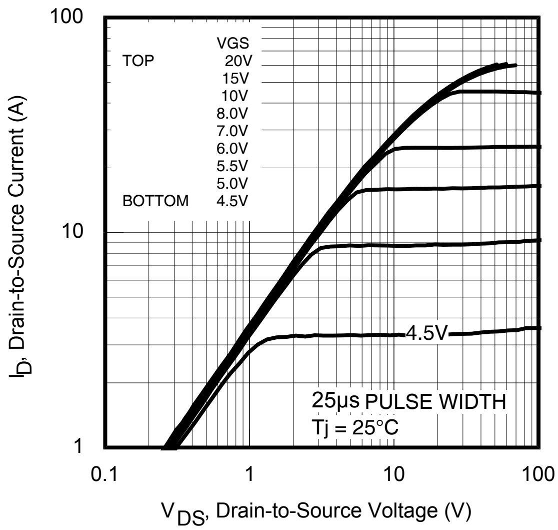


Fig 1. Typical Output Characteristics

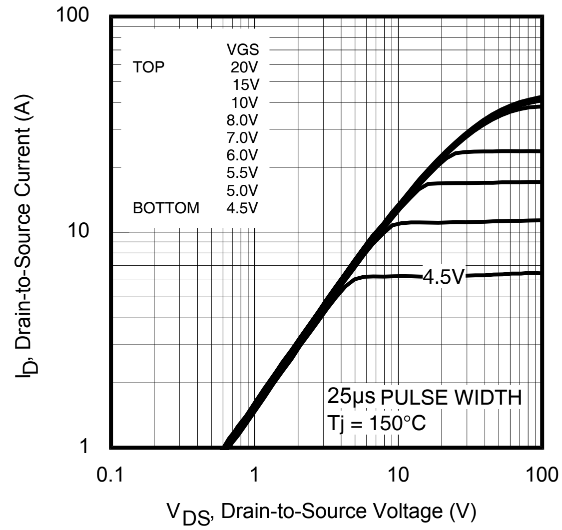


Fig 2. Typical Output Characteristics

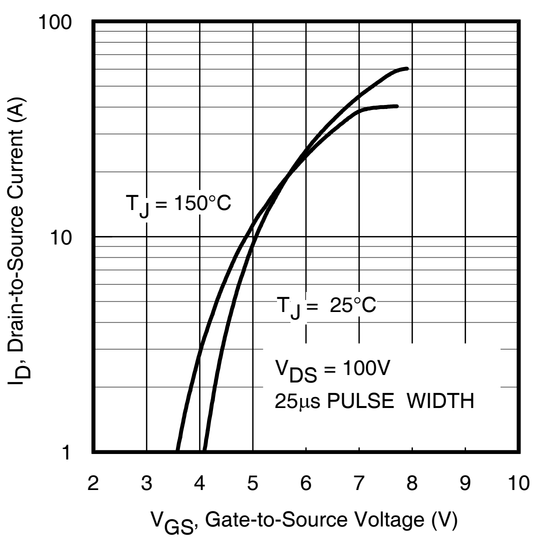


Fig 3. Typical Transfer Characteristics

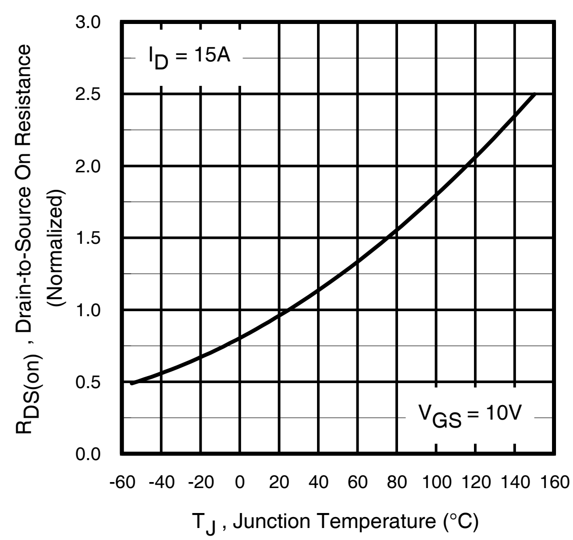


Fig 4. Normalized On-Resistance Vs. Temperature

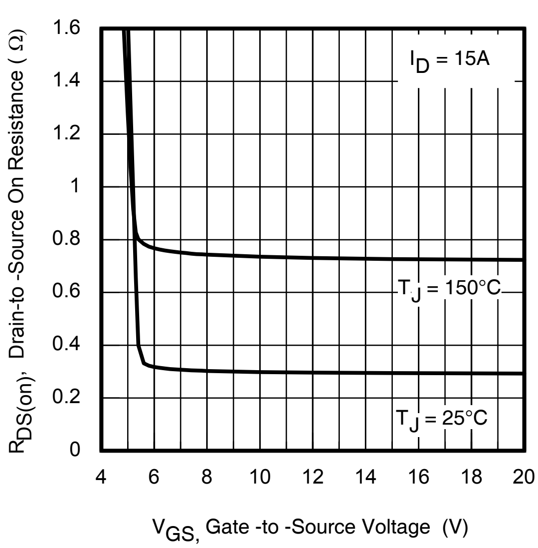


Fig 5. Typical On-Resistance Vs Gate Voltage

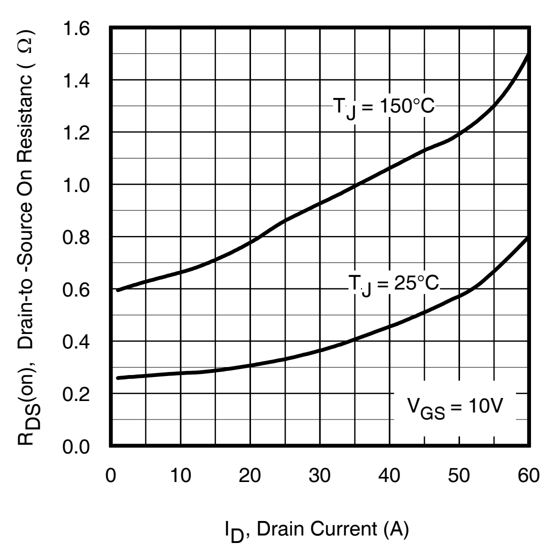


Fig 6. Typical On-Resistance Vs Drain Current

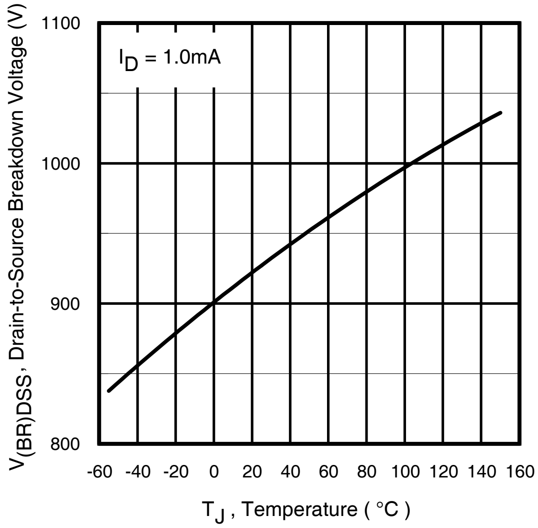


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

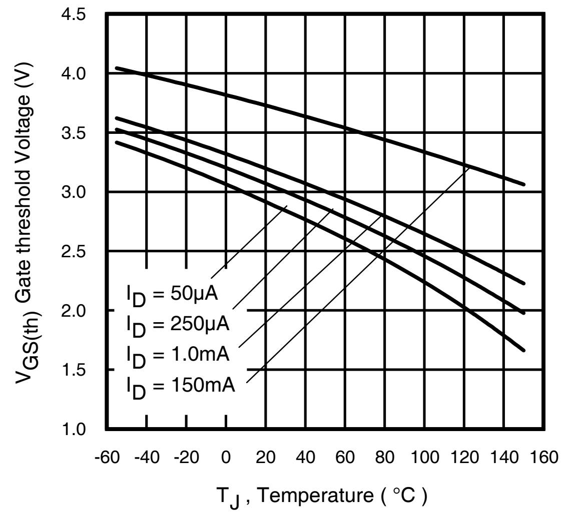


Fig 8. Typical Threshold Voltage Vs Temperature

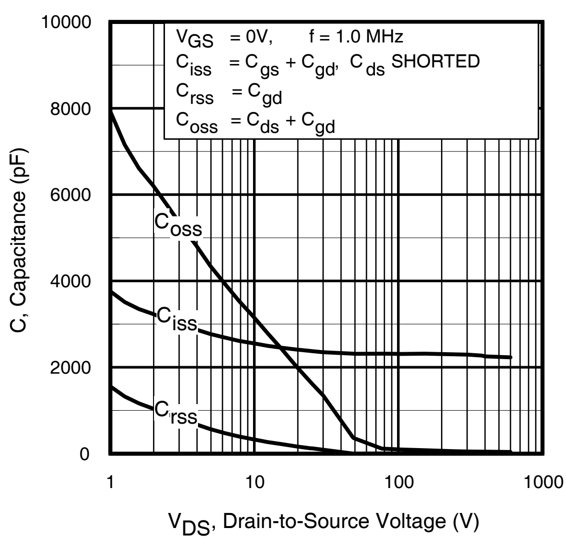


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

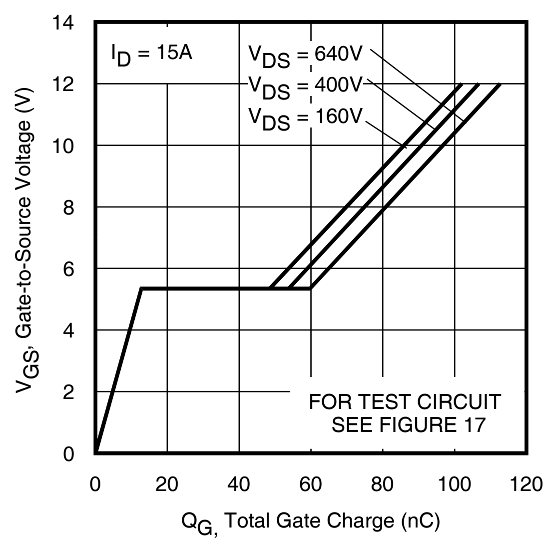


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

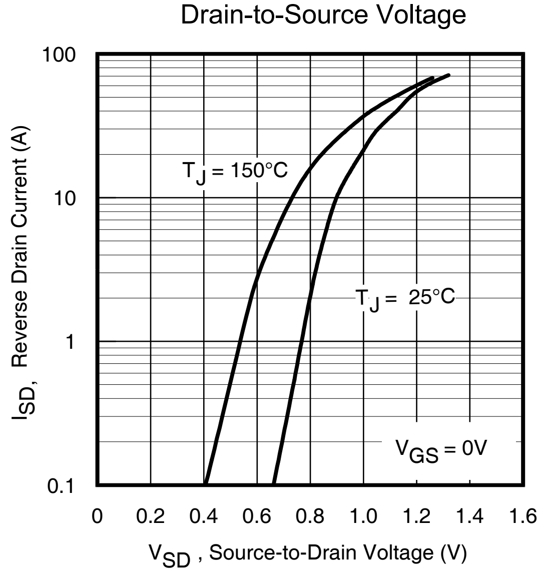


Fig 11. Typical Source-Drain Diode Forward Voltage

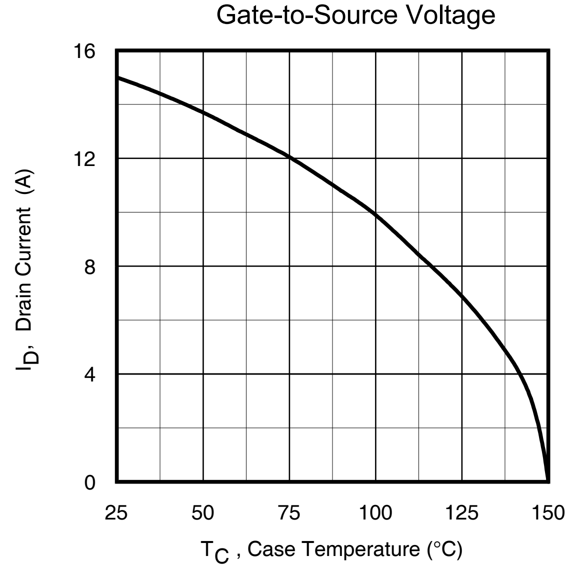


Fig 12. Maximum Drain Current Vs.Case Temperature

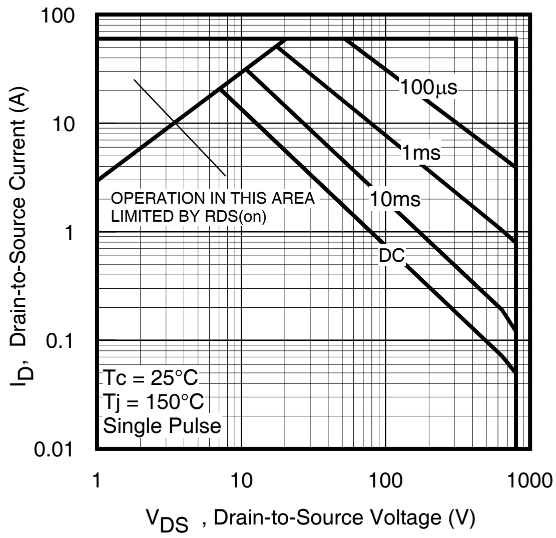


Fig 13. Maximum Safe Operating Area

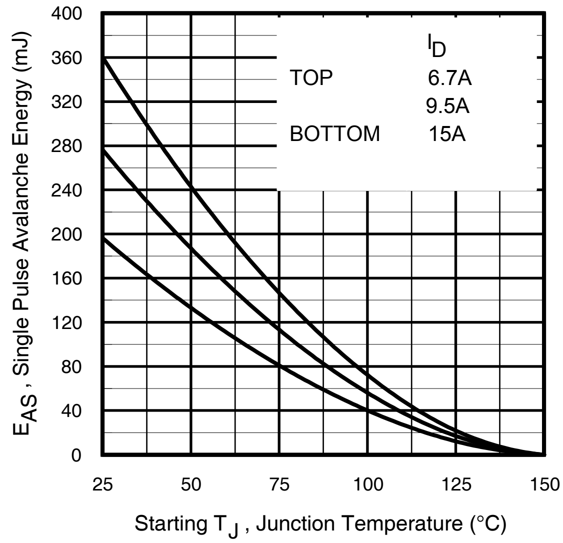


Fig 14. Maximum Avalanche Energy Vs. Drain Current

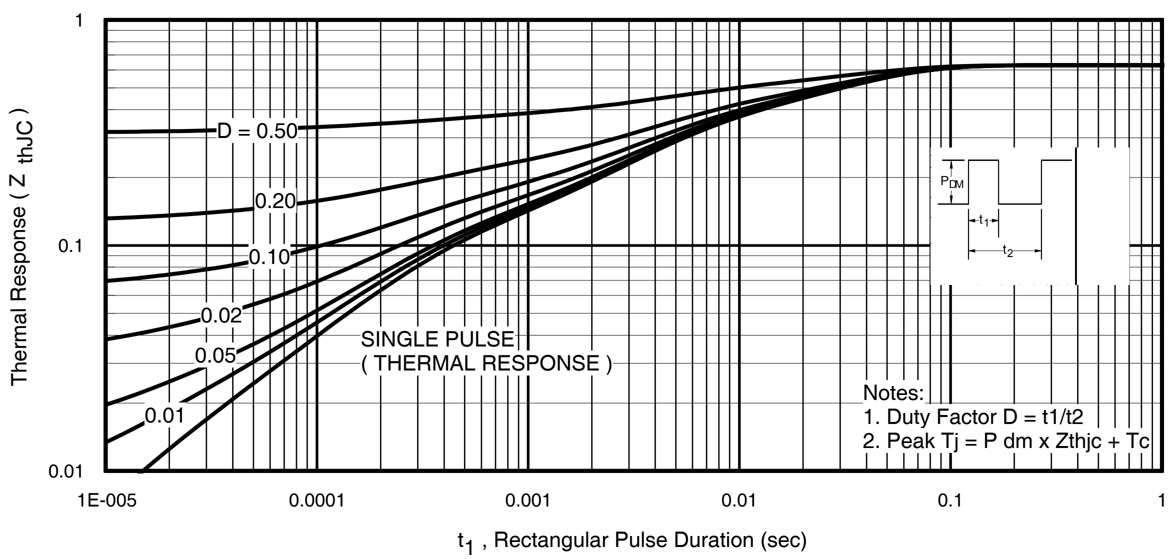


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

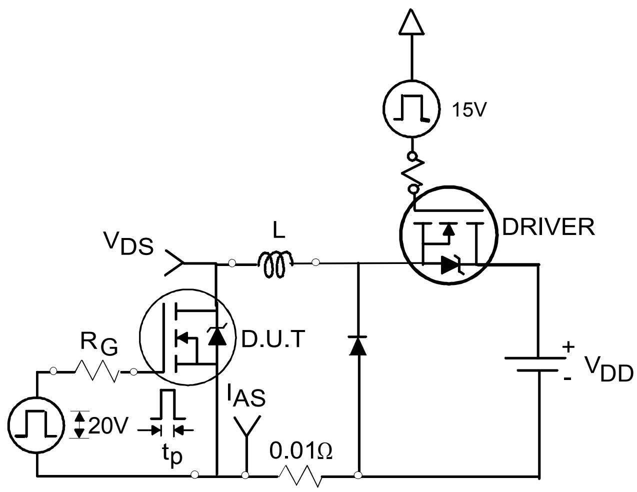


Fig 16a. Unclamped Inductive Test Circuit

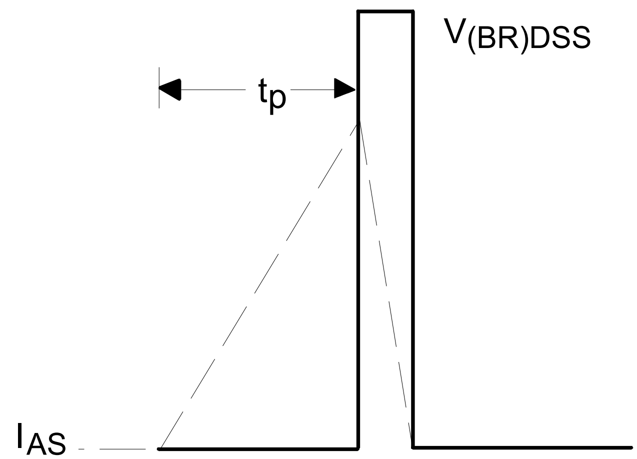


Fig 16b. Unclamped Inductive Waveforms

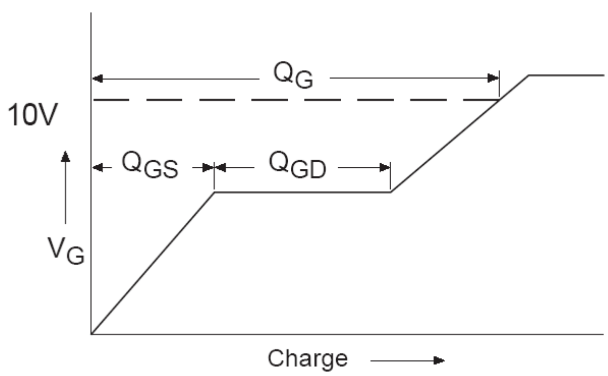


Fig 17a. Gate Charge Waveform

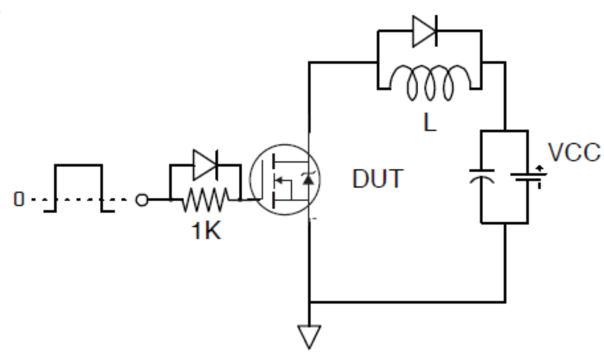


Fig 17b. Gate Charge Test Circuit

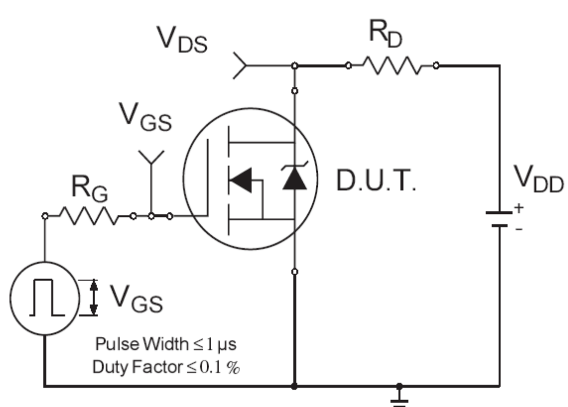


Fig 18a. Switching Time Test Circuit

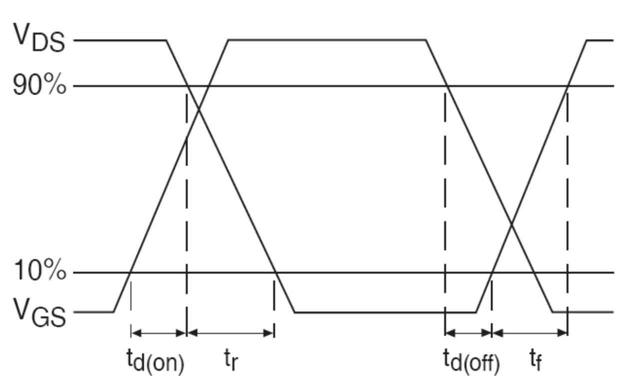
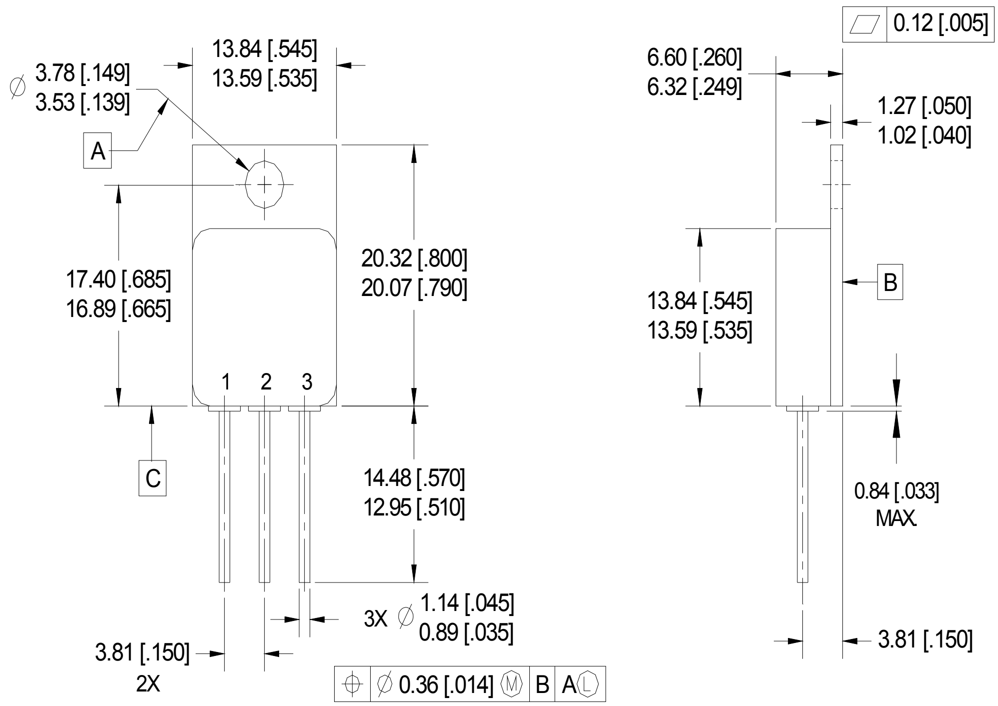


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions - Low-Ohmic TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

1 = DRAIN
2 = SOURCE
3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

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