An Infineon Technologies Company

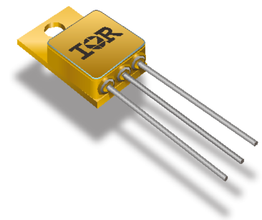
IRHYS67234CM
JANSR2N7594T3

250V, N-CHANNEL
REF: MIL-PRF-19500/755
R6 TECHNOLOGY

RADIATION HARDENED POWER MOSFET THRU-HOLE (Low –Ohmic TO-257AA)

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHYS67234CM	100K Rads (Si)	0.22Ω	12A	JANSR2N7594T3
IRHYS63234CM	300K Rads (Si)	0.22Ω	12A	JANSF2N7594T3



Low-Ohmic
TO-257AA

Description

IR HiRel R6 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 90MeV/(mg/cm^2). Their combination of very low $R_{DS(on)}$ and faster switching times reduces power loss and increases power density in today's high speed switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, ease of paralleling and temperature stability of electrical parameters.

Features

- Low $R_{DS(on)}$
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Eyelets
- Electrically Isolated
- Light Weight
- ESD Rating: Class 2 per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	12	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	7.6	
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	48	
P_D @T_C = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	80	mJ
I_{AR}	Avalanche Current ①	12	A
E_{AR}	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.2	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Pckg. Mounting Surface Temp.	300 (0.063 in. / 1.6mm from case for 10s)	
	Weight	4.3 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.22	Ω	V_{GS} = 12V, I_{D2} = 7.6A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10.2	—	mV/°C	
Gfs	Forward Transconductance	8.6	—	—	S	V_{DS} = 15V, I_{D2} = 7.6A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	25		V_{DS} = 200V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	40	nC	I_{D1} = 12A
Q_{GS}	Gate-to-Source Charge	—	—	12		V_{DS} = 125V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	17		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	19	ns	V_{DD} = 125V
tr	Rise Time	—	—	27		I_{D1} = 12A
$t_{d(off)}$	Turn-Off Delay Time	—	—	36		R_G = 7.5Ω
t_f	Fall Time	—	—	20		V_{GS} = 12V
Ls +L_D	Total Inductance	—	6.8	—	nH	Measured from Drain lead(6mm / 0.25 in from package)to Source lead (6mm/ 0.25 in from package)
C_{iss}	Input Capacitance	—	1420	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	184	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	2.2	—		f = 1.0MHz
R_G	Gate Resistance	—	9.8	—	Ω	f = 1.0MHz,open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	12	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	48		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 12A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	281	450	ns	T_J = 25°C, I_F = 12A, V_{DD} ≤ 50V
Q_{rr}	Reverse Recovery Charge	—	—	5.0	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical Socket Mount)	—	—	80	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L = 1.1mH, Peak I_L = 12A, V_{GS} = 12V

③ I_{SD} ≤ 12A, di/dt ≤ 508A/µs, V_{DD} ≤ 250V, T_J ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ Total Dose Irradiation with V_{DS} Bias. 200 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si)[1]		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	10	µA	V_{DS} = 200V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.24	Ω	V_{GS} = 12V, I_{D2} = 7.6A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-257AA)	——	0.22	Ω	V_{GS} = 12V, I_{D2} = 7.6A
V_{SD}	Diode Forward Voltage ④	——	1.2	V	V_{GS} = 0V, I_S = 12A

[1] Part numbers IRHYS67234CM (JANSR2N7594T3) and IRHYS63234CM (JANSF2N7594T3)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V)				
			@VGS = 0V	@VGS = -5V	@VGS = -10V	@VGS = -15V	@VGS = -20V
44 ± 5%	1350 ± 5%	125 ± 5%	250	250	250	250	40
61 ± 5%	825 ± 5%	66 ± 5%	250	250	250	50	——
90 ± 5%	1470 ± 5%	80 ± 5%	75	75	——	——	——

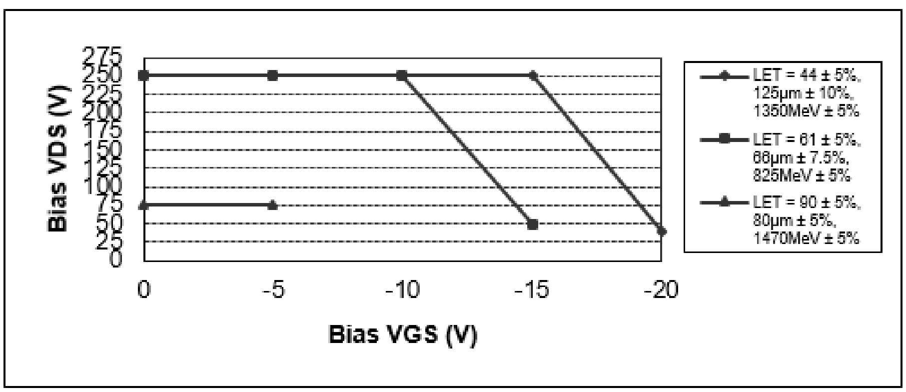


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

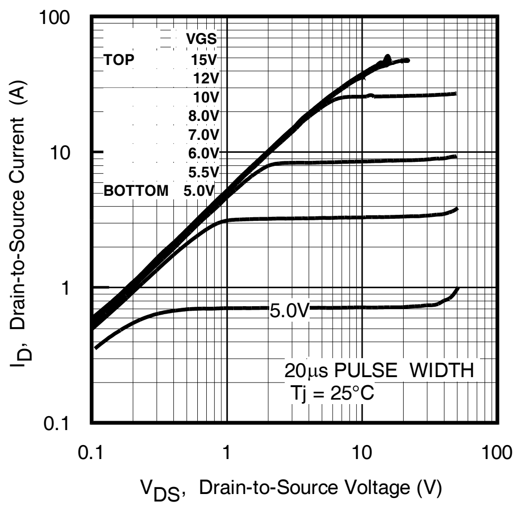


Fig 1. Typical Output Characteristics

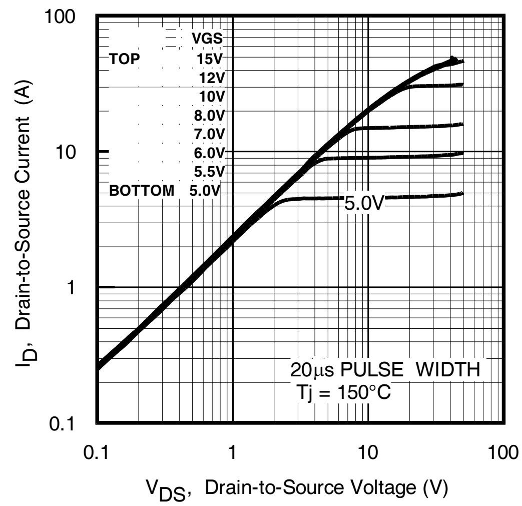


Fig 2. Typical Output Characteristics

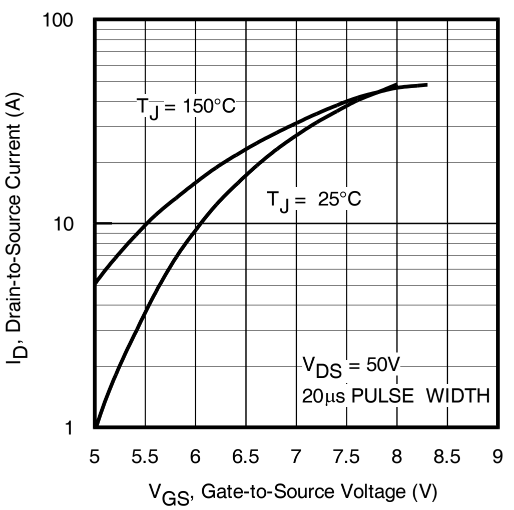


Fig 3. Typical Transfer Characteristics

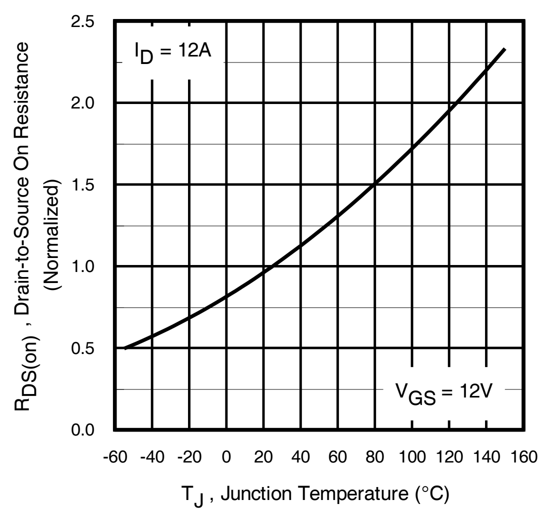


Fig 4. Normalized On-Resistance Vs. Temperature

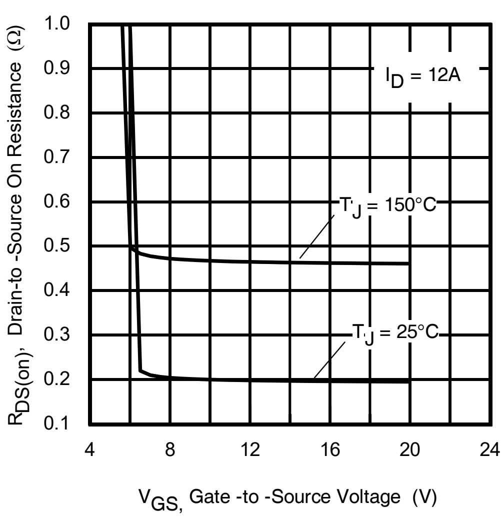


Fig 5. Typical On-Resistance Vs Gate Voltage

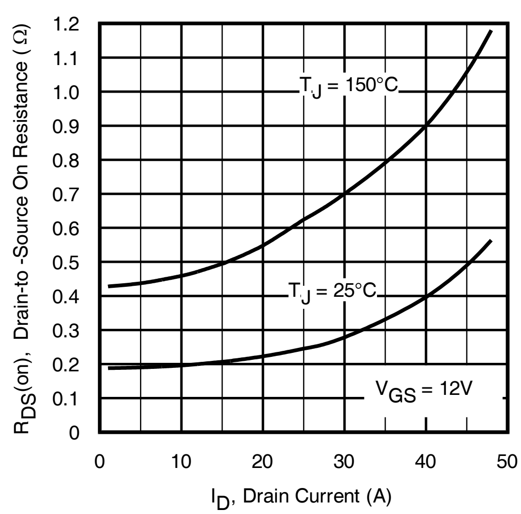


Fig 6. Typical On-Resistance Vs Drain Current

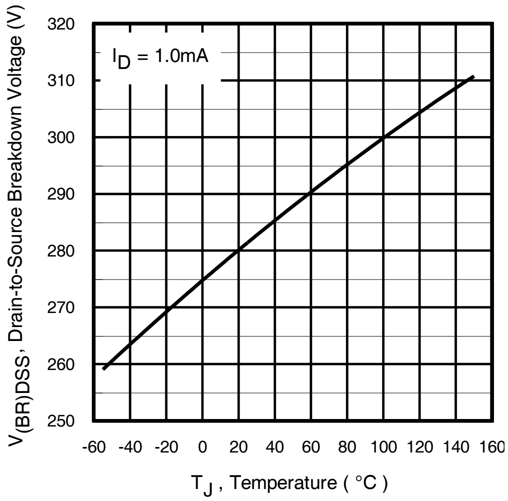


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

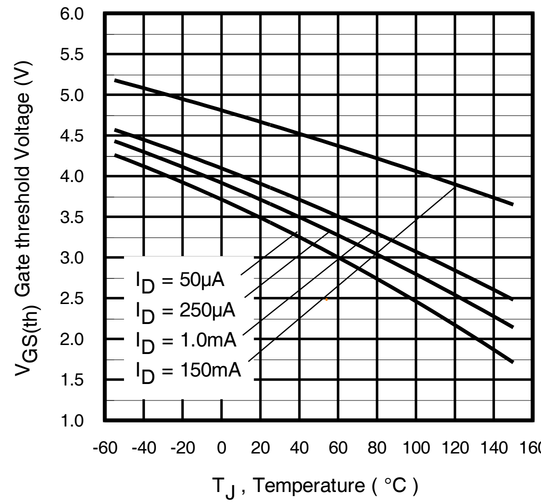


Fig 8. Typical Threshold Voltage Vs Temperature

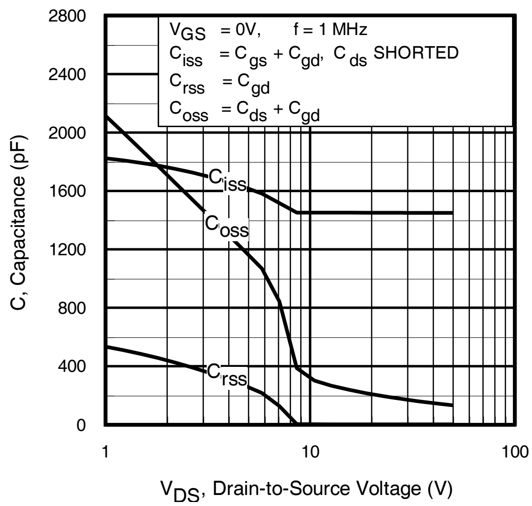


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

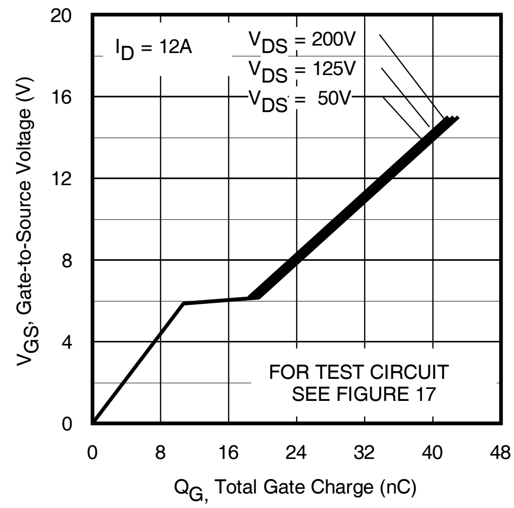


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

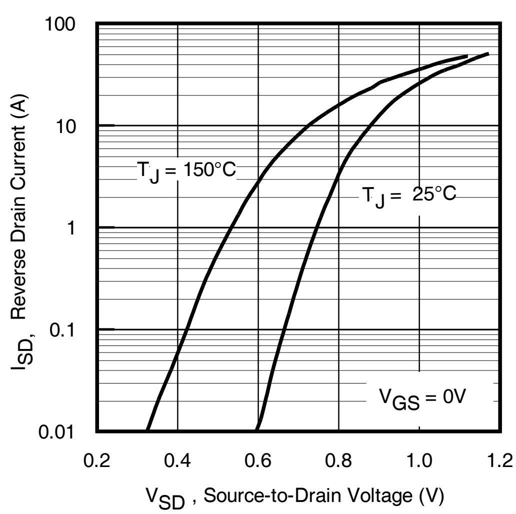


Fig 11. Typical Source-to-Drain Diode Forward Voltage

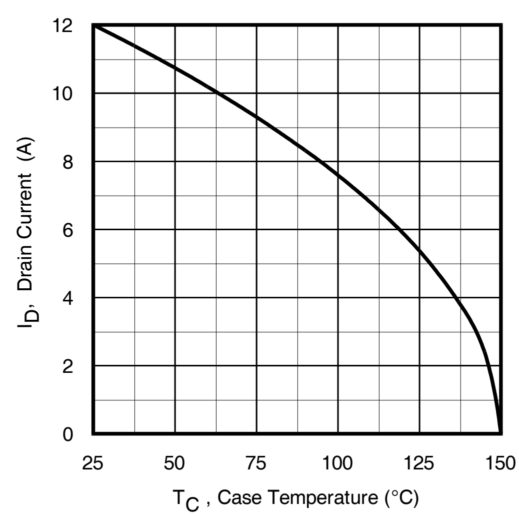


Fig 12. Maximum Drain Current Vs. Case Temperature

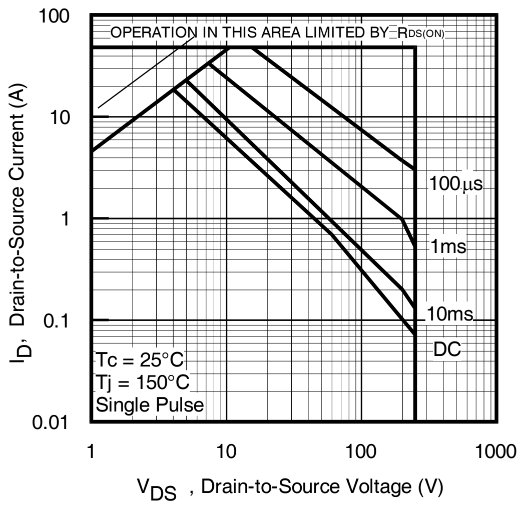


Fig 13. Maximum Safe Operating Area

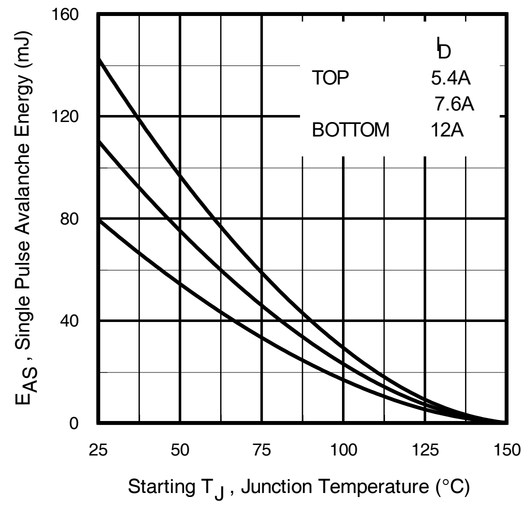


Fig 14. Maximum Avalanche Energy Vs. Drain Current

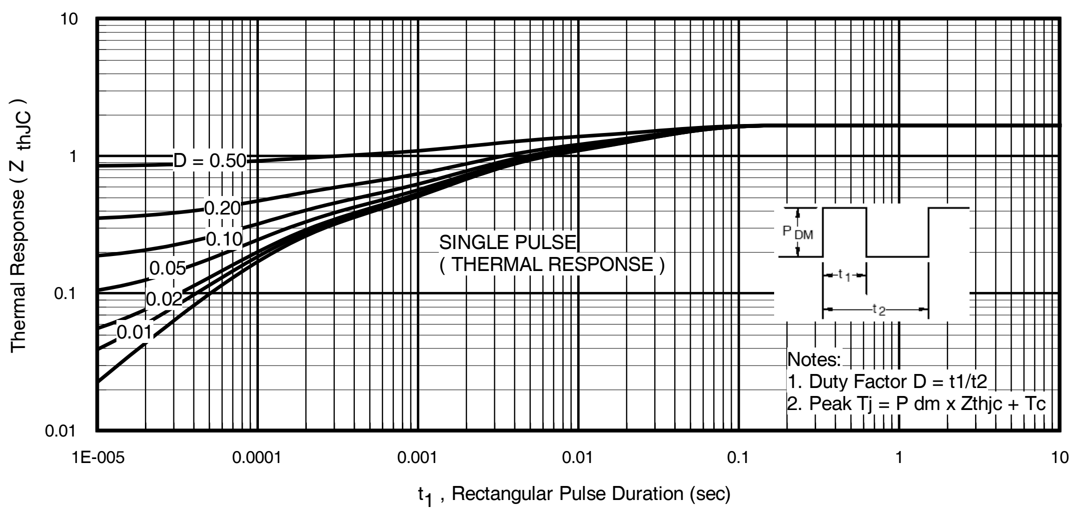


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-

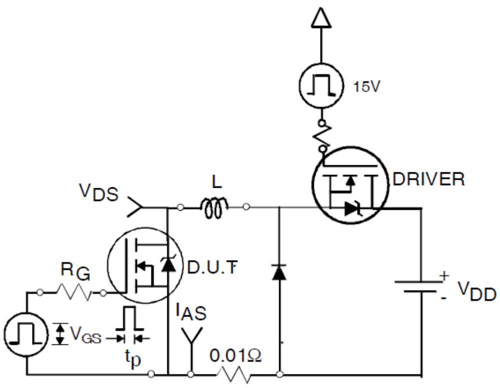


Fig 16a. Unclamped Inductive Test Circuit

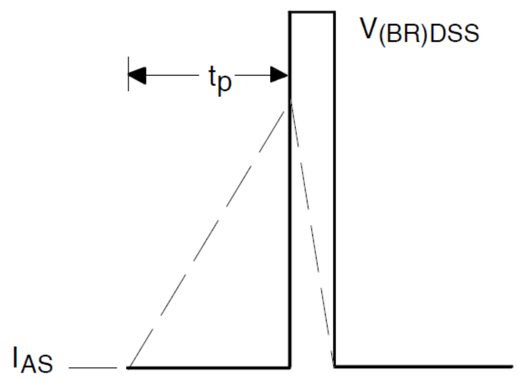


Fig 16b. Unclamped Inductive Wave-

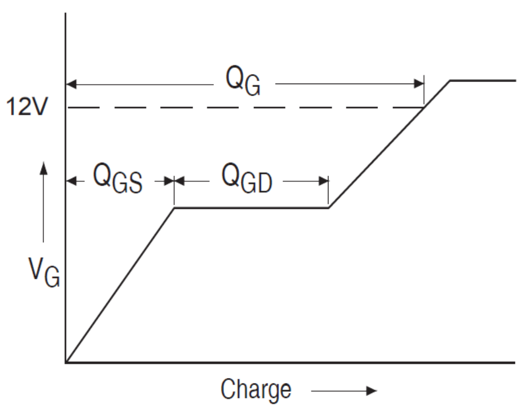


Fig 17a. Basic Gate Charge Waveform

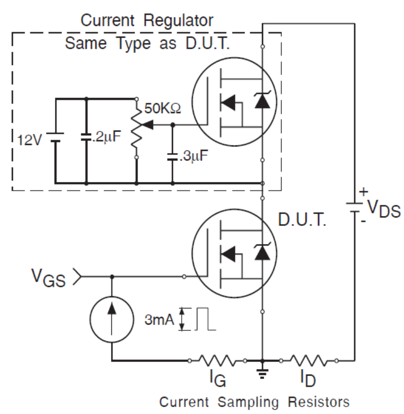


Fig 17b. Gate Charge Test Circuit

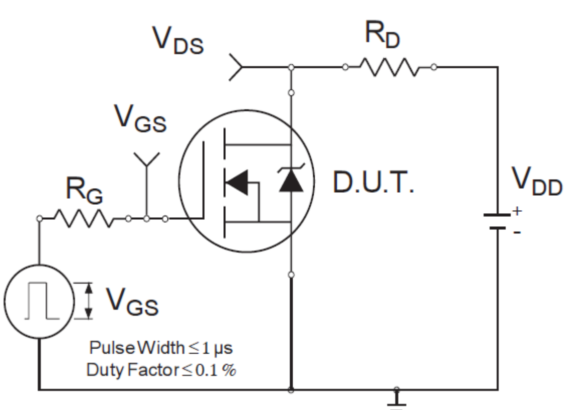


Fig 18a. Switching Time Test Circuit

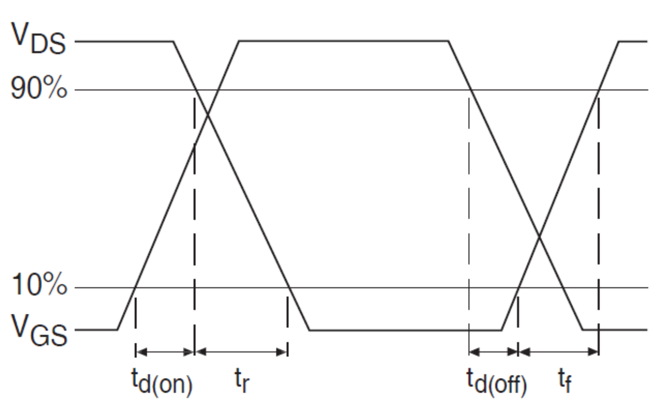
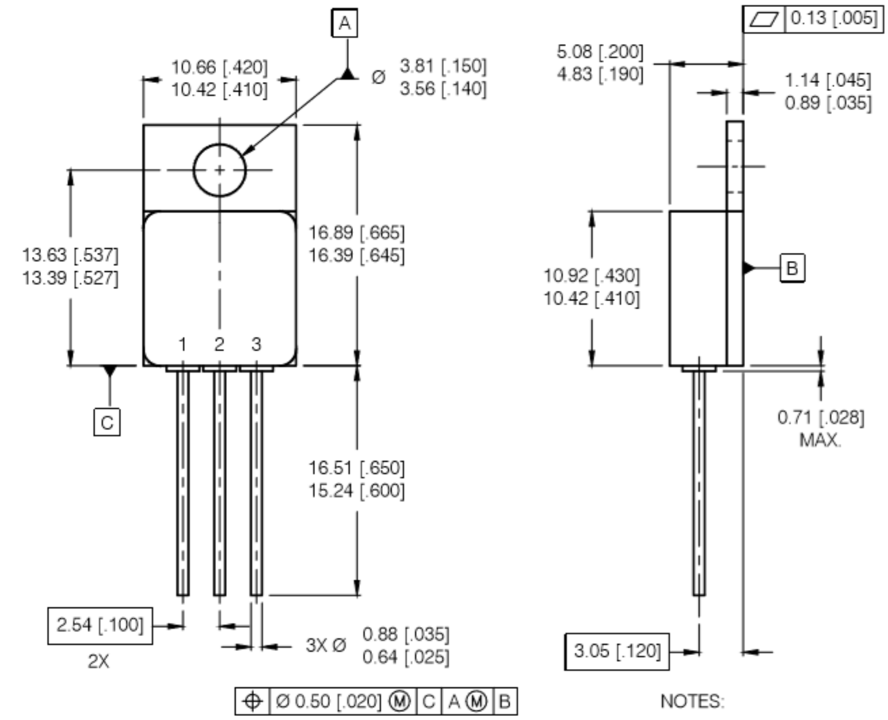


Fig 18b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: TO-257AA

Case Outline and Dimensions — Low –Ohmic (TO-257AA)

REV.	DESCRIPTION	ECN	DATE
B	INITIAL RELEASE	1120_ER6904	4–2–20



PIN ASSIGNMENTS
1 = DRAIN
2 = SOURCE
3 = GATE

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.
5. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

IR HiRel
An Infineon Technologies Company

TITLE: TO–257AA PACKAGE OUTLINE (STD & LOW OHMIC)	
DRAWING NO. D100723G–WEB	REV B

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

IR HiRel
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