An Infineon Technologies Company

IRHNS597Z60
JANSR2N7523U2A

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SupIR-SMD)

30V, P-CHANNEL
REF: MIL-PRF-19500/733
R5 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHNS597Z60	100 kRads(Si)	0.013Ω	-56A*	JANSR2N7523U2A
IRHNS593Z60	300 kRads(Si)	0.013Ω	-56A*	JANSF2N7523U2A

SupIR-SMD

Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 80 (MeV/(mg/cm^2). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight
- ESD Rating Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = -12V, T_C = 25°C	Continuous Drain Current	-56*	A
I_{D2} @ V_{GS} = -12V, T_C = 100°C	Continuous Drain Current	-56*	
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	-224	
P_D @ T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	1116	mJ
I_{AR}	Avalanche Current ①	-56	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	0.83	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package Mounting Surface Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

* Current is limited by package

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-30	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.03	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.013	Ω	V_{GS} = -12V, I_{D2} = -56A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
Gfs	Forward Transconductance	40	—	—	S	V_{DS} = -15V, I_{D2} = -56A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-10	µA	V_{DS} = -24V, V_{GS} = 0V
		—	—	-25		V_{DS} = -24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	240	nC	I_{D1} = -56A
Q_{GS}	Gate-to-Source Charge	—	—	60		V_{DS} = -15V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	55		V_{GS} = -12V
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = -15V
tr	Rise Time	—	—	175		I_{D1} = -56A
$t_{d(off)}$	Turn-Off Delay Time	—	—	100		R_G = 2.35Ω
t_f	Fall Time	—	—	80		V_{GS} = -12V
Ls +L_D	Total Inductance	—	2.8	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	7844	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	4512	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	564	—		f = 1.0MHz
R_G	Gate Resistance	—	2.1	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-56*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-224		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_J=25°C, I_S=-56A, V_{GS}=0V④
t_{rr}	Reverse Recovery Time	—	—	140	ns	T_J=25°C, I_F=-56A, V_{DD} ≤ -30V
Q_{rr}	Reverse Recovery Charge	—	—	351	nC	di/dt = -100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.5	°C/W

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = -30V, starting T_J = 25°C, L = 0.71mH, Peak I_L = -56A, V_{GS} = -12V
③ I_{SD} ≤ -56A, di/dt ≤ -187A/µs, V_{DD} ≤ -30V, T_J ≤ 150°C
④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
⑤ Total Dose Irradiation with V_{GS} Bias. -12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
⑥ Total Dose Irradiation with V_{DS} Bias. –24 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	100 kRads (Si)[1]		300 kRads (Si)[2]		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-30	——	-30	——	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	-2.0	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	-100	——	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	100	——	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	——	-10	——	-10	µA	V_{DS} = -24V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.014	——	0.014	Ω	V_{GS} = -12V, I_{D2} = -56A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SupIR-SMD)	——	0.013	——	0.013	Ω	V_{GS} = -12V, I_{D2} = -56A
V_{SD}	Diode Forward Voltage ④	——	-5.0	——	-5.0	V	V_{GS} = 0V, I_S = -56A

1. Part numbers IRHNS597Z60, JANSR2N7523U2A
2. Part numbers IRHNS593Z60, JANSF2N7523U2A

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS (V)				
			@ VGS = 0V	@ VGS = 5V	@ VGS = 10V	@ VGS = 15V	@ VGS = 20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-30	-30	-30	-30	-30
61 ± 5%	330 ± 7.5%	31 ± 10%	-30	-30	-30	-30	-25
84 ± 5%	350 ± 10%	28 ± 7.5%	-30	-30	-30	-25	——

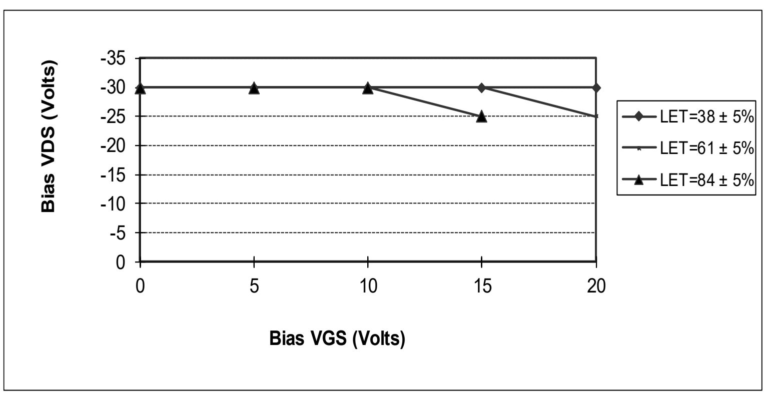


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation

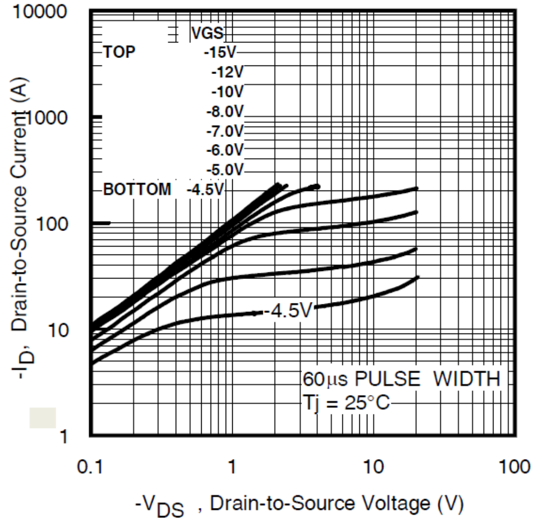


Fig 1. Typical Output Characteristics

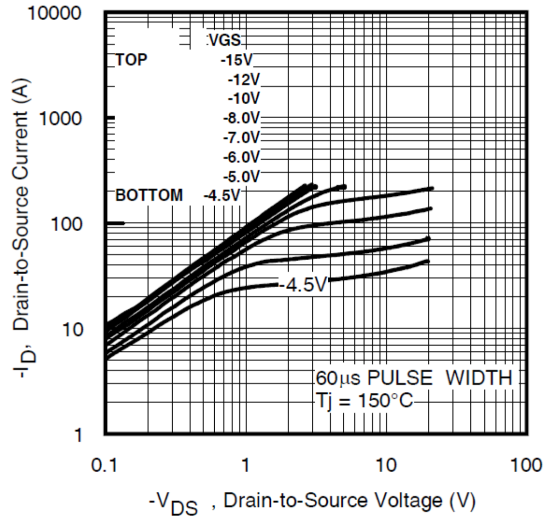


Fig 2. Typical Output Characteristics

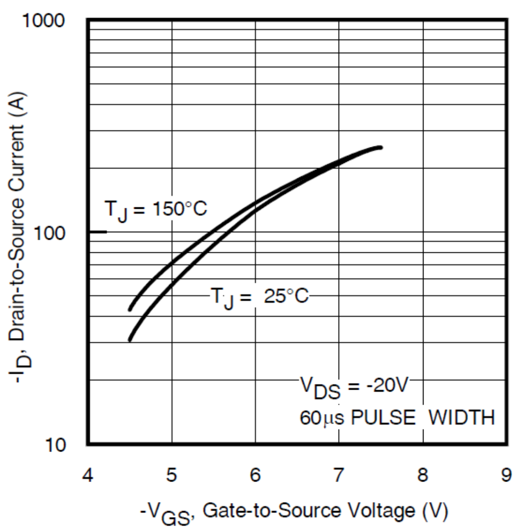


Fig 3. Typical Transfer Characteristics

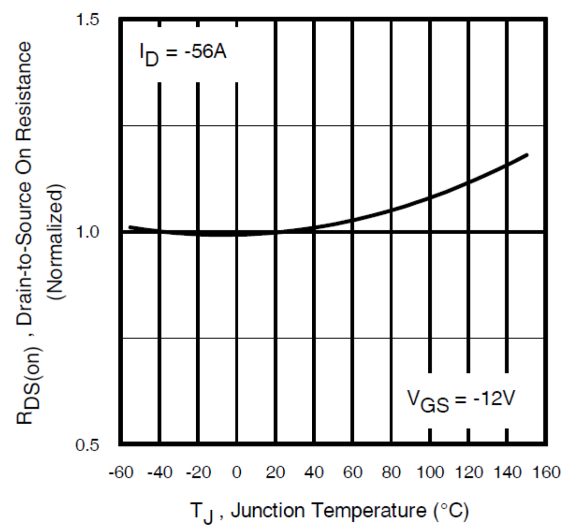


Fig 4. Normalized On-Resistance Vs. Temperature

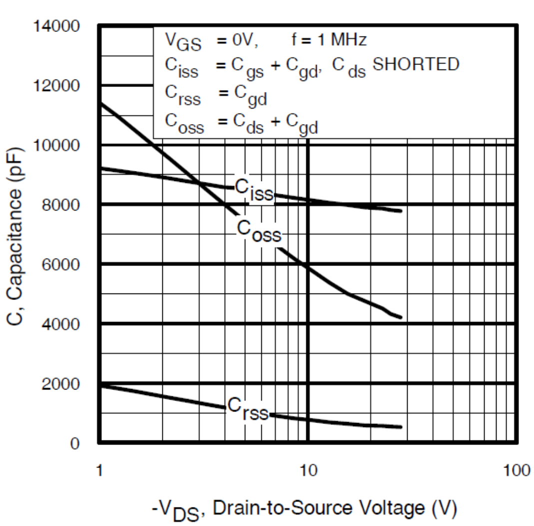


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

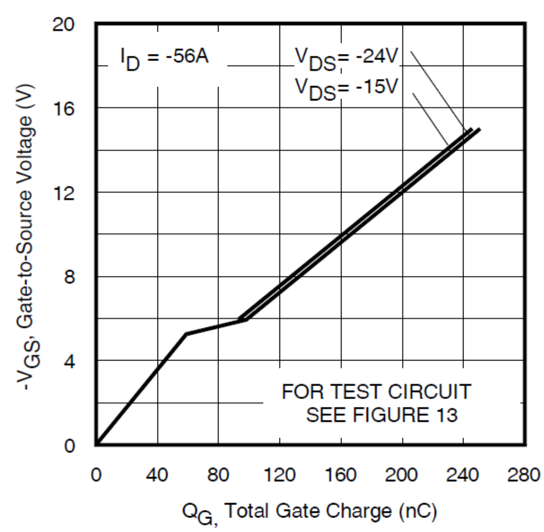


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

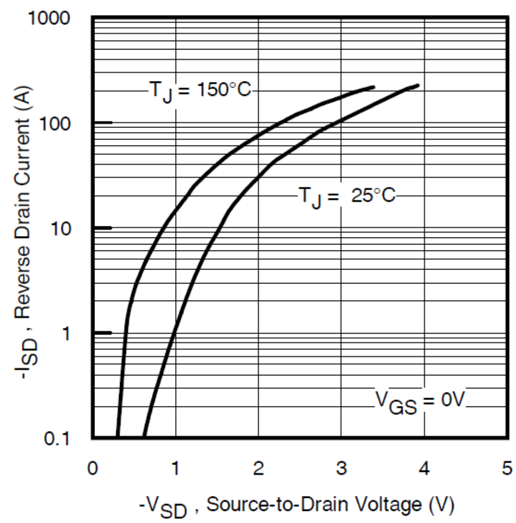


Fig 7. Typical Source-Drain Diode Forward Voltage

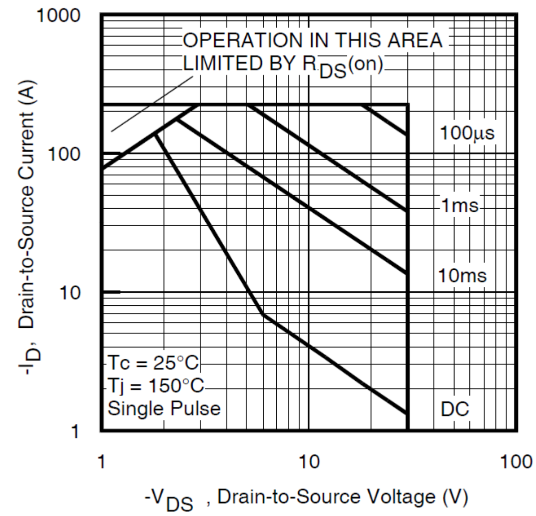


Fig 8. Maximum Safe Operating Area

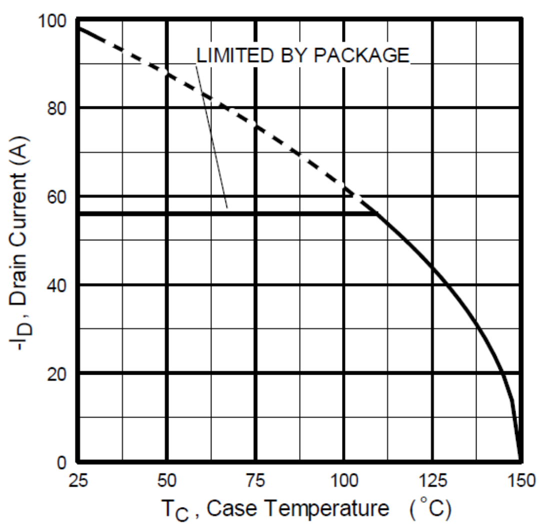


Fig 9. Maximum Drain Current Vs. Case Temperature

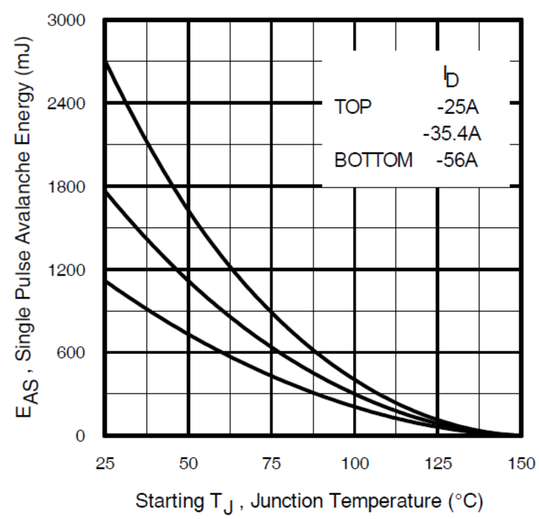


Fig 10. Maximum Avalanche Energy Vs. Drain Current

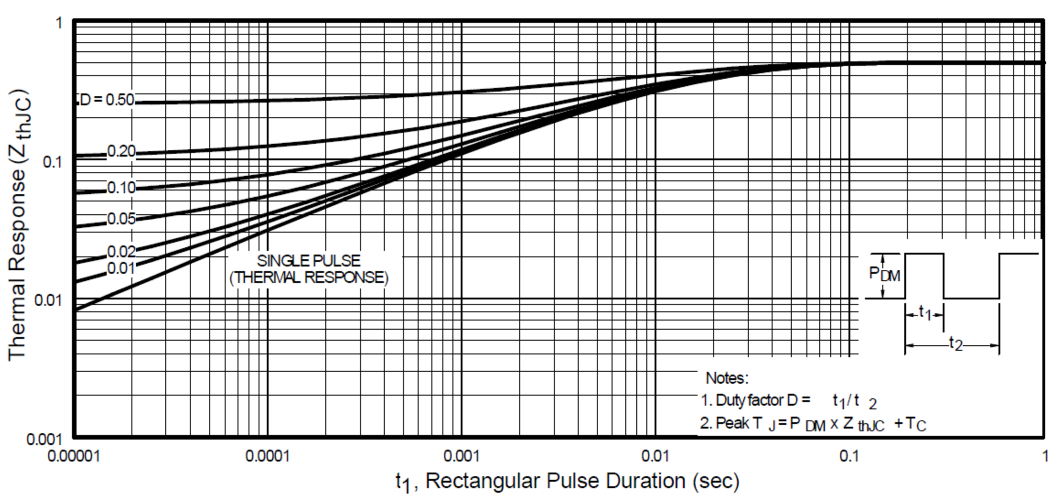


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

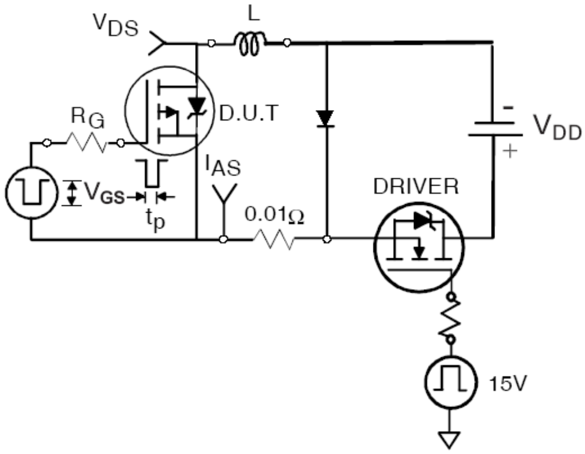


Fig 12a. Unclamped Inductive Test Circuit

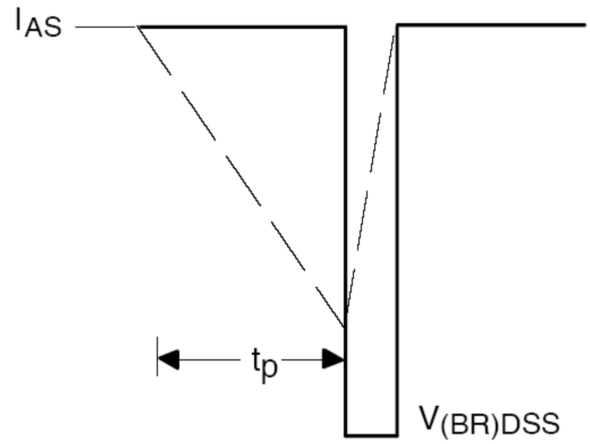


Fig 12b. Unclamped Inductive Waveforms

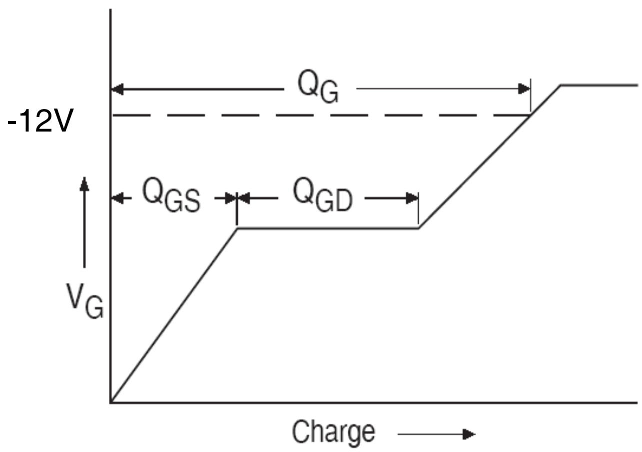


Fig 13a. Basic Gate Charge Waveform

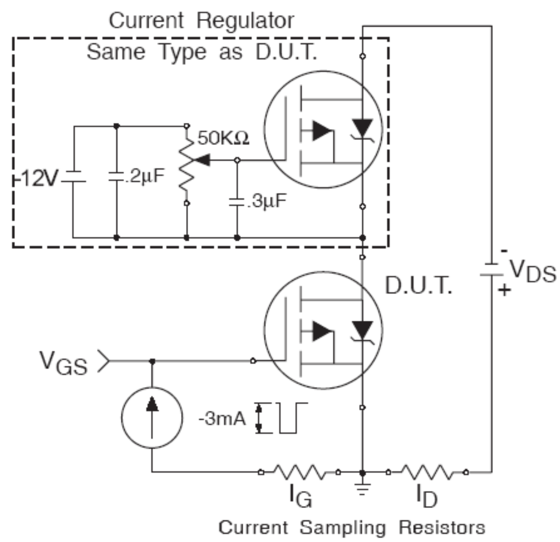


Fig 13b. Gate Charge Test Circuit

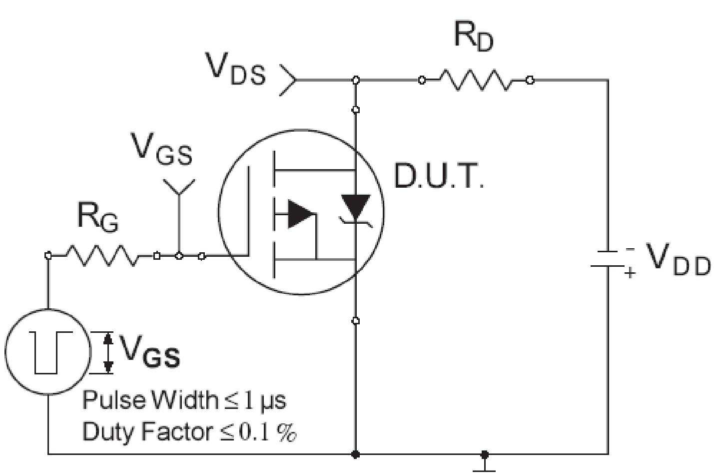


Fig 14a. Switching Time Test Circuit

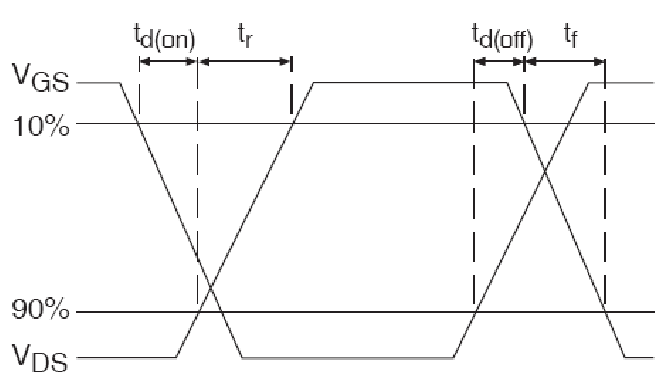
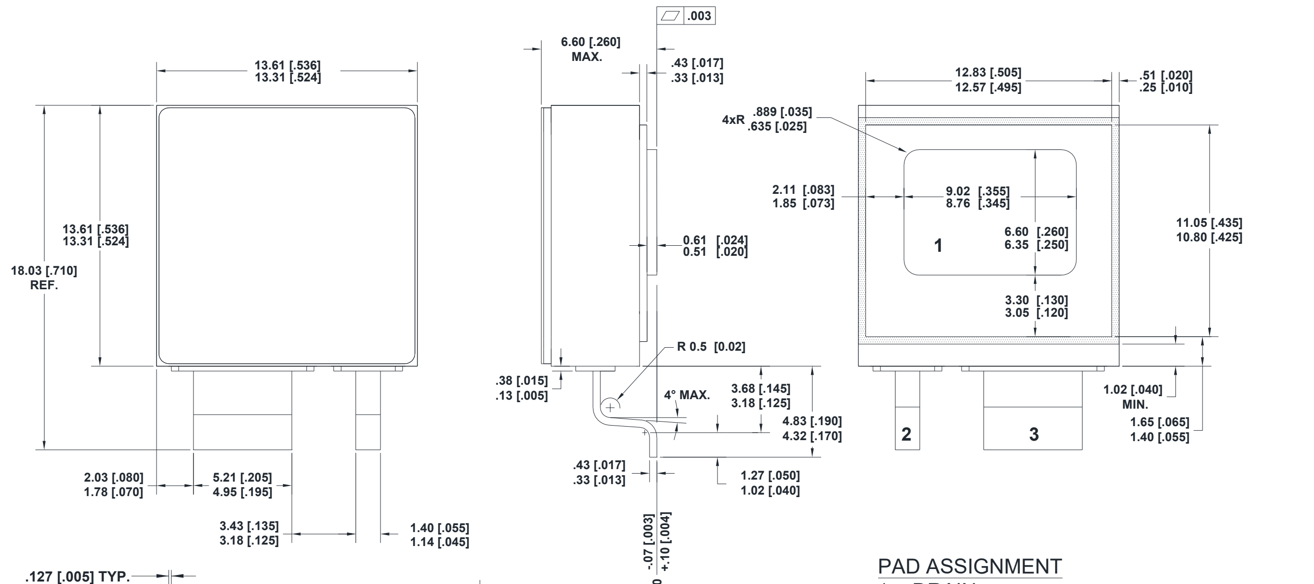


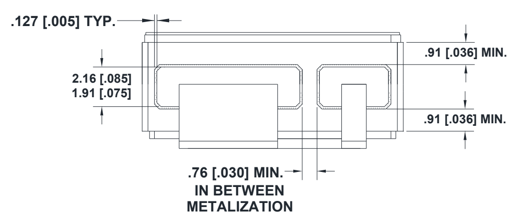
Fig 14b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [SupIR-SMD]

Case Outline and Dimensions - SupIR-SMD

REV.	DESCRIPTION	ECN	DATE
E	INITIAL RELEASE	1120_ER6904	4-3-20





PAD ASSIGNMENT
1 = DRAIN
2 = GATE
3 = SOURCE

NOTES:
1. FOR REFERENCE ONLY: LEAD LENGTH AFTER TIE-BAR CUT MUST .300 ±.015 FROM THE FROM PACKAGE BODY.
2. BEND AND TRIM LEADS USING EQUIPMENT ASSET #03493.
3. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

IOR HiRel
An Infineon Technologies Company

TITLE: CASE OUTLINE STD SUPSMD2, LF	
DRAWING NO. D101003G-WEB	REV E

IOR HiRel
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