IR HiRel
An Infineon Technologies Company

IRHNA67264
JANSR2N7585U2

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SMD-2)

250V, N-CHANNEL
REF: MIL-PRF-19500/760
R6 TECHNOLOGY

SMD-2

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHNA67264	100 kRads(Si)	0.040Ω	50A	JANSR2N7585U2
IRHNA63264	300 kRads(Si)	0.040Ω	50A	JANSF2N7585U2

Description

IR HiRel R6 technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 90 (MeV/(mg/cm^2). The combination of low R_{DS}(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Electrically Isolated
- Ceramic Package
- Light Weight
- Surface Mount
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	50	
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	31.5	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	200	
P_D @T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	240	mJ
I_{AR}	Avalanche Current ①	50	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.3	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.040	Ω	V_{GS} = 12V, I_{D2} = 31.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 1.0mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10.1	—	mV/°C	
gfs	Forward Transconductance	37	—	—	S	V_{DS} = 15V, I_{D2} = 31.5A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	25		V_{DS} = 200V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	220	nC	I_{D1} = 50A
Q_{GS}	Gate-to-Source Charge	—	—	50		V_{DS} = 125V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	70		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	50	ns	V_{DD} = 125V
t_r	Rise Time	—	—	150		I_{D1} = 50A
$t_{d(off)}$	Turn-Off Delay Time	—	—	100		R_G = 2.35Ω
t_f	Fall Time	—	—	50		V_{GS} = 12V
Ls +L_D	Total Inductance	—	2.8	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	6912	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	940	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	10.8	—		f = 1.0MHz
R_G	Gate Resistance	—	0.52	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	50	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	200		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J=25°C, I_S = 50A, V_{GS}=0V④
t_{rr}	Reverse Recovery Time	—	—	700	ns	T_J=25°C, I_F = 50A,V_{DD} ≤ 25V
Q_{rr}	Reverse Recovery Charge	—	—	15	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.5	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PC Board (Soldered to 2" sq copper clad board)	—	1.6	—	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L = 0.19mH, Peak I_L = 50A, V_{GS} = 12V

③ I_{SD} ≤ 50A, di/dt ≤ 900A/µs, V_{DD} ≤ 250V, T_J ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ Total Dose Irradiation with V_{DS} Bias. 200 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si)[1]		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	10	µA	V_{DS} = 200V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.041	Ω	V_{GS} = 12V, I_{D2} = 31.5A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SMD-2)	——	0.040	Ω	V_{GS} = 12V, I_{D2} = 31.5A
V_{SD}	Diode Forward Voltage ④	——	1.2	V	V_{GS} = 0V, I_S = 50A

1. Part numbers IRHNA67264 (JANSR2N7585U2) and IRHNA63264 (JANSF2N7585U2)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm^2))	Energy (MeV)	Range (µm)	VDS (V)				
			@ VGS=0V	@ VGS=-5V	@ VGS=-10V	@ VGS=-15V	@ VGS=-20V
44 ± 5%	1350 ± 5%	125 ± 10%	250	250	250	250	40
61 ± 5%	825 ± 5%	66 ± 7.5%	250	250	250	50	——
90 ± 5%	1470 ± 5%	80 ± 5%	75	75	——	——	——

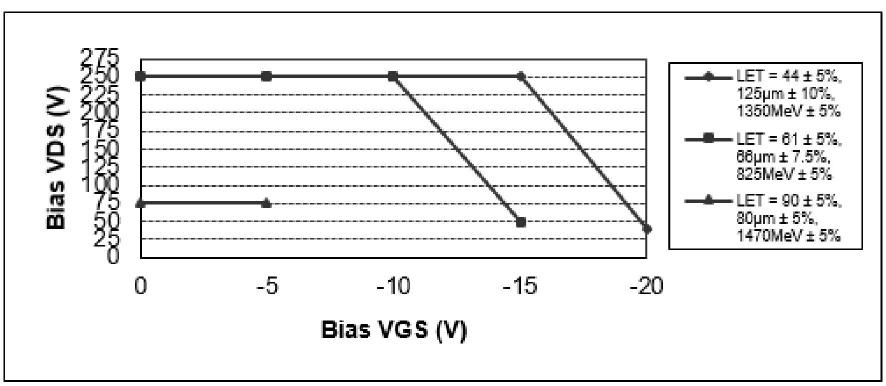


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

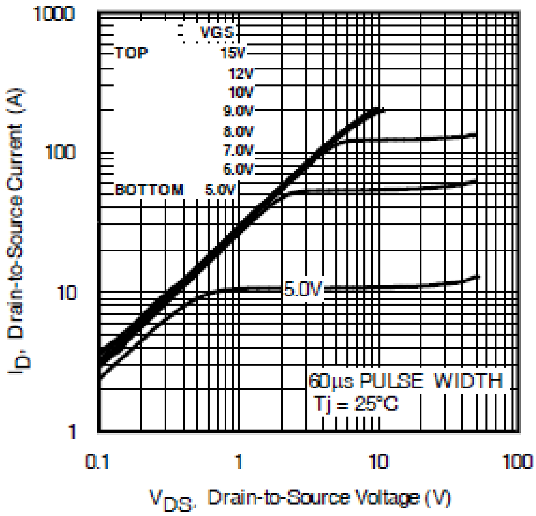


Fig 1. Typical Output Characteristics

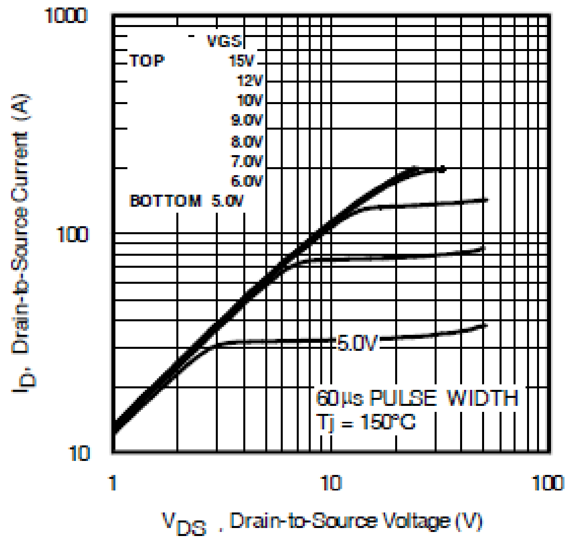


Fig 2. Typical Output Characteristics

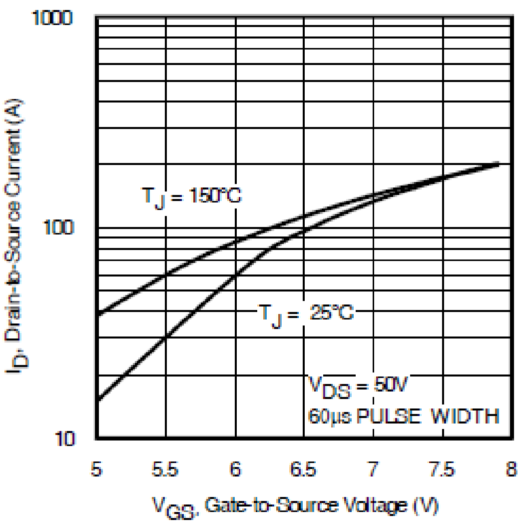


Fig 3. Typical Transfer Characteristics

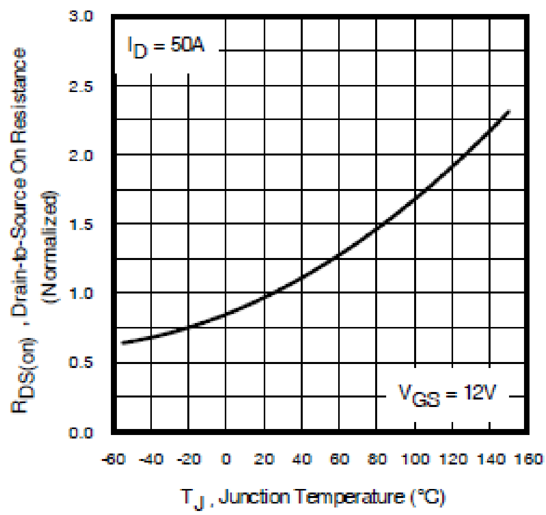


Fig 4. Normalized On-Resistance Vs. Temperature

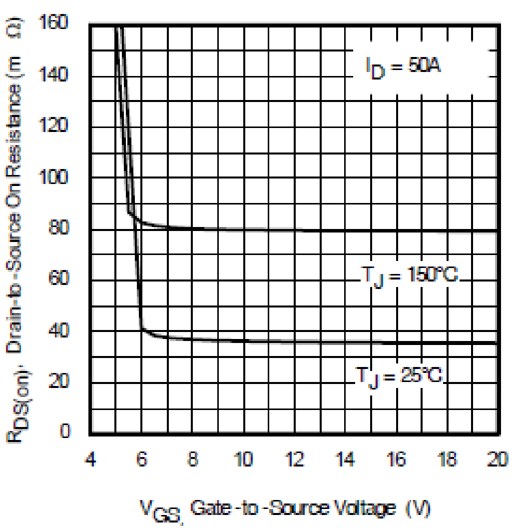


Fig 5. Typical On-Resistance Vs Gate Voltage

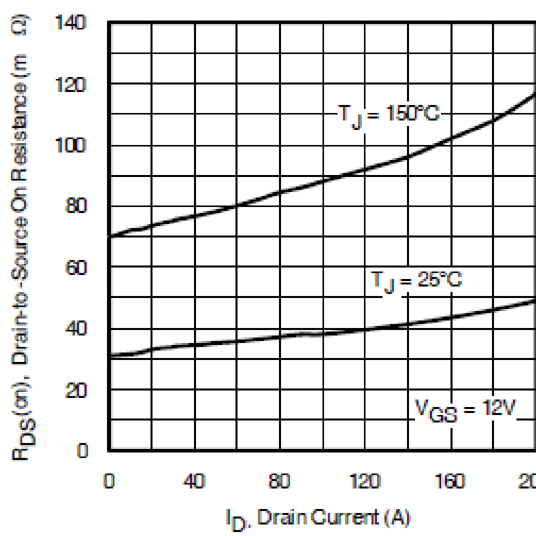


Fig 6. Typical On-Resistance Vs Drain Current

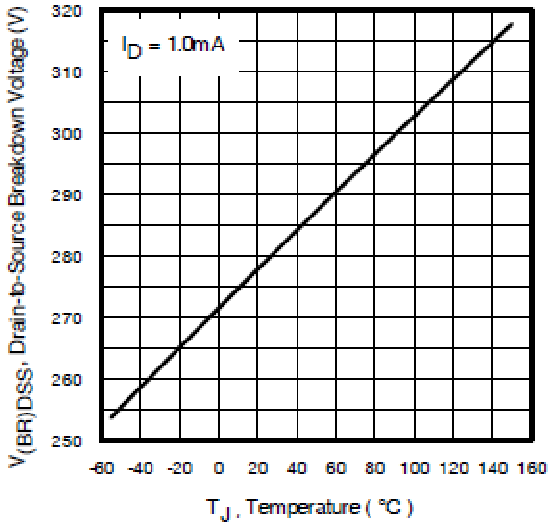


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

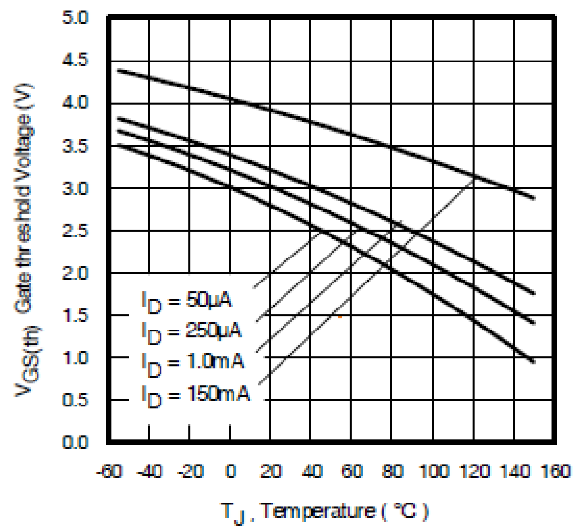


Fig 8. Typical Threshold Voltage Vs Temperature

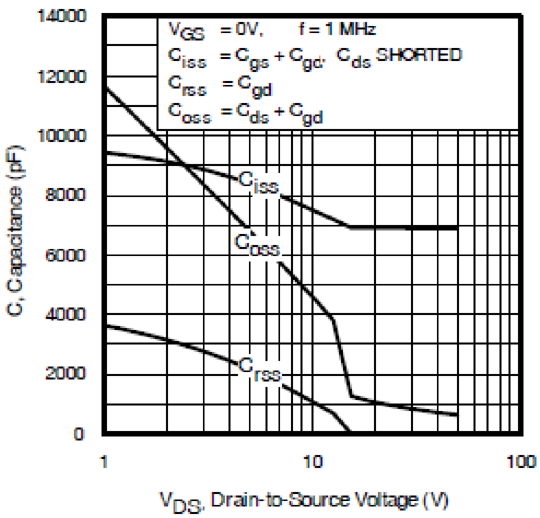


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

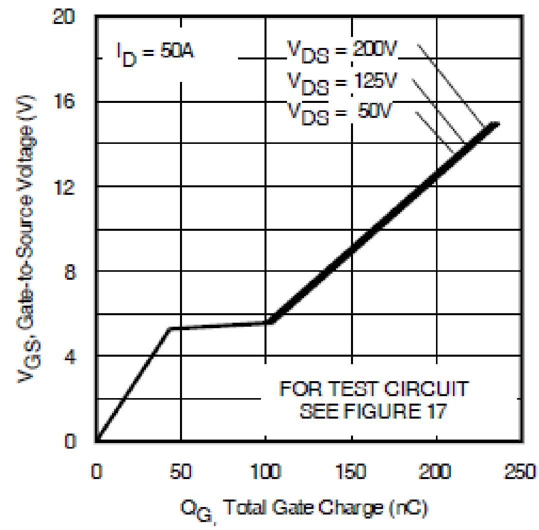


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

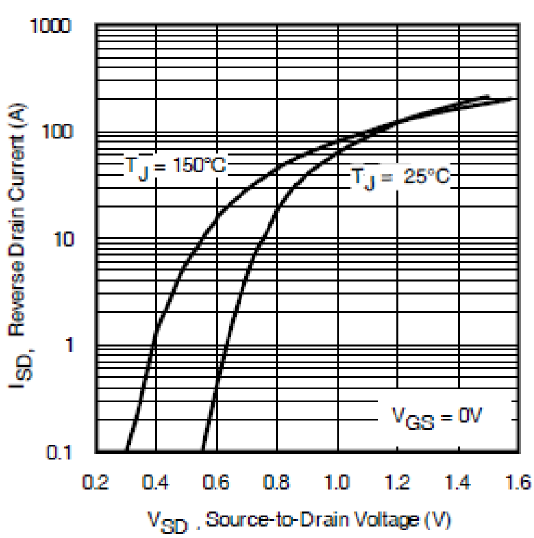


Fig 11. Typical Source-Drain Diode Forward Voltage

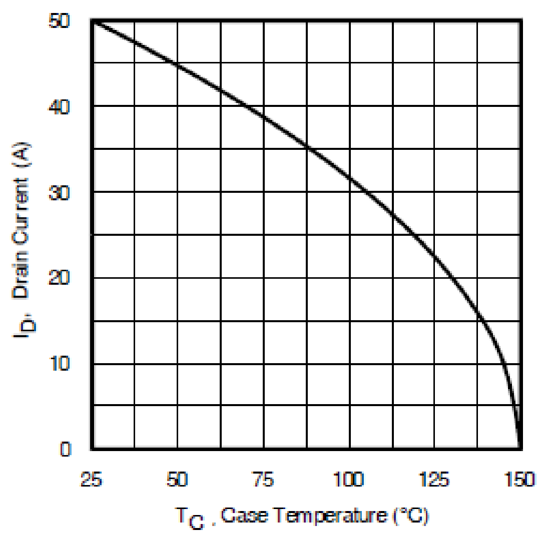


Fig 12. Maximum Drain Current Vs.Case Temperature

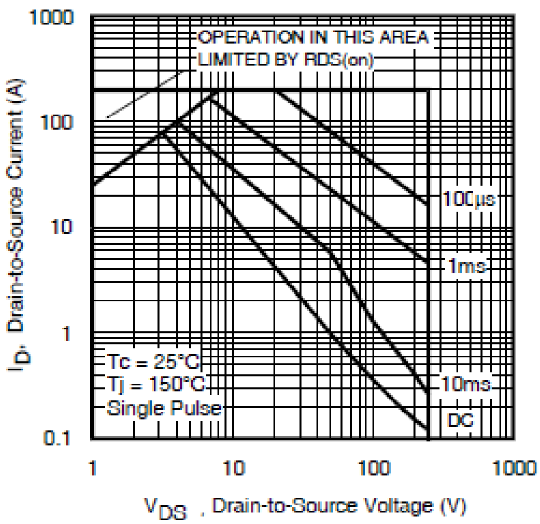


Fig 13. Maximum Safe Operating Area

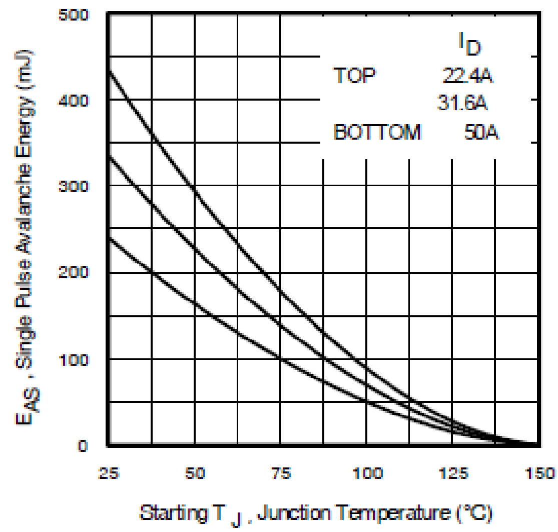


Fig 14. Maximum Avalanche Energy Vs. Drain Current

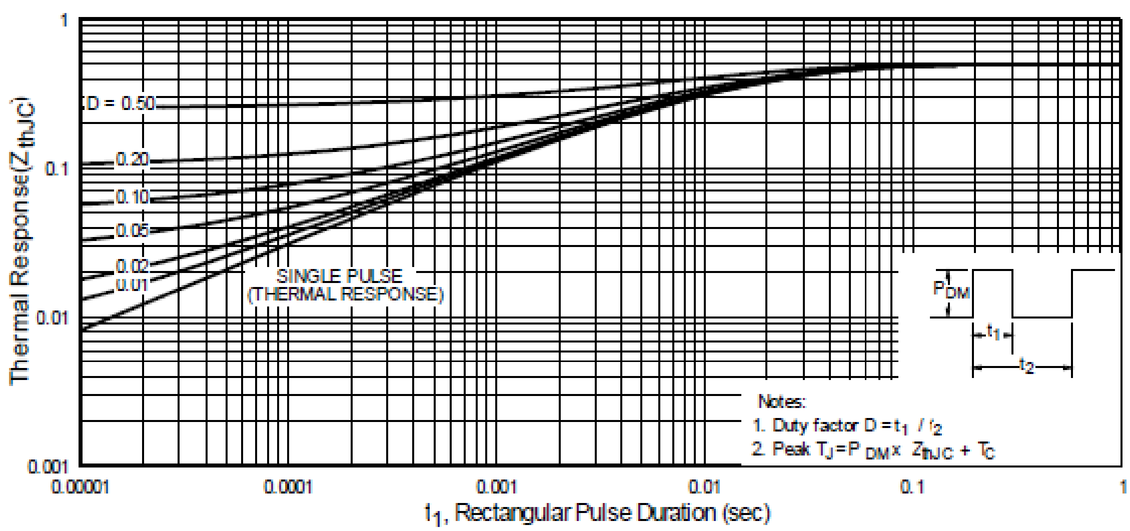


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

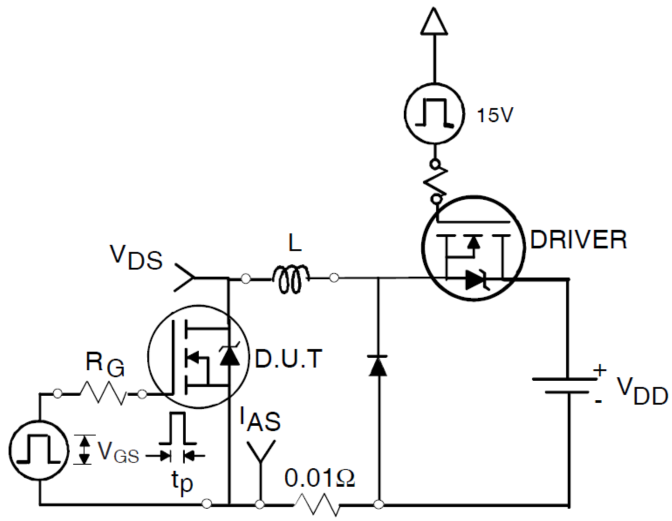


Fig 16a. Unclamped Inductive Test Circuit

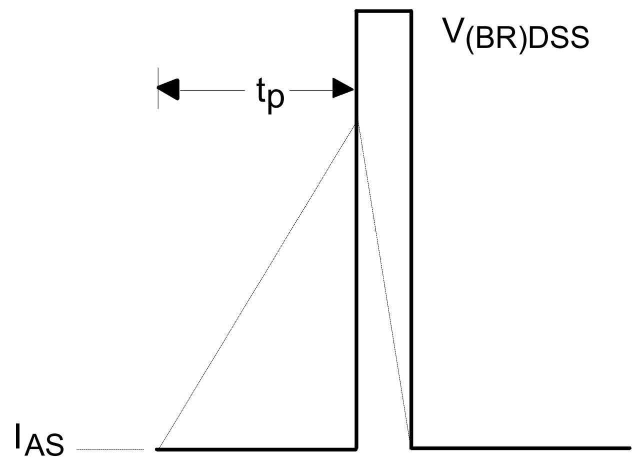


Fig 16b. Unclamped Inductive Wave-

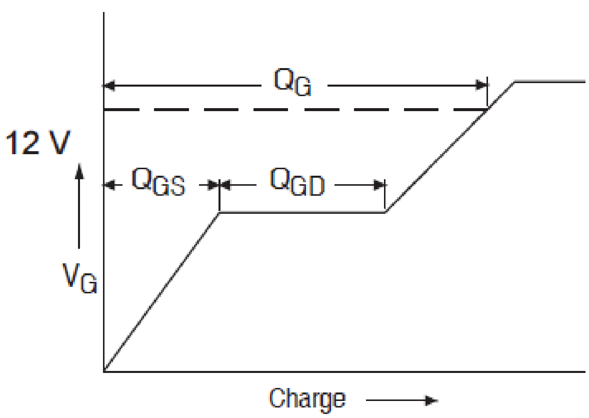


Fig 17a. Gate Charge Waveform

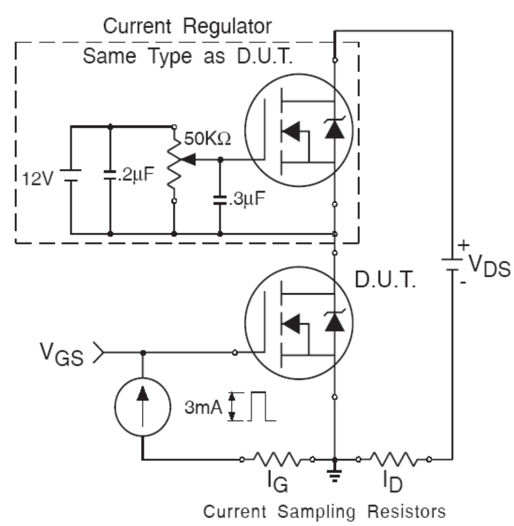


Fig 17b. Gate Charge Test Circuit

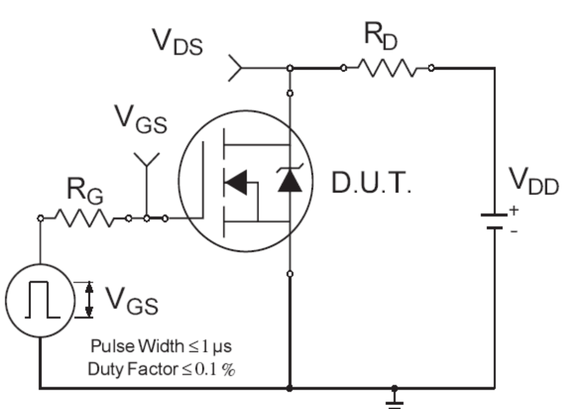


Fig 18a. Switching Time Test Circuit

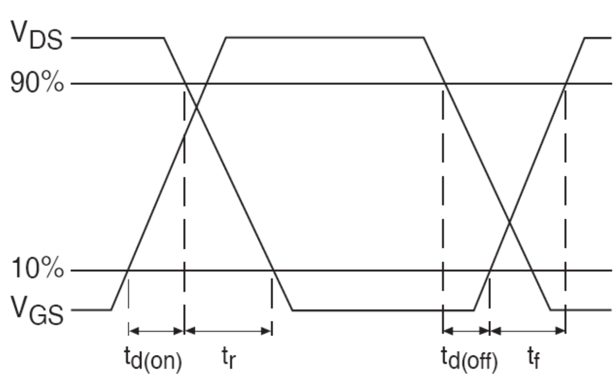
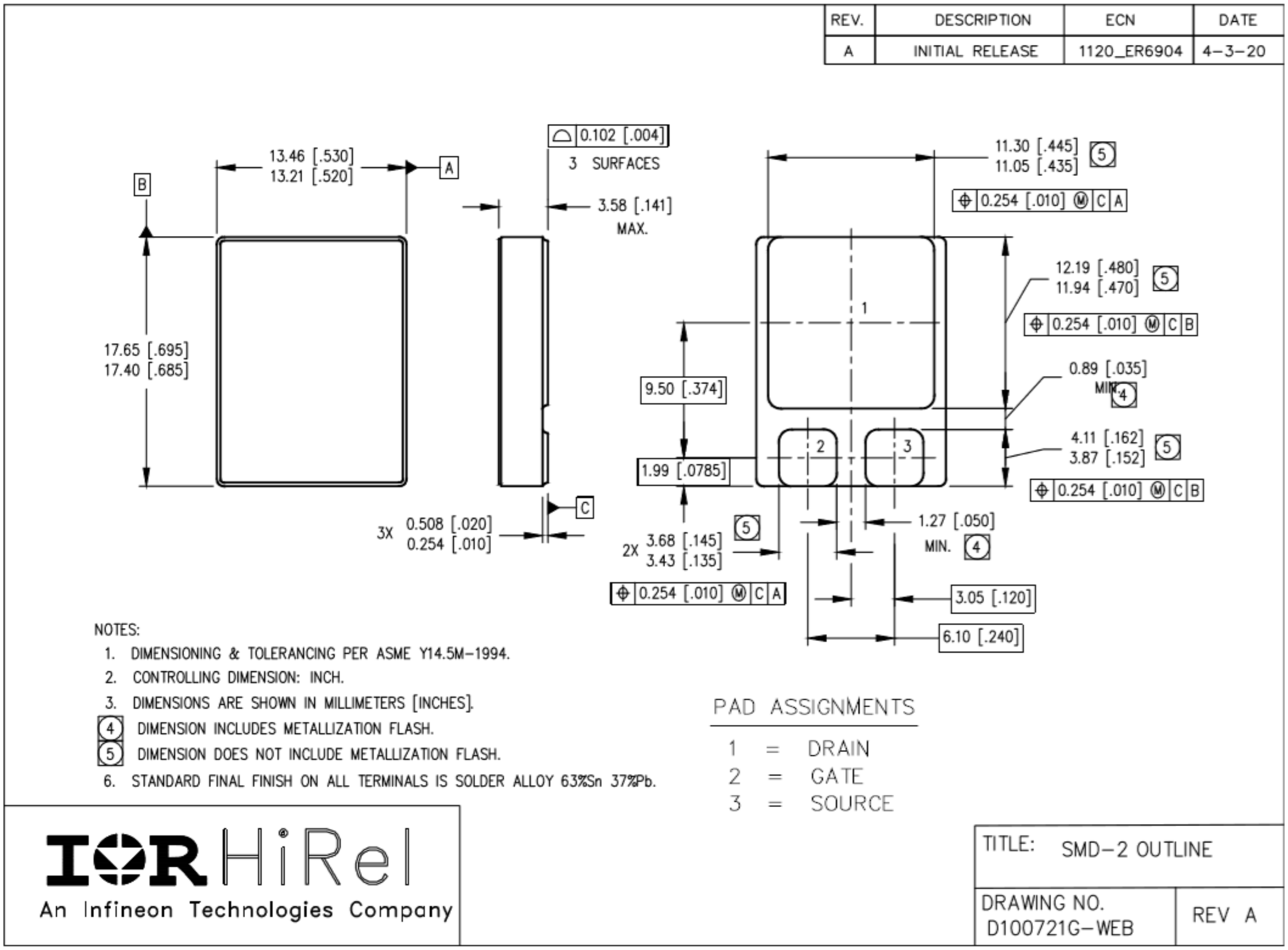


Fig 18b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [SMD-2]

Case Outline and Dimensions — SMD-2



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