PD-93816G

An Infineon Technologies Company

IRHNA57264SE
JANSR2N7474U2

RADIATION HARDENED
POWER MOSFET
SURFACE MOUNT (SMD-2)

250V, N-CHANNEL
REF: MIL-PRF-19500/684
R5 TECHNOLOGY

SMD-2

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHNA57264SE	100 kRads(Si)	0.06Ω	45A	JANSR2N7474U2

Description

IRHNA57264SE is part of the International Rectifier HiRel family of products. IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 80 (MeV/(mg/cm^2)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Package
- Light Weight
- Surface Mount
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	45	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	28	
I_{DM}	Pulsed Drain Current ①	180	
P_D @T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	222	mJ
I_{AR}	Avalanche Current ①	45	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.28	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.06	Ω	V_{GS} = 12V, I_D = 28A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.5	—	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
Gfs	Forward Transconductance	27	—	—	S	V_{DS} = 15V, I_D = 28A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	25		V_{DS} = 200V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	165	nC	I_D = 45A
Q_{GS}	Gate-to-Source Charge	—	—	45		V_{DS} = 125V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	75		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = 125V
tr	Rise Time	—	—	125		I_D = 45A
$t_{d(off)}$	Turn-Off Delay Time	—	—	80		R_G = 2.35Ω
t_f	Fall Time	—	—	65		V_{GS} = 12V
Ls +L_D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	5045	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	781	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	70	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	45	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J=25°C, I_S= 45A, V_{GS}=0V④
t_{rr}	Reverse Recovery Time	—	—	560	ns	T_J=25°C, I_F = 45A, V_{DD} ≤ 50V
Q_{rr}	Reverse Recovery Charge	—	—	8.6	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.5	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PC Board (Soldered to 2" sq copper clad board)	—	1.6	—	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L = 0.22mH, Peak I_L = 45A, V_{GS} = 12V

③ I_{SD} ≤ 45A, di/dt ≤ 274A/µs, V_{DD} ≤ 250V, T_J ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ Total Dose Irradiation with V_{GS} Bias: 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ Total Dose Irradiation with V_{DS} Bias: 200 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100 kRads (Si)		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	10	µA	V_{DS} = 200V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.061	Ω	V_{GS} = 12V, I_D = 28A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SMD-2)	——	0.060	Ω	V_{GS} = 12V, I_D = 28A
V_{SD}	Diode Forward Voltage ④	——	1.2	V	V_{GS} = 0V, I_D = 45A

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm^2))	Energy (MeV)	Range (µm)	VDS (V)				
			@ VGS = 0V	@ VGS=-5V	@ VGS=-10V	@ VGS =-15V	@ VGS=-20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	250	250	250	250	250
61 ± 5%	330 ± 7.5%	31 ± 10%	250	250	250	250	240
84 ± 5%	350 ± 7.5%	28 ± 7.5%	250	250	225	175	50

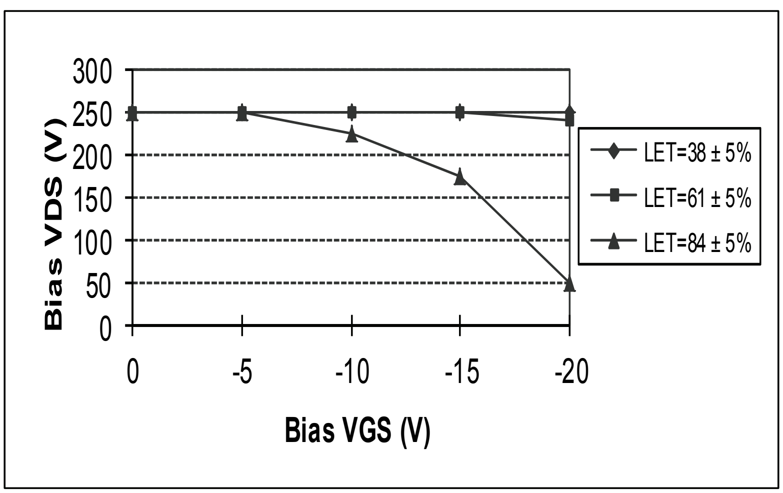


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation

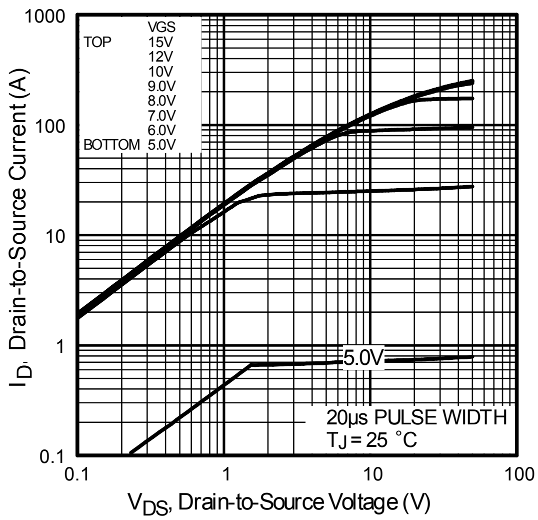


Fig 1. Typical Output Characteristics

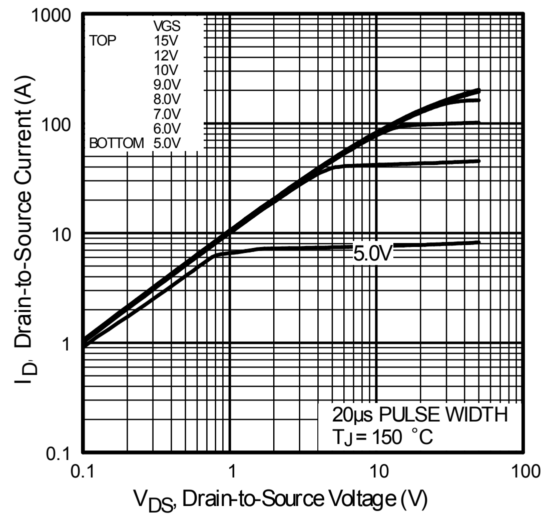


Fig 2. Typical Output Characteristics

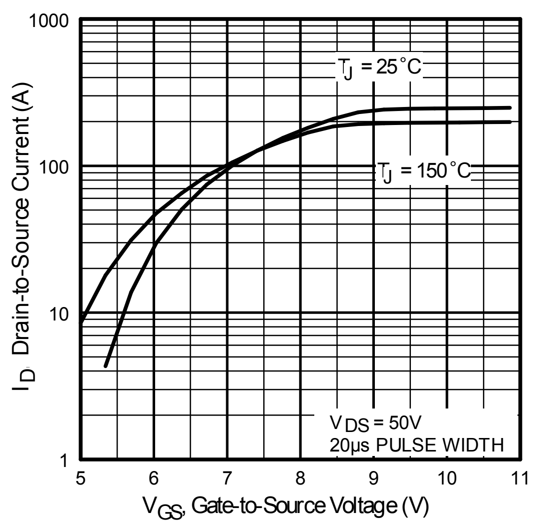


Fig 3. Typical Transfer Characteristics

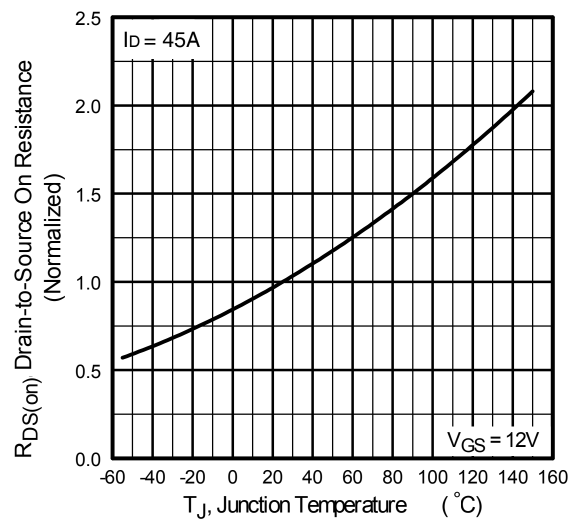


Fig 4. Normalized On-Resistance Vs. Temperature

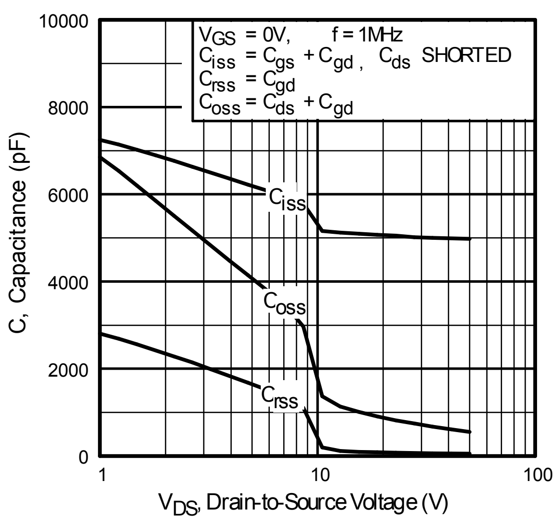


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

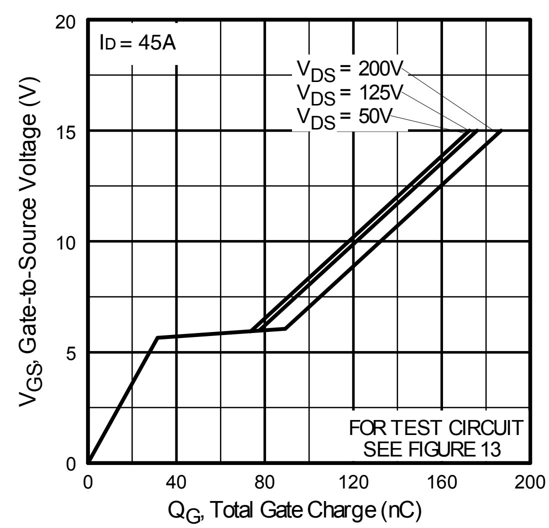


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

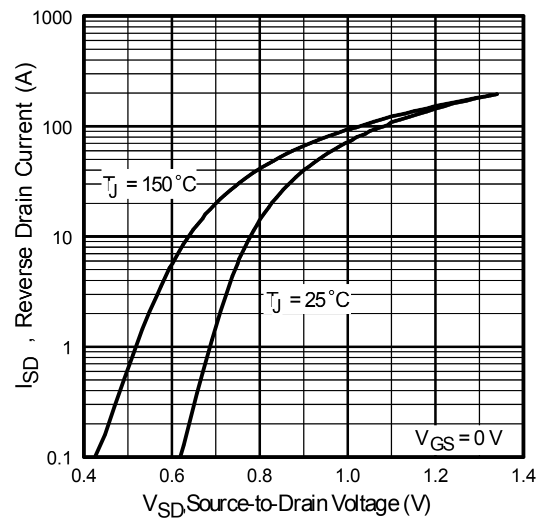


Fig 7. Typical Source-Drain Diode Forward Voltage

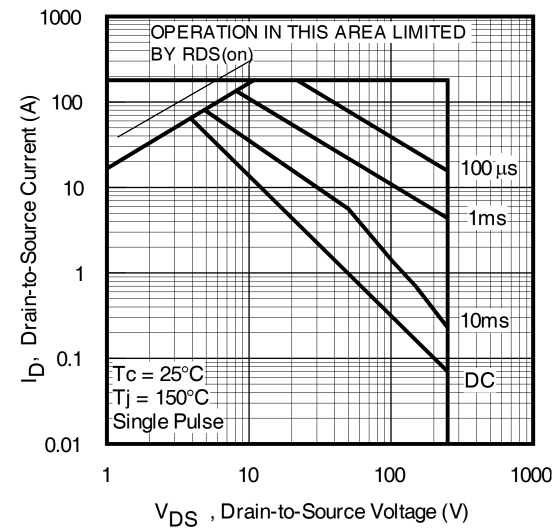


Fig 8. Maximum Safe Operating Area

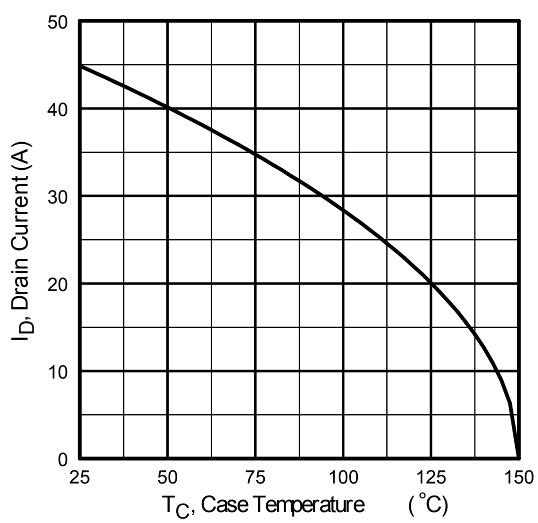


Fig 9. Maximum Drain Current Vs. Case Temperature

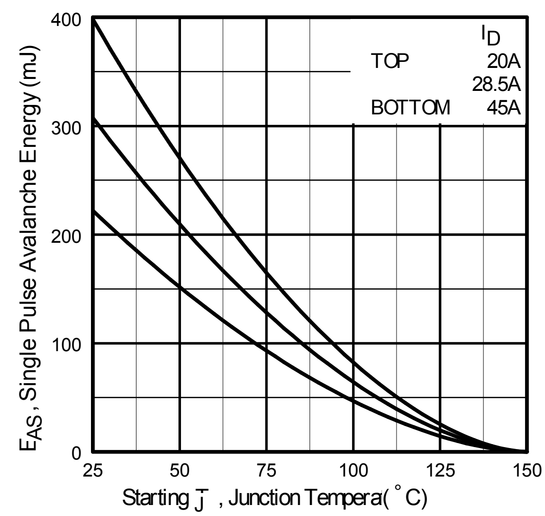


Fig 10. Maximum Avalanche Energy Vs. Drain Current

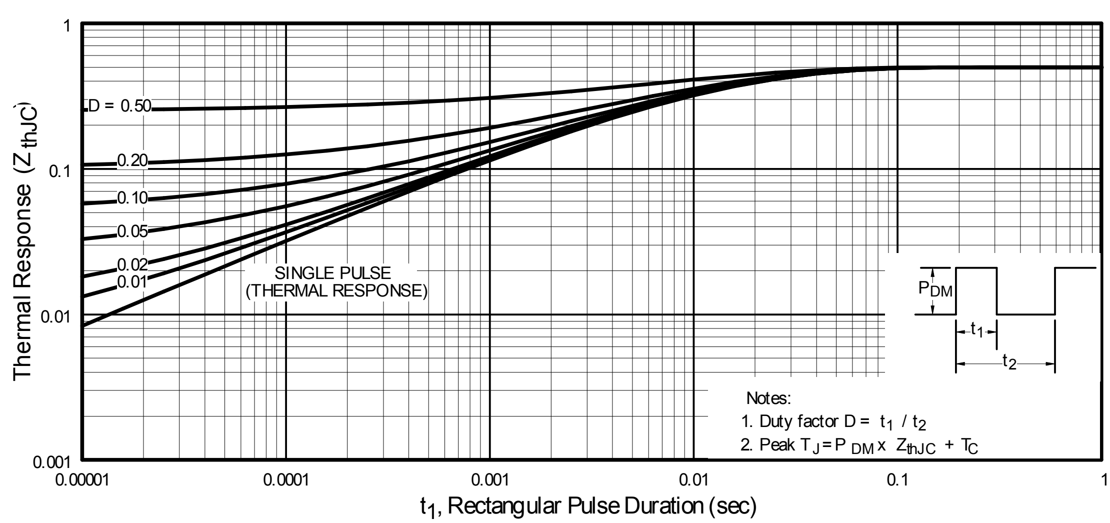


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

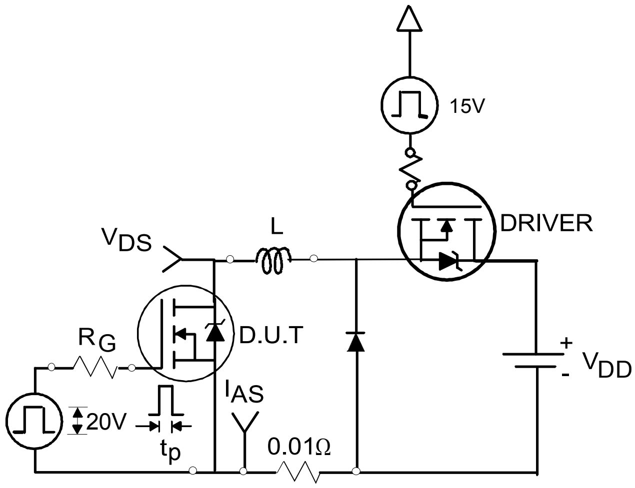


Fig 16a. Unclamped Inductive Test Circuit

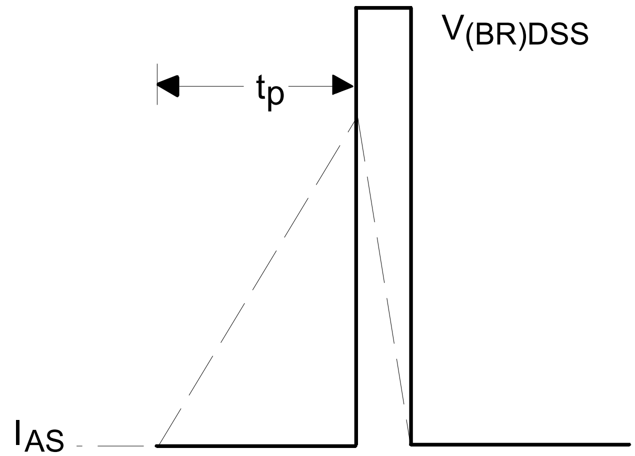


Fig 16b. Unclamped Inductive Waveforms

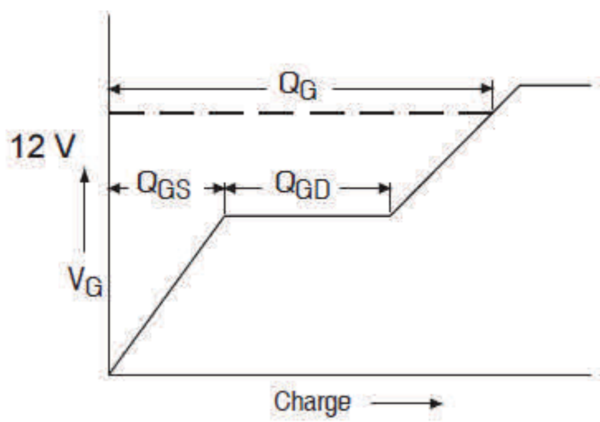


Fig 17a. Gate Charge Waveform

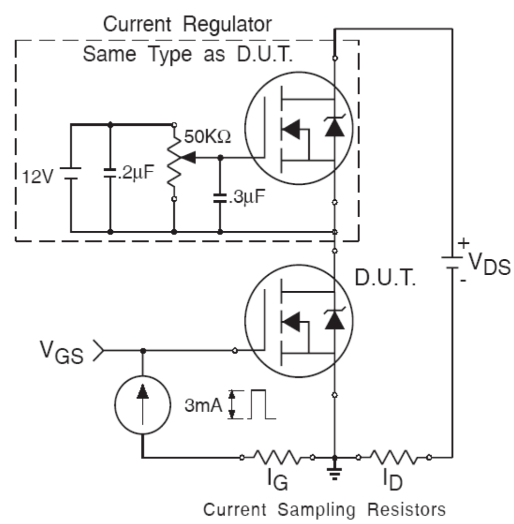


Fig 17b. Gate Charge Test Circuit

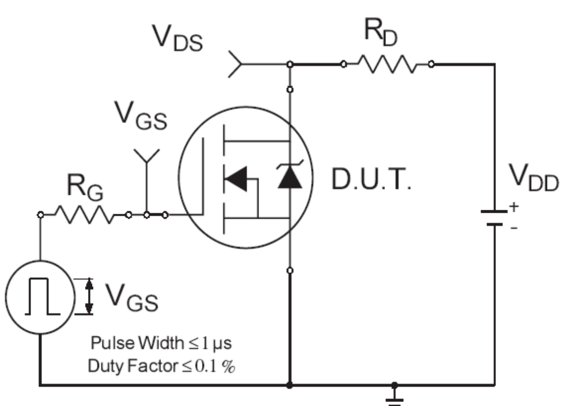


Fig 18a. Switching Time Test Circuit

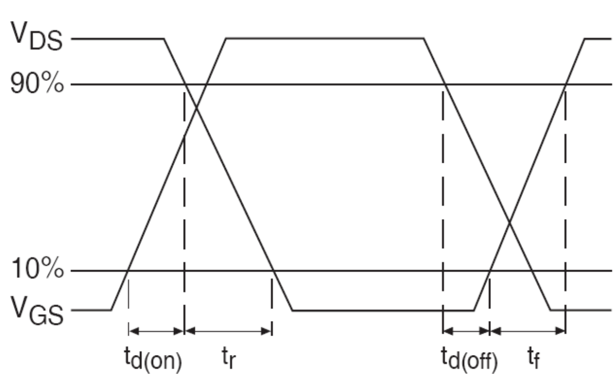
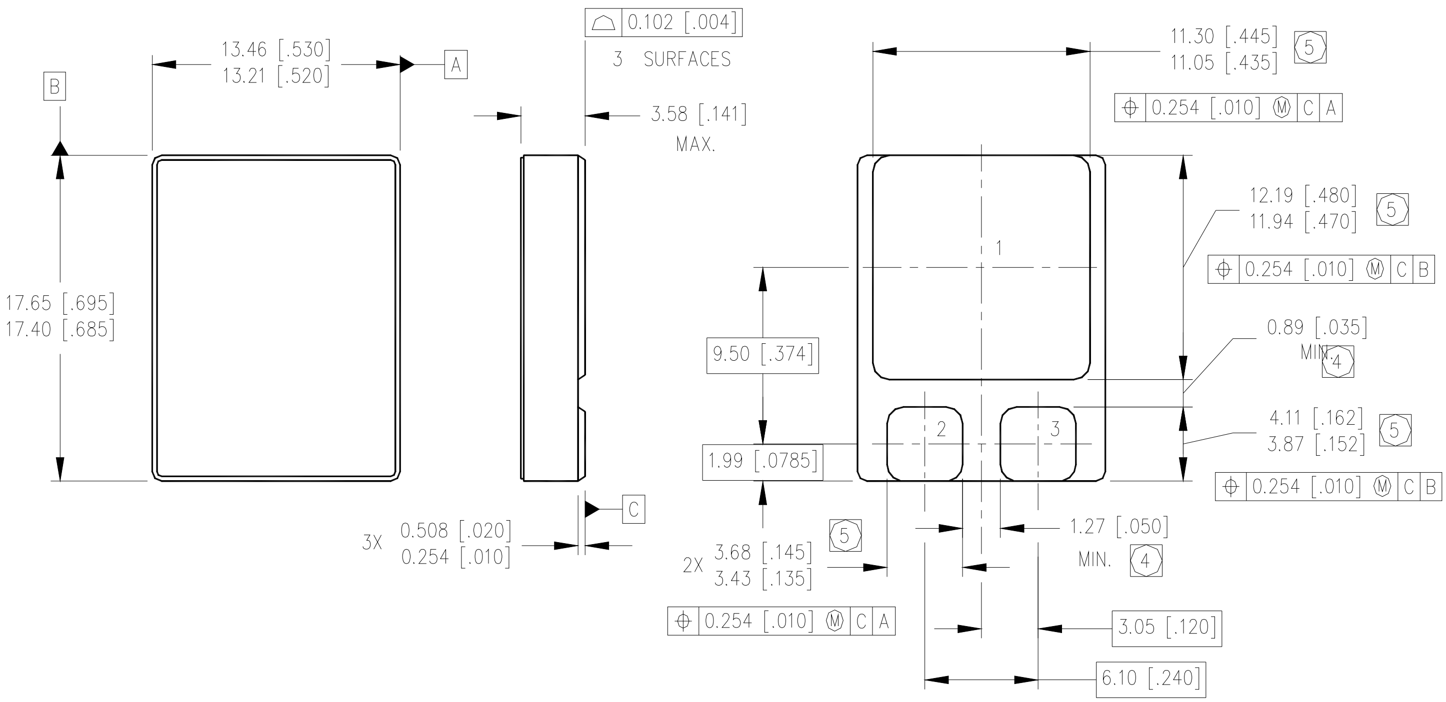


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions — SMD-2



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 DIMENSION INCLUDES METALLIZATION FLASH.
5 DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

MOSFET
1 = DRAIN
2 = GATE
3 = SOURCE

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