

**RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
SURFACE MOUNT (SMD-2)**

**60V, N-CHANNEL
R7 TECHNOLOGY**

Product Summary

Part Number	Radiation Level	RDS(on)	I _D
IRHLNA77064	100 kRads(Si)	0.012Ω	56A*
IRHLNA73064	300 kRads(Si)	0.012Ω	56A*



Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Features

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic package
- Light Weight
- Surface Mount
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	56*	A
I _{D2} @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	56*	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	224	
P _D @ T _C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V _{GS}	Gate-to-Source Voltage	± 10	V
E _{AS}	Single Pulse Avalanche Energy ②	402	mJ
I _{AR}	Avalanche Current ①	56	A
E _{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.9	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package Mounting Surface Temperature	300 (for 5s)	
	Weight	3.3.(Typical)	g

* Current is limited by package

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.012	Ω	V _{GS} = 4.5V, I _{D2} = 56A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-6.6	—	mV/°C	
G _{fs}	Forward Transconductance	32	—	—	S	V _{DS} = 10V, I _{D2} = 56A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V _{DS} = 48V, V _{GS} = 0V
		—	—	15		V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 10V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -10V
Q _G	Total Gate Charge	—	—	140	nC	I _{D1} = 56A
Q _{GS}	Gate-to-Source Charge	—	—	40		V _{DS} = 30V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	70		V _{GS} = 4.5V
t _{d(on)}	Turn-On Delay Time	—	—	90	ns	V _{DD} = 30V
t _r	Rise Time	—	—	310		I _{D1} = 56A
t _{d(off)}	Turn-Off Delay Time	—	—	140		R _G = 2.35Ω
t _f	Fall Time	—	—	35		V _{GS} = 4.5V
L _S + L _D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C _{iSS}	Input Capacitance	—	10220	—	pF	V _{GS} = 0V
C _{oSS}	Output Capacitance	—	2343	—		V _{DS} = 25V
C _{rSS}	Reverse Transfer Capacitance	—	40	—		f = 100kHz
R _G	Gate Resistance	—	0.56	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	56*	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	224		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 56A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	214	ns	T _J = 25°C, I _F = 56A, V _{DD} ≤ 30V
Q _{rr}	Reverse Recovery Charge	—	—	1.18	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

* Current is limited by package

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	0.5	°C/W
R _{θJ-PCB}	Junction-to-PC Board (soldered to 2 inch square cu clad board)	—	1.6	—	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 25V, starting T_J = 25°C, L = 0.26mH, Peak I_L = 56A, V_{GS} = 10V
- ③ I_{SD} ≤ 56A, di/dt ≤ 350A/μs, V_{DD} ≤ 60V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V_{GS} Bias. 10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V_{DS} Bias. 48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si) ¹		Units	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	60	—	V	V _{GS} = 0V, I _D = 250μA
V _{GS(th)}	Gate Threshold Voltage	1.0	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	V _{GS} = -10V
I _{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	V _{DS} = 48V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (TO-3)	—	0.010	Ω	V _{GS} = 4.5V, I _{D2} = 56A
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (SMD-2)	—	0.012	Ω	V _{GS} = 4.5V, I _{D2} = 56A
V _{SD}	Diode Forward Voltage	—	1.2	V	V _{GS} = 0V, I _S = 56A

1. Part numbers IRHLNA77064 and IRHLNA73064

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)					
			@ VGS = 0V	@ VGS = -2V	@ VGS = -4V	@ VGS = -5V	@ VGS = -6V	@ VGS = -7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	60	60	60	60	60	—
62 ± 5%	355 ± 7.5%	33 ± 7.5%	60	60	60	60	—	—
85 ± 5%	380 ± 7.5%	29 ± 7.5%	60	60	60	—	—	—

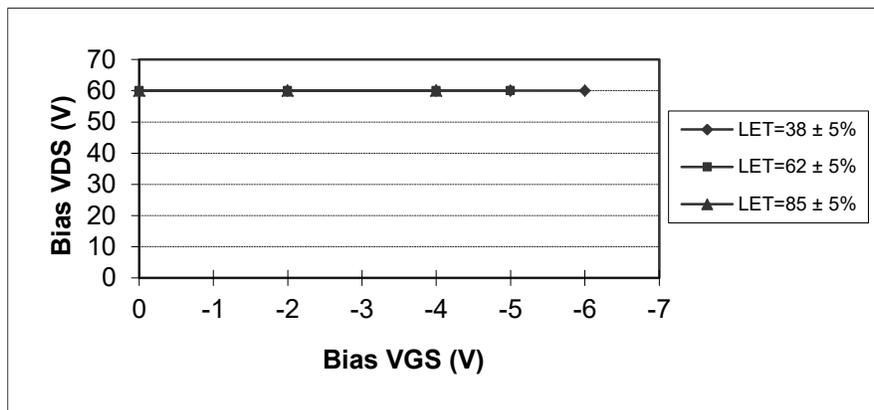


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

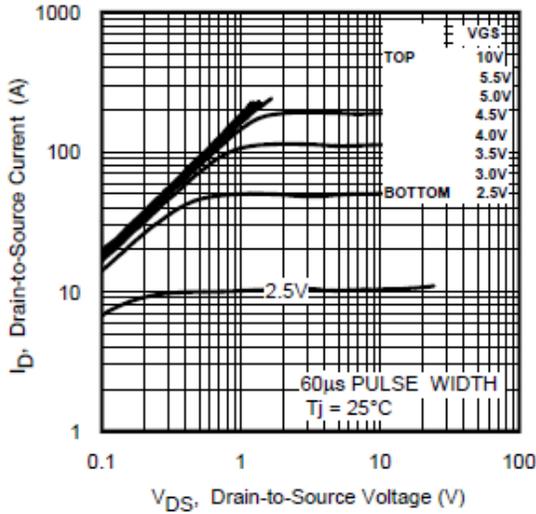


Fig 1. Typical Output Characteristics

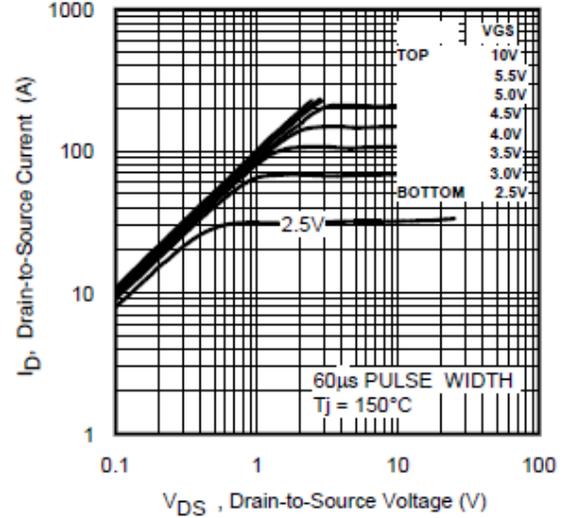


Fig 2. Typical Output Characteristics

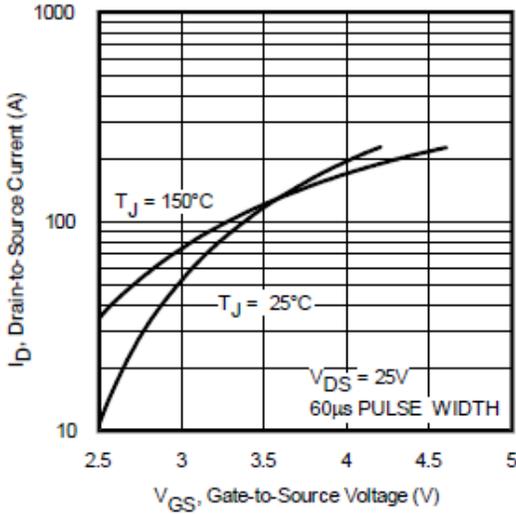


Fig 3. Typical Transfer Characteristics

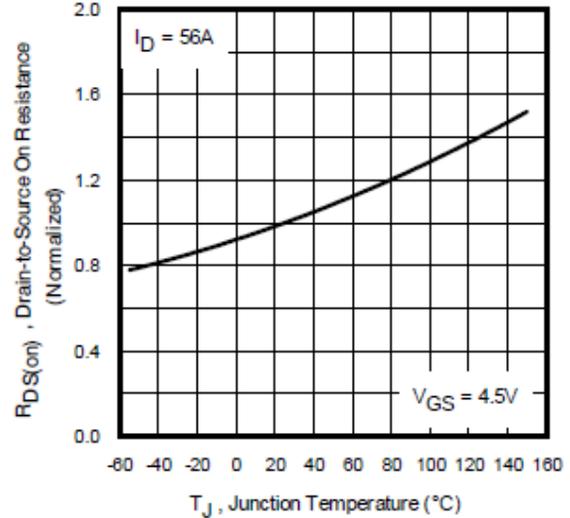


Fig 4. Normalized On-Resistance Vs. Temperature

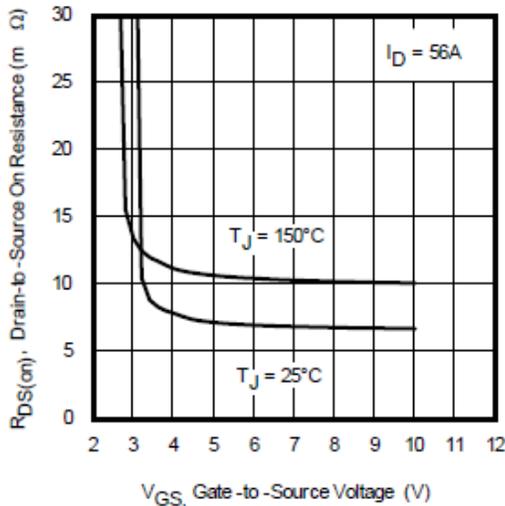


Fig 5. Typical On-Resistance Vs Gate Voltage

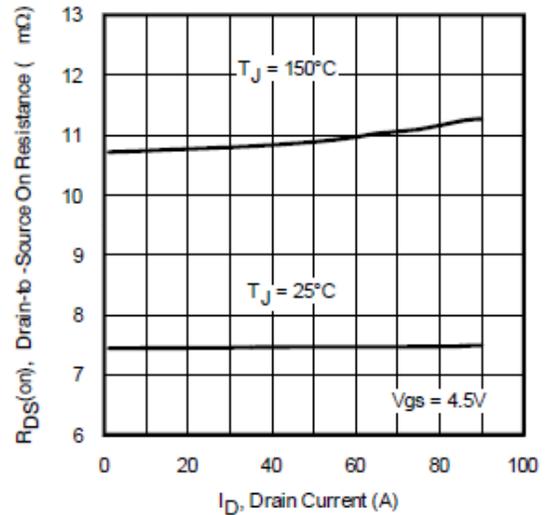


Fig 6. Typical On-Resistance Vs Drain Current

Pre-Irradiation

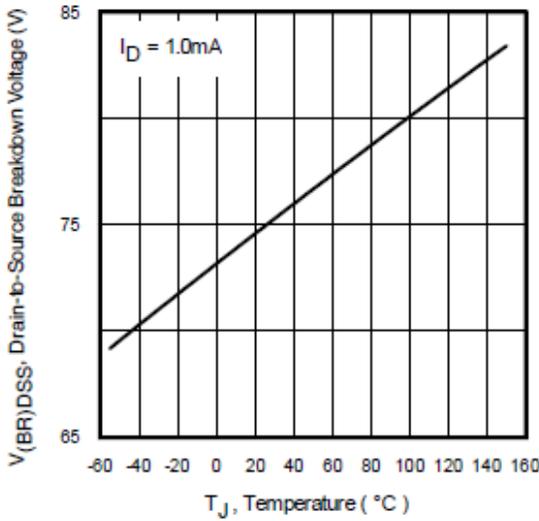


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

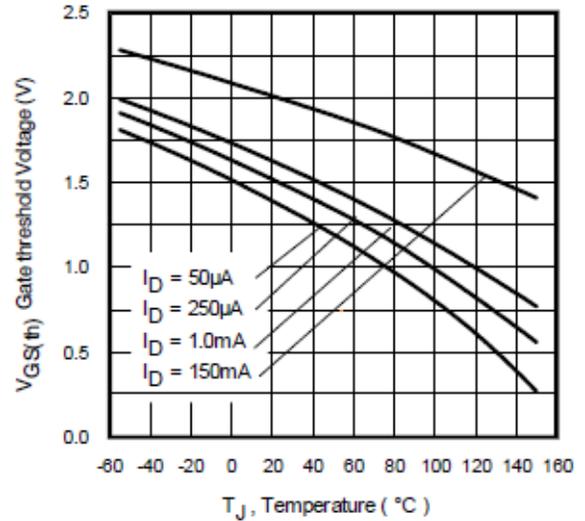


Fig 8. Typical Threshold Voltage Vs Temperature

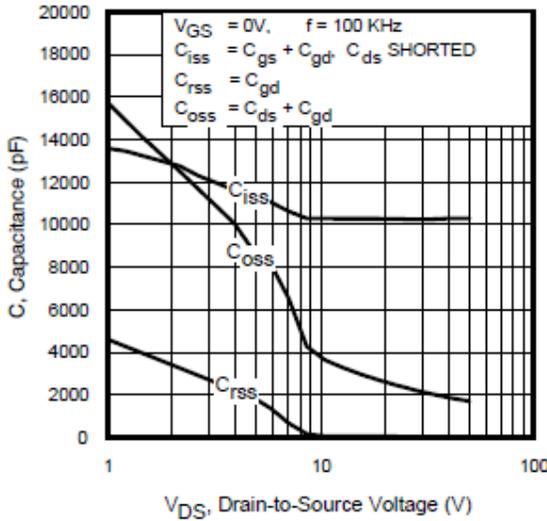


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

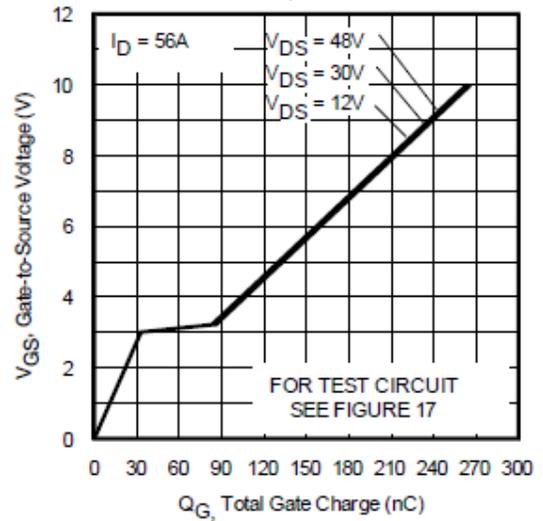


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

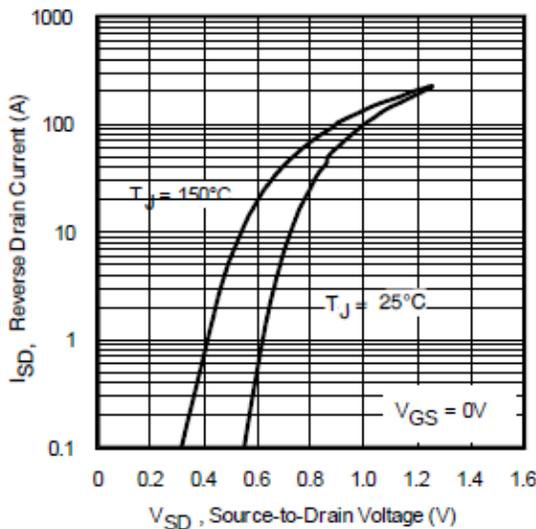


Fig 11. Typical Source-Drain Diode Forward Voltage

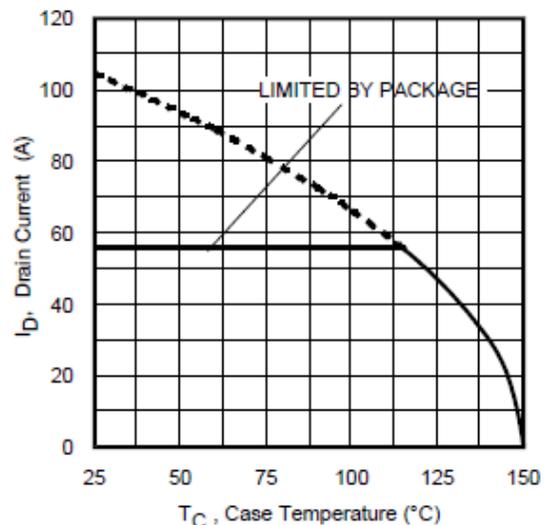


Fig 12. Maximum Drain Current Vs. Case Temperature

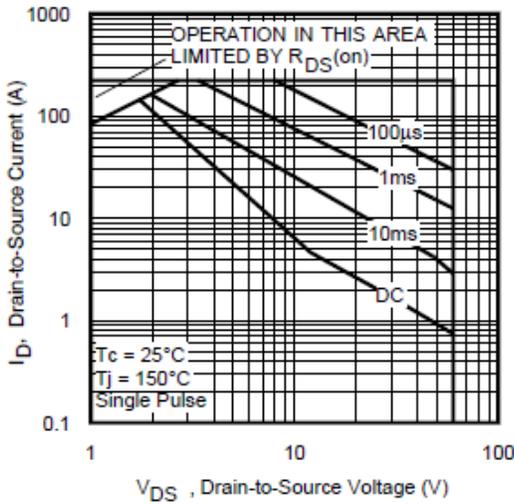


Fig 13. Maximum Safe Operating Area

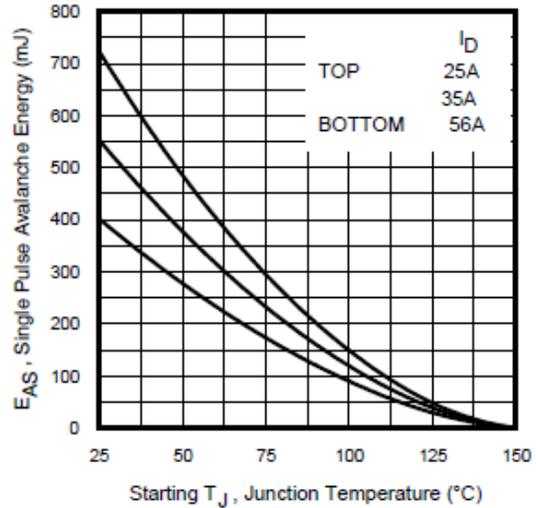


Fig 14. Maximum Avalanche Energy Vs. Drain Current

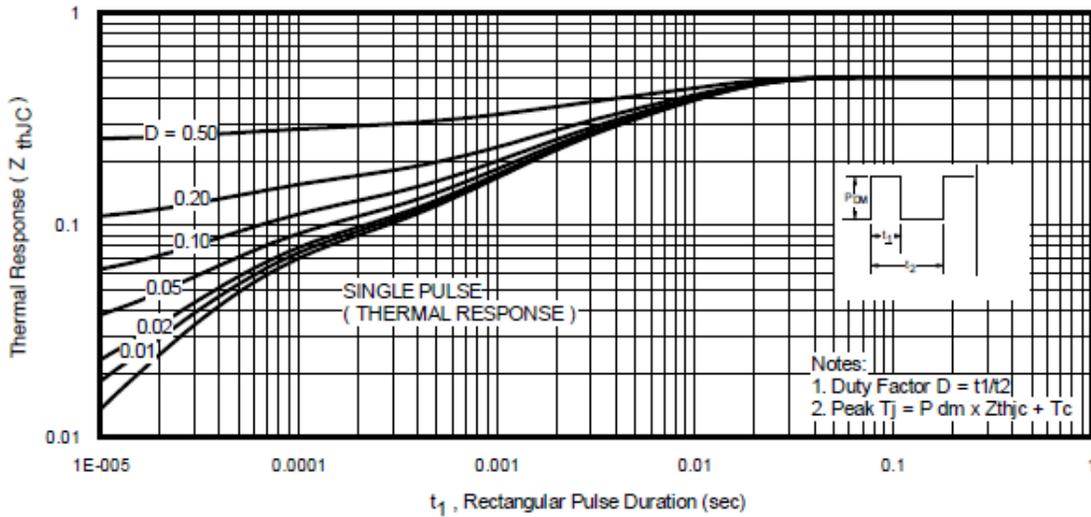


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

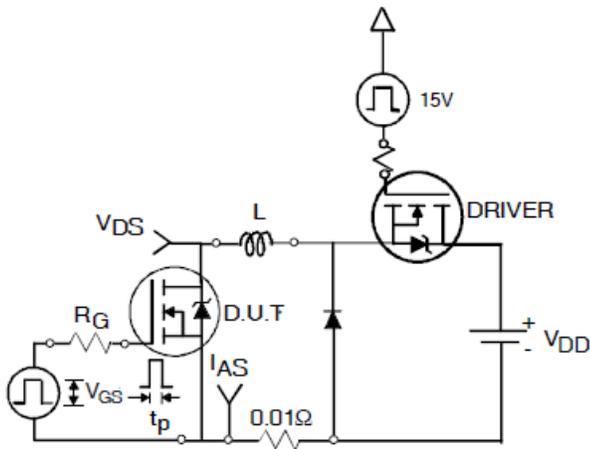


Fig 16a. Unclamped Inductive Test Circuit

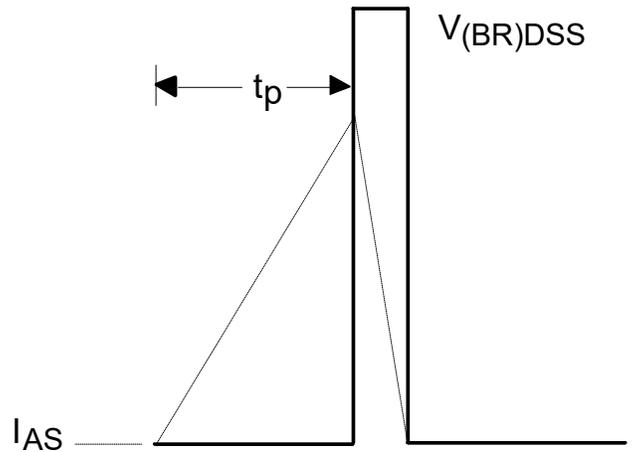


Fig 16b. Unclamped Inductive Waveforms

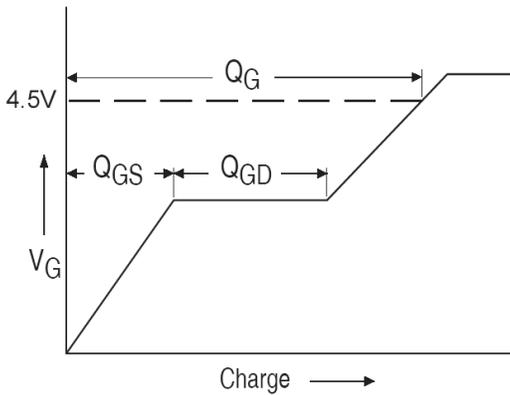


Fig 17a. Gate Charge Waveform

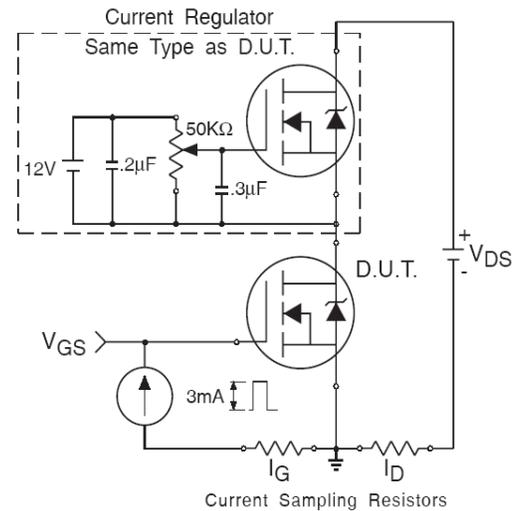


Fig 17b. Gate Charge Test Circuit

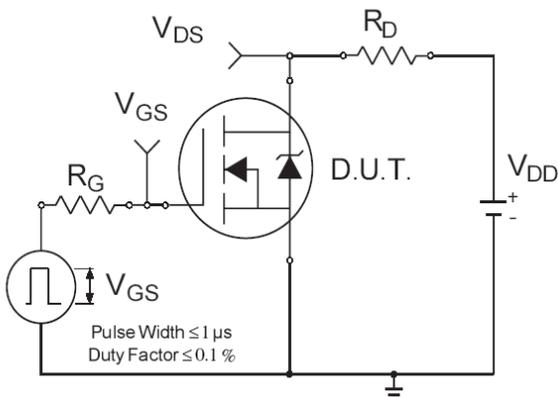


Fig 18a. Switching Time Test Circuit

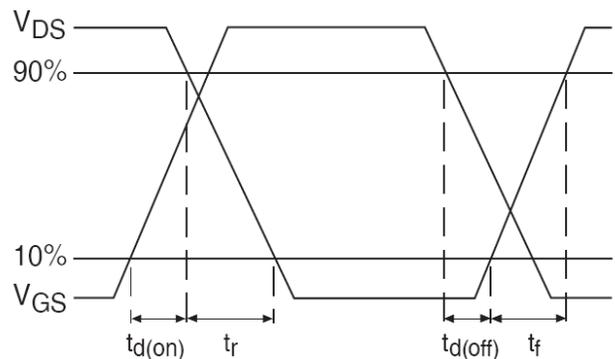
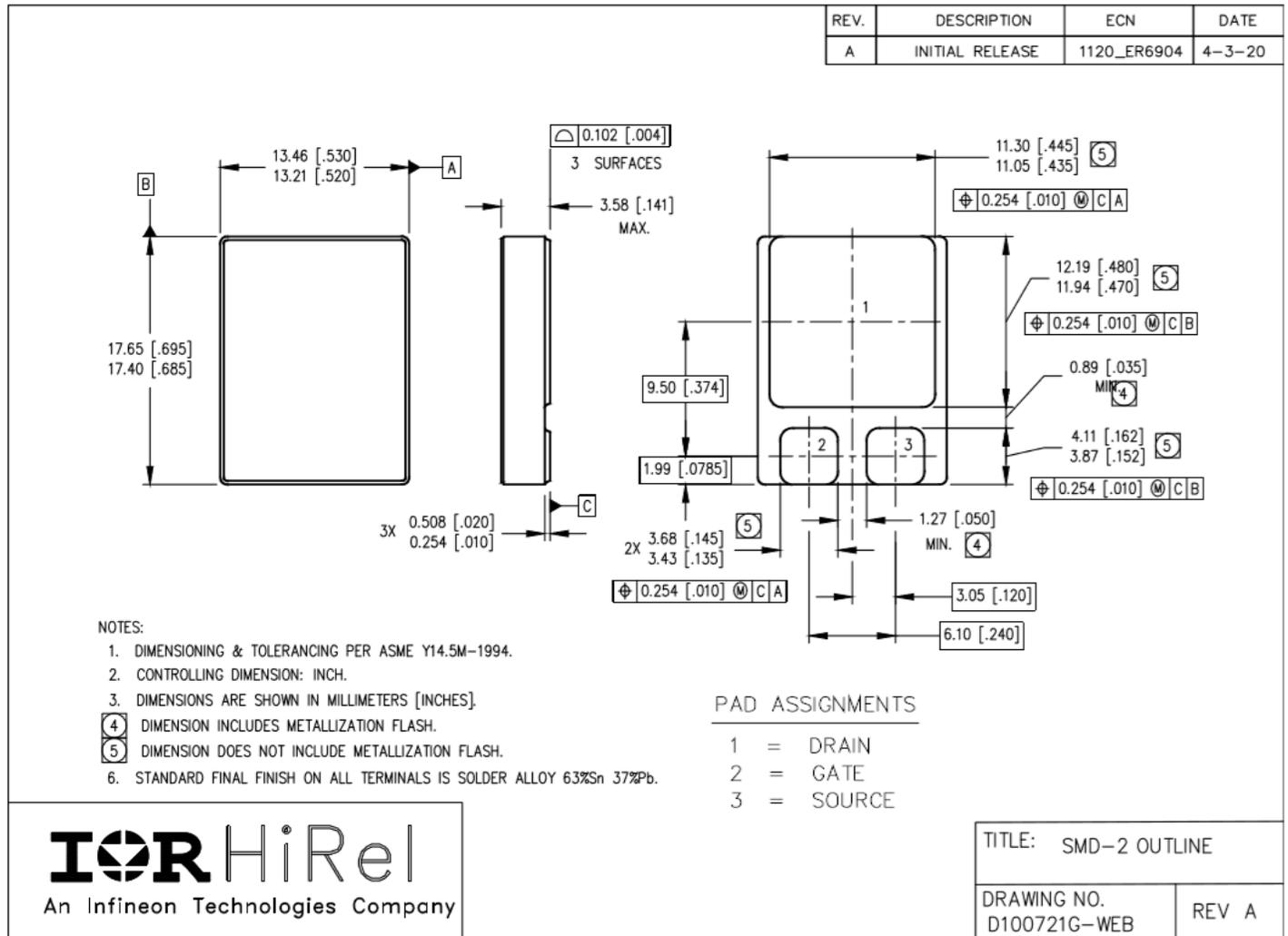


Fig 18b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [SMD-2](#)

Case Outline and Dimensions — SMD-2



IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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