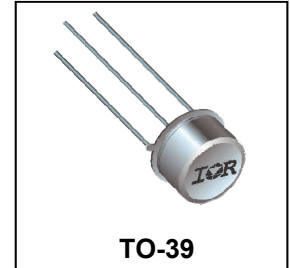


**RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
THRU-HOLE (TO-39)**

**20V, N-CHANNEL
R₈ TECHNOLOGY**

Product Summary

Part Number	Radiation Level	RDS(on)	I _D
IRHLF87Y20	100 kRads (Si)	32mΩ	12A*
IRHLF83Y20	300 kRads (Si)	32mΩ	12A*



Description

IRHLF87Y20 is part of the International Rectifier HiRel family of products. IR HiRel R8 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Features

- 5V CMOS and TTL Compatible
- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Light Weight
- ESD Rating: Class 1B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = 4.5V, T _C = 25°C	Continuous Drain Current	12*	A
I _{D2} @ V _{GS} = 4.5V, T _C = 100°C	Continuous Drain Current	10.2	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	48	
P _D @ T _C = 25°C	Maximum Power Dissipation	15.6	W
	Linear Derating Factor	0.13	W/°C
V _{GS}	Gate-to-Source Voltage	± 12	V
E _{AS}	Single Pulse Avalanche Energy ②	43	mJ
I _{AR}	Avalanche Current ①	12	A
E _{AR}	Repetitive Avalanche Energy ①	1.6	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.85	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063in/1.6mm from case for 10s)	
	Weight	0.98 (Typical)	g

* Current is limited by package

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.03	—	V/°C	Reference to 25°C, $I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	27	32	mΩ	$V_{GS} = 4.5V, I_{D2} = 10.2A$ ④
		—	26	31	mΩ	$V_{GS} = 7.0V, I_{D2} = 10.2A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.3	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.7	—	mV/°C	
G_{fs}	Forward Transconductance	20	—	—	S	$V_{DS} = 15V, I_{D2} = 10.2A$ ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	10		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ C$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -12V$
Q_G	Total Gate Charge	—	20	27	nC	$I_{D1} = 12A$
Q_{GS}	Gate-to-Source Charge	—	4.0	5.7		$V_{DS} = 10V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	4.5	8.5		$V_{GS} = 5.5V$
$t_{d(on)}$	Turn-On Delay Time	—	17	21	ns	$I_{D1} = 12A$ **
t_r	Rise Time	—	63	114		$V_{DD} = 10V$
$t_{d(off)}$	Turn-Off Delay Time	—	26	30		$R_G = 2.35\Omega$
t_f	Fall Time	—	12	22		$V_{GS} = 5.5V$
$L_S + L_D$	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm / 0.25in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
C_{iss}	Input Capacitance	—	2431	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	592	—		$V_{DS} = 20V$
C_{rss}	Reverse Transfer Capacitance	—	143	—		$f = 1.0MHz$
R_G	Gate Resistance	—	0.94	—	Ω	$f = 1.0MHz, \text{open drain}$

** Switching speed maximum limits are based on manufacturing test equipment and capability.

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	12*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	48		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ C, I_S = 12A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	—	41	ns	$T_J = 25^\circ C, I_F = 12A, V_{DD} \leq 20V$
Q_{rr}	Reverse Recovery Charge	—	—	51	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	8.0	°C/W

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 20V$, starting $T_J = 25^\circ C$, $L = 0.6mH$, Peak $I_L = 12A$, $V_{GS} = 12V$
- ③ $I_{SD} \leq 12A$, $di/dt \leq 423A/\mu s$, $V_{DD} \leq 20V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.** 16 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si) ¹		Units	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	20	—	V	V _{GS} = 0V, I _D = 250μA
V _{GS(th)}	Gate Threshold Voltage	1.0	2.3	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 12V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	V _{GS} = -12V
I _{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	V _{DS} = 16V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (TO-3)	—	32	mΩ	V _{GS} = 4.5V, I _{D2} = 10.2A
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (TO-39)	—	32	mΩ	V _{GS} = 4.5V, I _{D2} = 10.2A
V _{SD}	Diode Forward Voltage	—	1.2	V	V _{GS} = 0V, I _S = 12A

1. Part numbers IRHLF87Y20 and IRHLF83Y20

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)					
			@ VGS = 0V	@ VGS = -1V	@ VGS = -2V	@ VGS = -3V	@ VGS = -5V	@ VGS = -10V
37 ± 5%	298 ± 5%	38 ± 5%	18	18			8	4
60 ± 5%	320 ± 5%	32 ± 7.5%	18	18	15	12	8	—
81 ± 5%	375 ± 7.5%	28 ± 7.5%	18	18		12	8	—

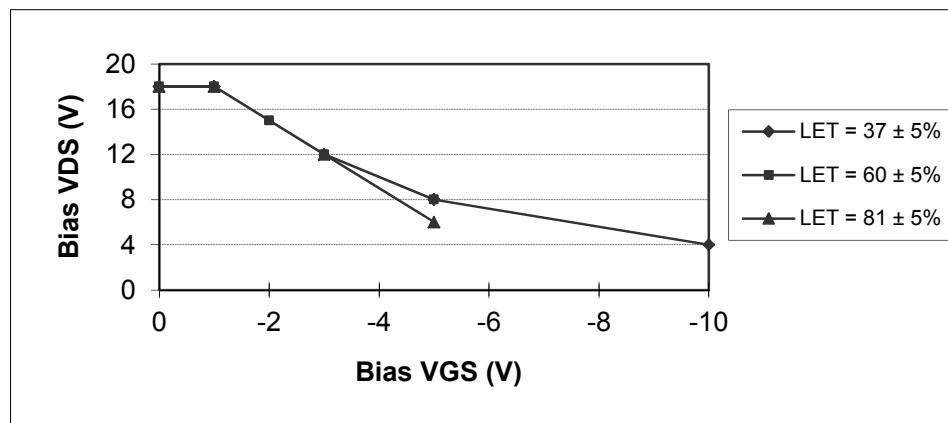


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

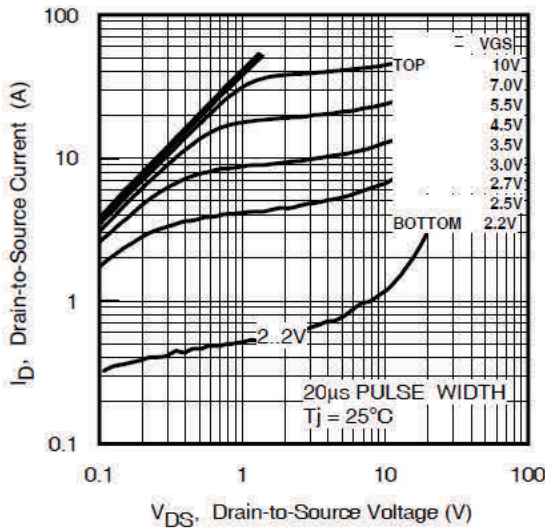


Fig 1. Typical Output Characteristics

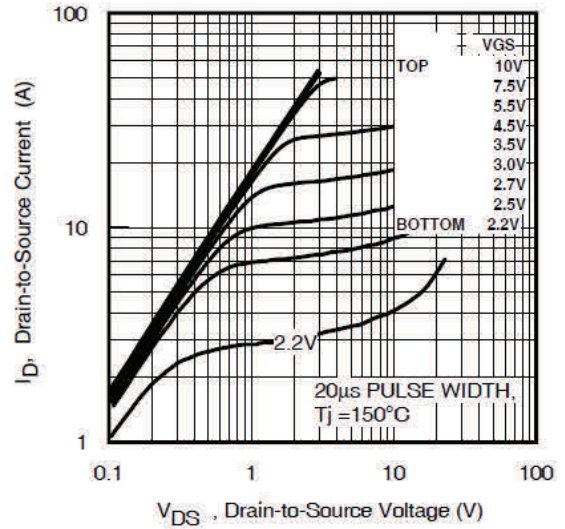


Fig 2. Typical Output Characteristics

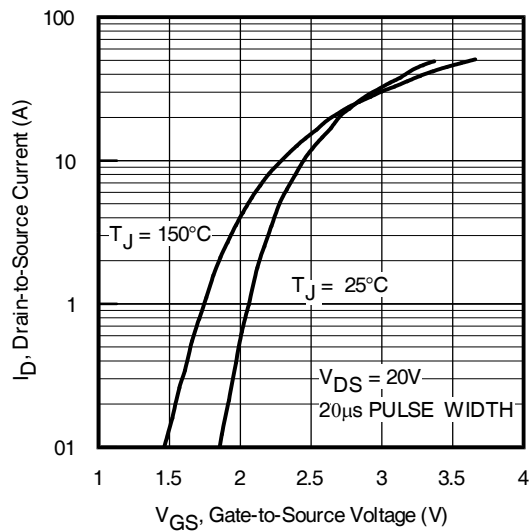


Fig 3. Typical Transfer Characteristics

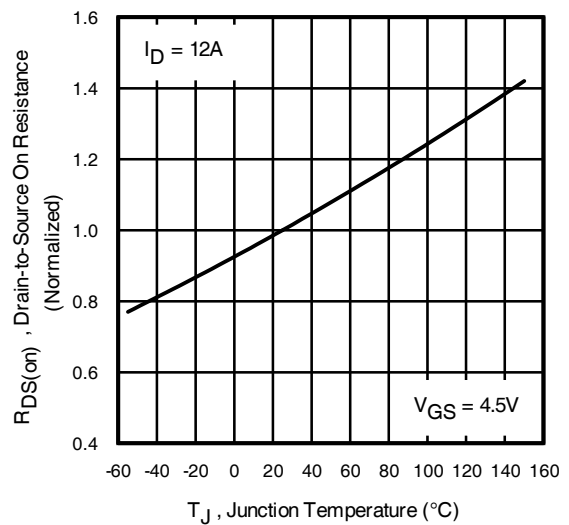


Fig 4. Normalized On-Resistance Vs. Temperature

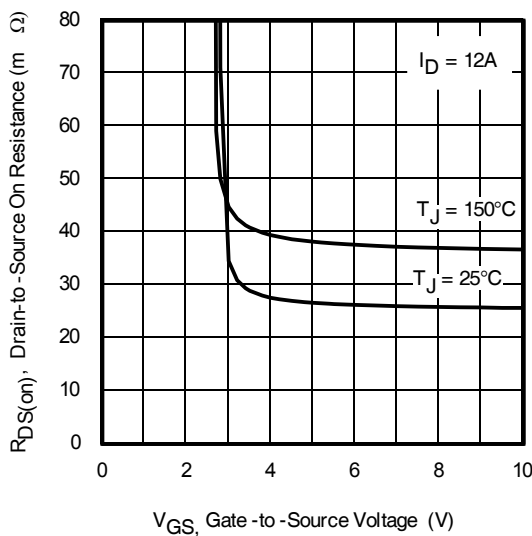


Fig 5. Typical On-Resistance Vs Gate Voltage

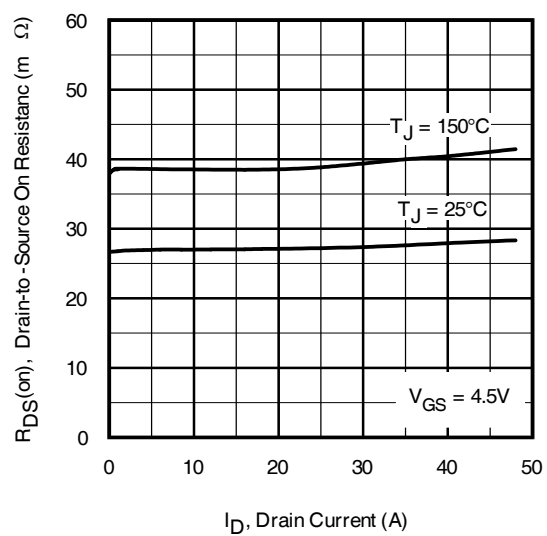


Fig 6. Typical On-Resistance Vs Drain Current

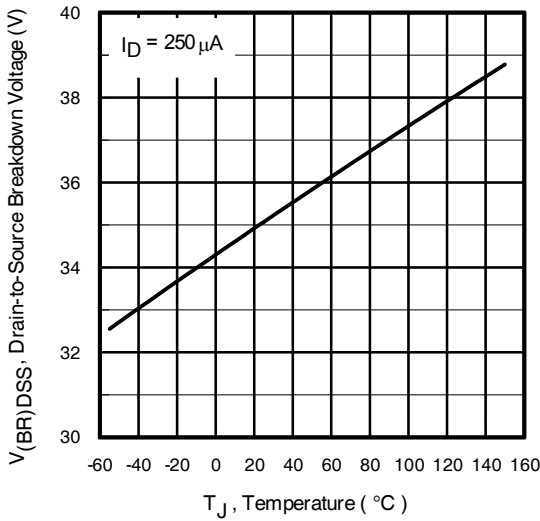


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

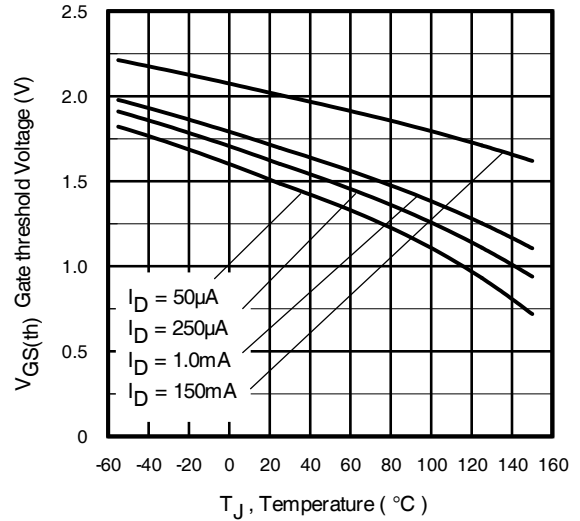


Fig 8. Typical Threshold Voltage Vs Temperature

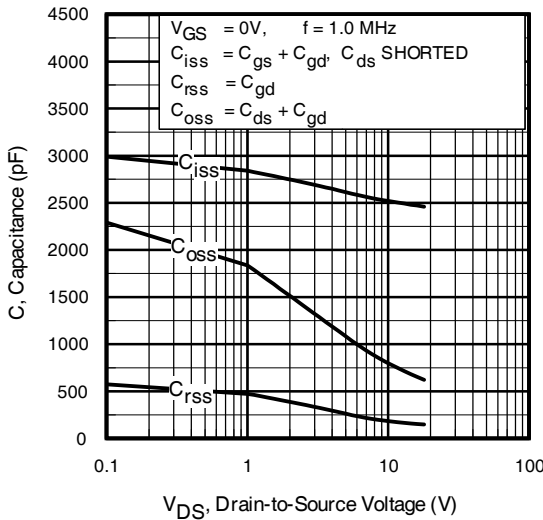


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

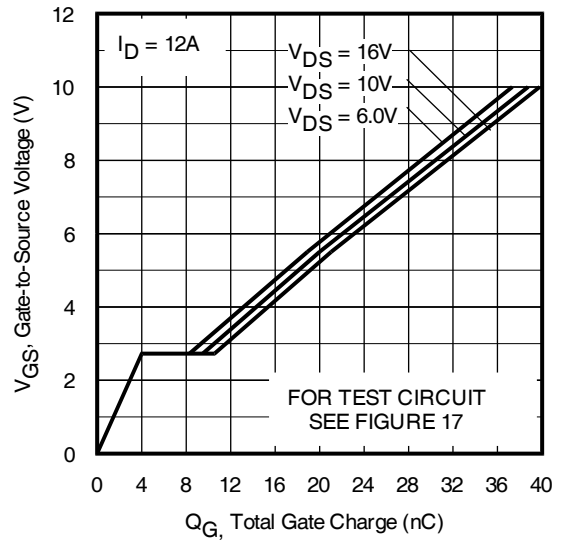


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

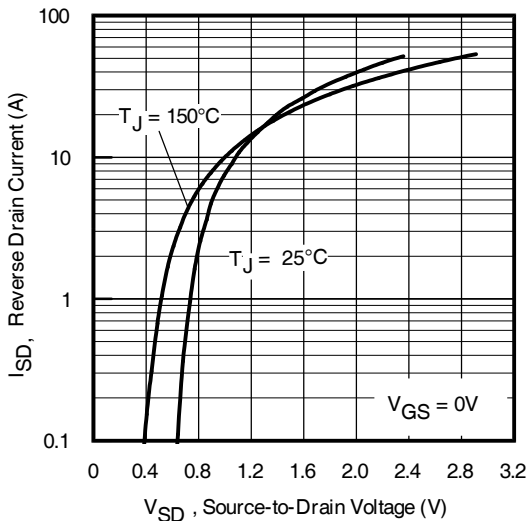


Fig 11. Typical Source-Drain Diode Forward Voltage

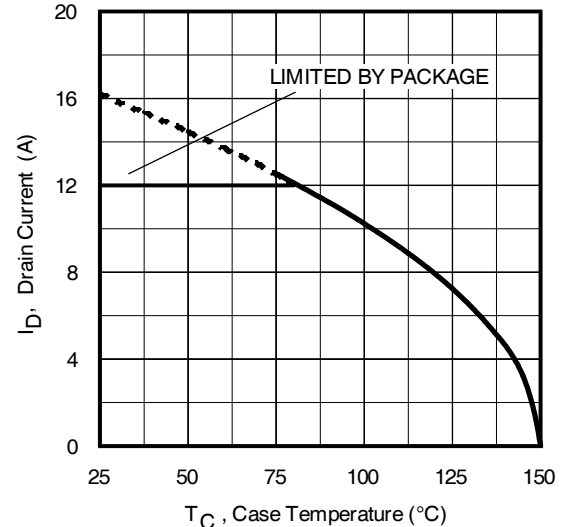


Fig 12. Maximum Drain Current Vs. Case Temperature

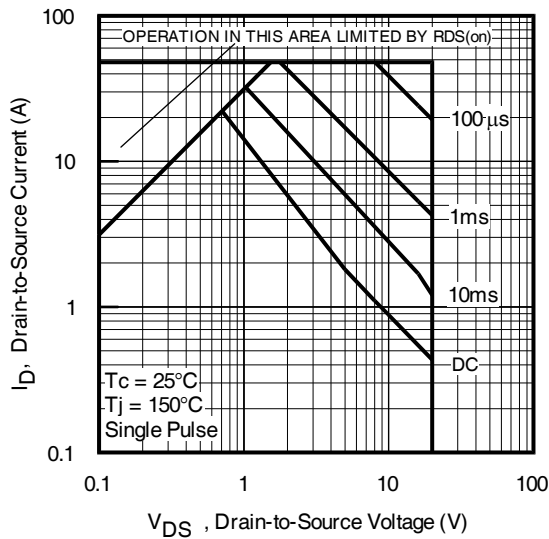


Fig 13. Maximum Safe Operating Area

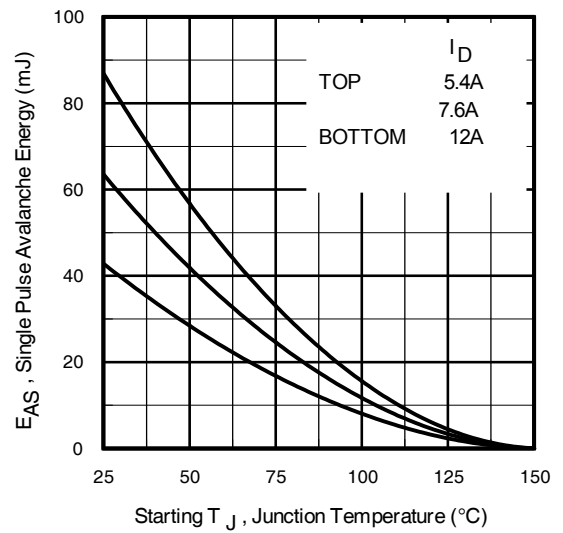


Fig 14. Maximum Avalanche Energy Vs. Drain Current

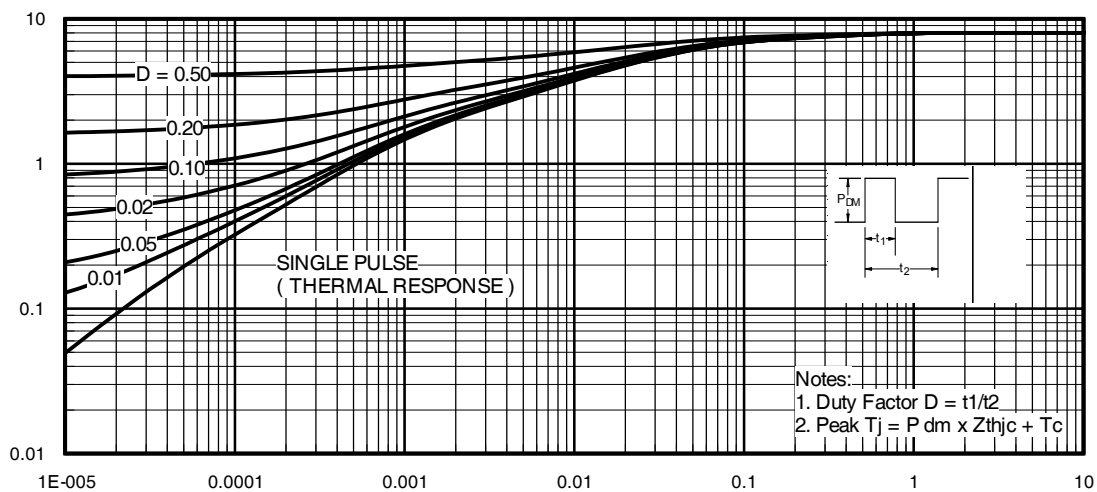


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

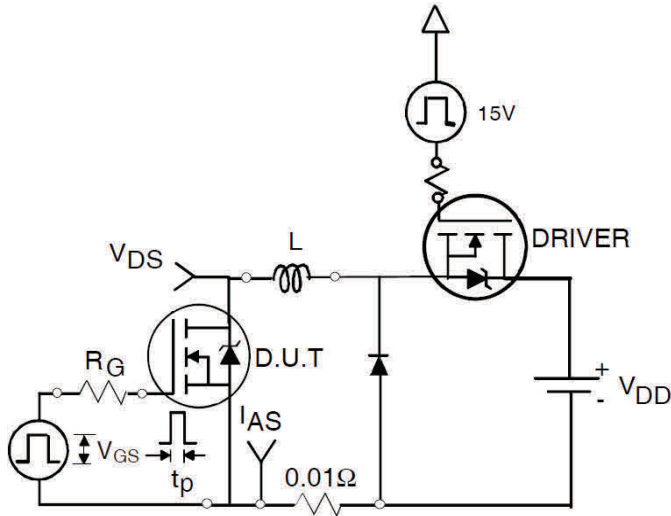


Fig 16a. Unclamped Inductive Test Circuit

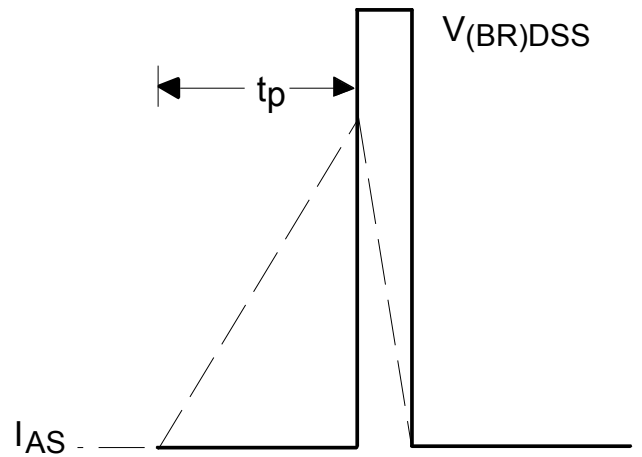


Fig 16b. Unclamped Inductive Waveforms

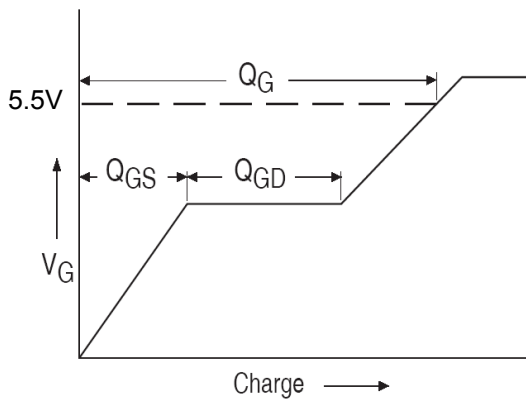


Fig 17a. Gate Charge Waveform

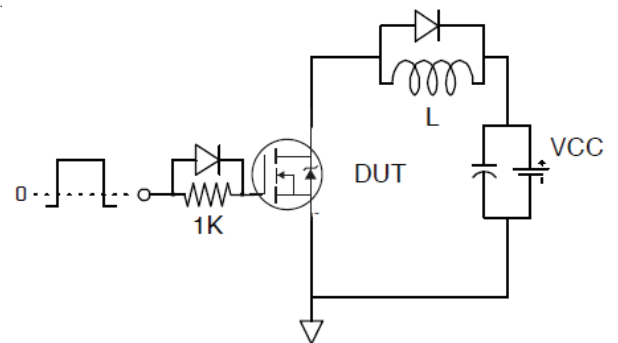


Fig 17b. Gate Charge Test Circuit

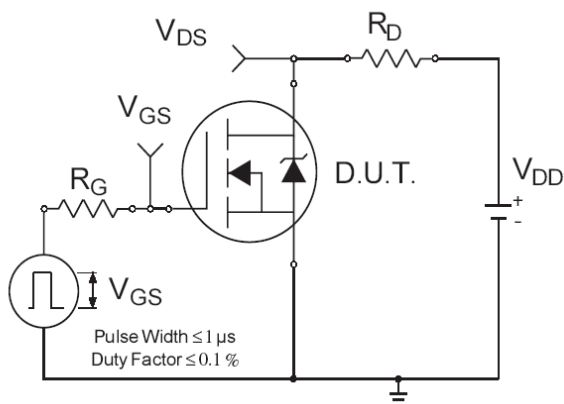


Fig 18a. Switching Time Test Circuit

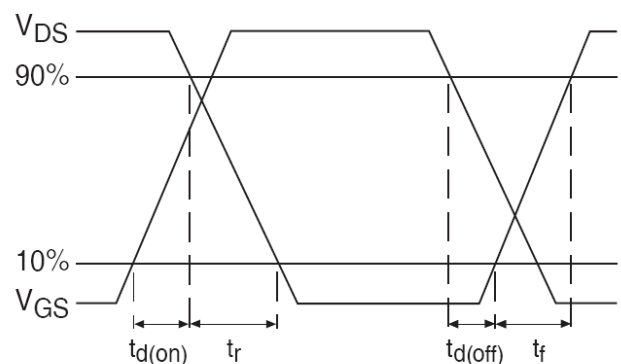
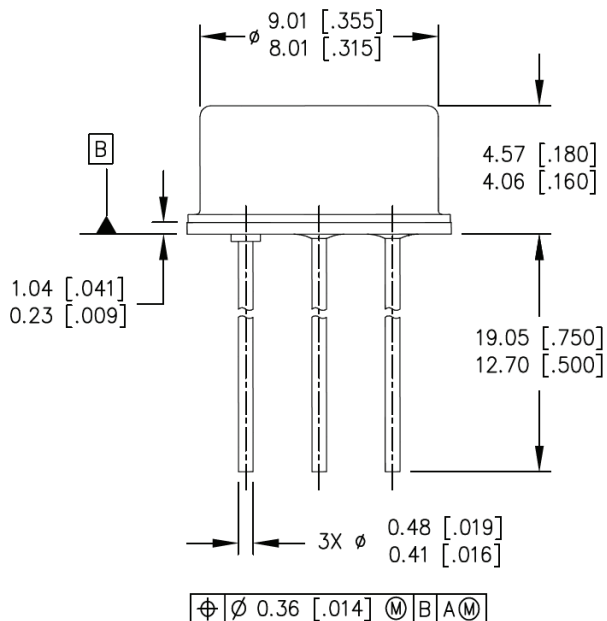
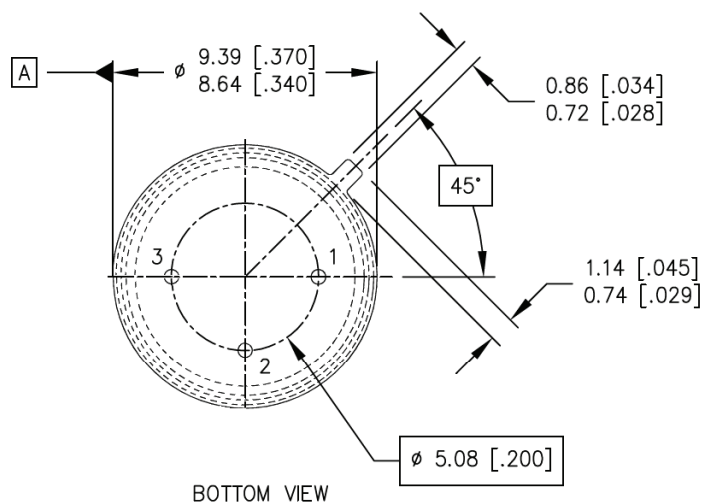


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions - TO-205AF (TO-39)



SIDE VIEW



BOTTOM VIEW

LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN (CONNECTED TO THE CASE)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

IMPORTANT NOTICE

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