

RADIATION HARDENED LOGIC LEVEL POWER MOSFET THRU-HOLE TO-205AF (TO-39)

250V, N-CHANNEL R7 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I _D
IRHLF7S7214	100 kRads(Si)	1.0Ω	3.3A
IRHLF7S3214	300 kRads(Si)	1.0Ω	3.3A

Description

IR HiRel R7 S-Line Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.



Features

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Light Weight
- Hermetically Sealed
- ESD Rating: Class 1B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol Parameter		Value	Units
I _{D1} @ V _{GS} = 4.5V, T _C = 25°C	Continuous Drain Current	3.3	
I _{D2} @ V _{GS} = 4.5V, T _C = 100°C	Continuous Drain Current	2.1	Α
IDM @ Tc = 25°C	Pulsed Drain Current ①	13.2	
P _D @T _C = 25°C	Maximum Power Dissipation	22.7	W
	Linear Derating Factor	0.18	W/°C
V_{GS}	V _{GS} Gate-to-Source Voltage		V
E _{AS}	E _{AS} Single Pulse Avalanche Energy ②		mJ
I _{AR}	Avalanche Current ①	3.3	Α
E _{AR}	Repetitive Avalanche Energy ①	2.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.29	V/ns
T_J	Operating Junction and	-55 to + 150	
T _{STG} Storage Temperature Range		-33 to + 130	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for	
	Weight	0.98 (Typical)	g

For Footnotes, refer to the page 2.



Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Symbol Parameter		Parameter Min. Typ. Max. U		Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	250			V	$V_{GS} = 0V, I_{D} = 250\mu A$
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.22		V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance			1.0	Ω	V _{GS} = 4.5V, I _{D2} = 2.1A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0		2.0	V	V - V I - 250A
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient		-5.2		mV/°C	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
Gfs	Forward Transconductance	2.5			S	V _{DS} = 15V, I _{D2} = 2.1A ④
I _{DSS}	Zero Gate Voltage Drain Current			1.0		$V_{DS} = 200V, V_{GS} = 0V$
	Zero Gate Voltage Drain Current			15	μA	$V_{DS} = 200V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I _{GSS}	Gate-to-Source Leakage Forward			100	nA	V _{GS} = 10V
	Gate-to-Source Leakage Reverse			-100	IIA	V _{GS} = -10V
Q _G	Total Gate Charge			18		I _{D1} = 3.3A
Q_{GS}	Gate-to-Source Charge			5.0	nC	V _{DS} = 125V
Q_{GD}	Gate-to-Drain ('Miller') Charge			12		V _{GS} = 4.5V
$t_{d(on)}$	Turn-On Delay Time			27		$V_{DD} = 125V$
tr	Rise Time			57	no	I _{D1} = 3.3A
$t_{d(off)}$	Turn-Off Delay Time			45	ns	$R_G = 7.5\Omega$
t _f	Fall Time			55		V _{GS} = 5.0V
Ls +L _D	Total Inductance		7.0		nH	Measured from Drain lead (6mm /0.25 in from package) to Source lead (6mm/0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
C _{iss}	Input Capacitance		611			V _{GS} = 0V
C _{oss}	Output Capacitance		62		pF	V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance		0.64			f = 1.0MHz
R _G	Gate Resistance		8.0		Ω	f = 1.0 MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current (Body Diode)			3.3	۸	
I _{SM}	Pulsed Source Current (Body Diode) ①			13.2	Α	
V _{SD}	Diode Forward Voltage			1.2	V	$T_J = 25^{\circ}C, I_S = 3.3A, V_{GS} = 0V$
t _{rr}	Reverse Recovery Time			371	ns	$T_J = 25^{\circ}C, I_F = 3.3A, V_{DD} \le 25V$
Q _{rr}	Reverse Recovery Charge			1.05	μC	di/dt = 100A/µs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

Symbol	Parameter	Min.	Тур.	Max.	Units
$R_{ heta JC}$	Junction-to-Case			5.5	°C/W

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- $^{\circ}$ V_{DD} = 50V, starting T_J = 25°C, L =5.4mH, Peak I_L = 3.3A, V_{GS} = 10V
- $\exists \quad I_{SD} \leq 3.3A, \ di/dt \leq 372A/\mu s, \ V_{DD} \leq 250V, \ T_J \leq 150^{\circ}C$
- \odot Total Dose Irradiation with V_{GS} Bias. 10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V_{DS} Bias. 200 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.



Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation \$6

Symbol	Parameter	Up to 300	kRads (Si) 1	Units	Test Conditions	
Cymbol	i didilictei	Min.	Max.	Oilles	rest conditions	
BV_{DSS}	Drain-to-Source Breakdown Voltage	250		V	$V_{GS} = 0V, I_{D} = 250\mu A$	
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
I _{GSS}	Gate-to-Source Leakage Forward		100	nA	V _{GS} = 10V	
I _{GSS}	Gate-to-Source Leakage Reverse		-100	nA	V _{GS} = -10V	
I _{DSS}	Zero Gate Voltage Drain Current		1.0	μA	V _{DS} = 200V, V _{GS} = 0V	
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)		0.88	Ω	V _{GS} = 4.5V, I _{D2} = 2.1A	
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-39)		1.0	Ω	V _{GS} = 4.5V, I _{D2} = 2.1A	
V_{SD}	Diode Forward Voltage		1.2	V	$V_{GS} = 0V, I_{S} = 3.3A$	

^{1.} Part numbers IRHLF7S7214 and IRHLF7S3214

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET Energy Range				VDS (V)						
ION	(MeV/(mg/cm ²))	Energy (MeV)	Range (µm)	@ VGS = 0V	@ VGS = -2V	@ VGS = -4V	@ VGS = -5V	@ VGS = -6V	@ VGS = -7V	
Kr	34.1	573	69.6	250	250	250	250	250	250	
Xe	56.8	1010	79.7	250	250	250				

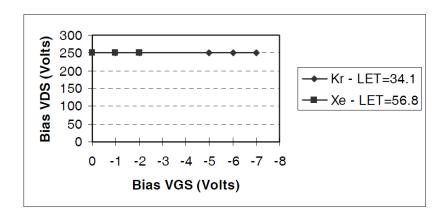


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

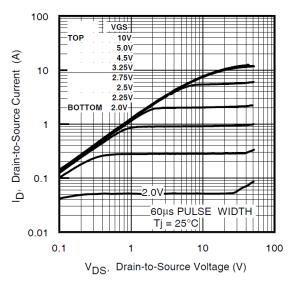


Fig 1. Typical Output Characteristics

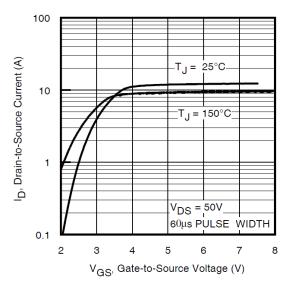


Fig 3. Typical Transfer Characteristics

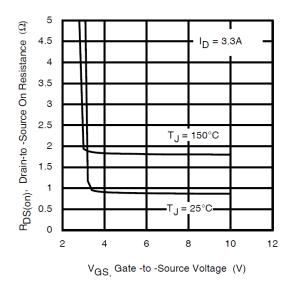


Fig 5. Typical On-Resistance Vs Gate Voltage

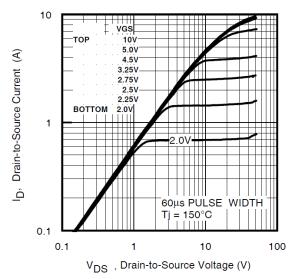


Fig 2. Typical Output Characteristics

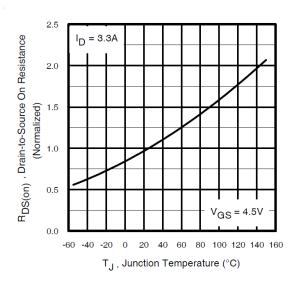


Fig 4. Normalized On-Resistance Vs. Temperature

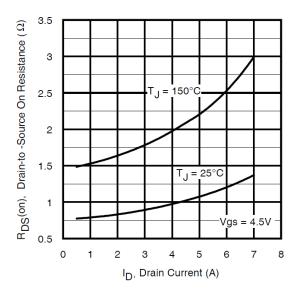


Fig 6. Typical On-Resistance Vs Drain Current

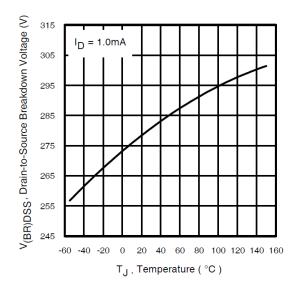


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

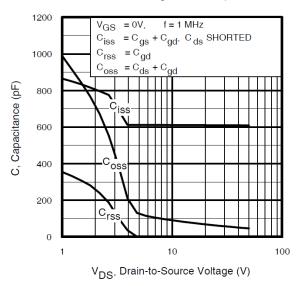


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

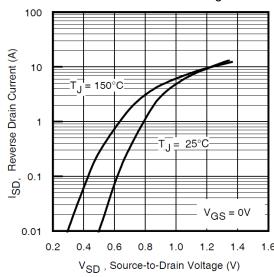


Fig 11. Typical Source-Drain Diode Forward Voltage

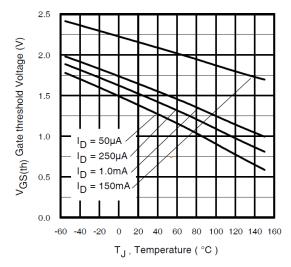


Fig 8. Typical Threshold Voltage Vs Temperature

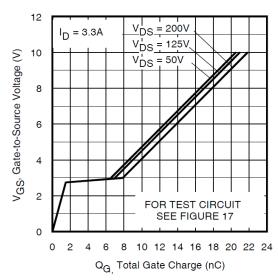


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

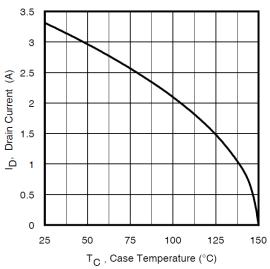


Fig 12. Maximum Drain Current Vs.Case Temperature

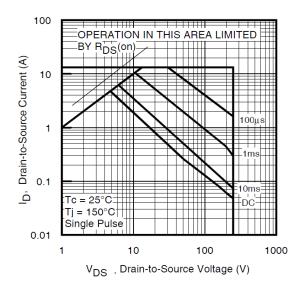


Fig 13. Maximum Safe Operating Area

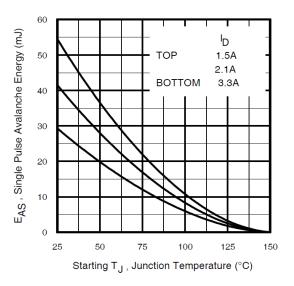


Fig 14. Maximum Avalanche Energy Vs. Drain Current

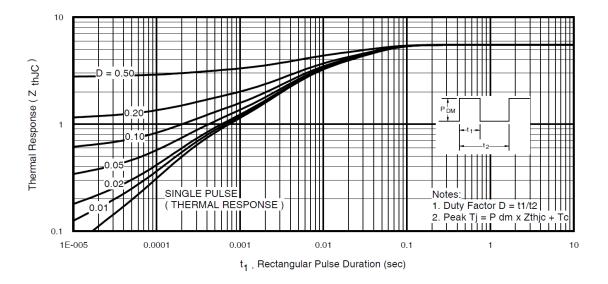


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

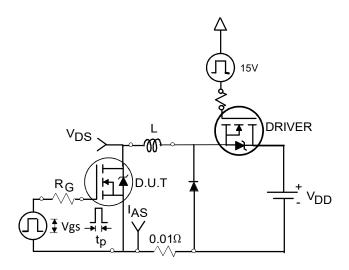


Fig 16a. Unclamped Inductive Test Circuit

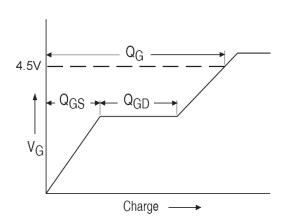


Fig 17a. Gate Charge Waveform

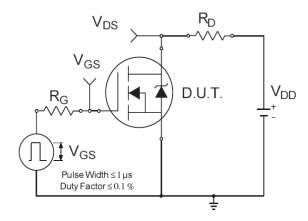


Fig 18a. Switching Time Test Circuit

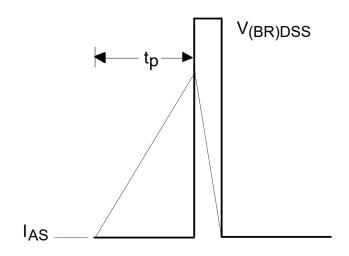


Fig 16b. Unclamped Inductive Waveforms

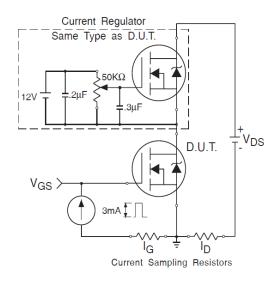


Fig 17b. Gate Charge Test Circuit

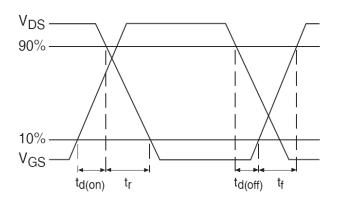
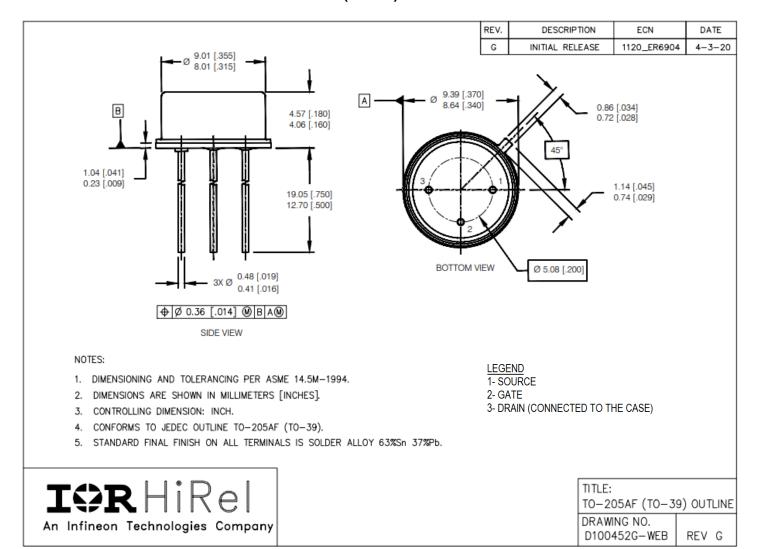


Fig 18b. Switching Time Waveforms



Note: For the most updated package outline, please see the website: TO-205AF (TO-39)

Case Outline and Dimensions - TO-205AF (TO-39)





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