

**RADIATION HARDENED  
POWER MOSFET  
THRU-HOLE TO-205AF (TO-39)**
**IRHF7130  
JANSR2N7261**
**100V, N-CHANNEL  
REF: MIL-PRF-19500/601  
RAD Hard™HEXFET® TECHNOLOGY**
**Product Summary**

Part Number	Radiation Level	RDS(on)	I <sub>D</sub>	QPL Part Number
IRHF7130	100 kRads(Si)	0.18Ω	8.0A	JANSR2N7261
IRHF3130	300 kRads(Si)	0.18Ω	8.0A	JANSF2N7261
IRHF5130	500 kRads(Si)	0.18Ω	8.0A	JANSG2N7261
IRHF8130	1000 kRads(Si)	0.18Ω	8.0A	JANSH2N7261

**Description**

IR HiRel RADHard™ HEXFET® MOSFET technology provides high performance power MOSFETs for space applications. This technology has long history of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical

**Features**

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

**Absolute Maximum Ratings**

Pre-Irradiation			
Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 25°C	Continuous Drain Current	8.0	A
I <sub>D2</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 100°C	Continuous Drain Current	5.0	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	32	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	25	W
	Linear Derating Factor	0.20	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	130	mJ
I <sub>AR</sub>	Avalanche Current ①	8.0	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	0.98 (Typical)	g

For Footnotes, refer to the page 2.

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 1.0\text{mA}$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.18	$\Omega$	$V_{GS} = 12V, I_{D2} = 5.0\text{A}$ ④
		—	—	0.185		$V_{GS} = 12V, I_{D1} = 8.0\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 1.0\text{mA}$
$Gfs$	Forward Transconductance	2.5	—	—	S	$V_{DS} = 15V, I_{D2} = 5.0\text{A}$ ④
$I_{DSS}$	Zero Gate Voltage Drain Current	—	—	25	$\mu\text{A}$	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
$Q_G$	Total Gate Charge	—	—	50	nC	$I_{D1} = 8.0\text{A}$
$Q_{GS}$	Gate-to-Source Charge	—	—	10		$V_{DS} = 50V$
$Q_{GD}$	Gate-to-Drain ('Miller') Charge	—	—	20		$V_{GS} = 12V$
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	$V_{DD} = 50V$
$t_r$	Rise Time	—	—	32		$I_{D1} = 8.0\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	—	40		$R_G = 7.5\Omega$
$t_f$	Fall Time	—	—	40		$V_{GS} = 12V$
$L_s + L_D$	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
$C_{iss}$	Input Capacitance	—	1100	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	310	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	55	—		$f = 1.0\text{MHz}$

**Source-Drain Diode Ratings and Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	8.0	A	
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	32		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 8.0\text{A}, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	—	270	ns	$T_J = 25^\circ\text{C}, I_F = 8.0\text{A}, V_{DD} \leq 50V$
$Q_{rr}$	Reverse Recovery Charge	—	—	3.0		$dI/dt = 100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_s + L_D$ )				

**Thermal Resistance**

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	5.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical Socket Mount)	—	—	175	

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 25V$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 4.1\text{mH}$ , Peak  $I_L = 3.5\text{A}$ ,  $V_{GS} = 10V$
- ③  $I_{SD} \leq 3.5\text{A}$ ,  $dI/dt \leq 140\text{A}/\mu\text{s}$ ,  $V_{DD} \leq 100V$ ,  $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\ \mu\text{s}$ ; Duty Cycle  $\leq 2\%$
- ⑤ Total Dose Irradiation with  $V_{GS}$  Bias. 12 volt  $V_{GS}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with  $V_{DS}$  Bias. 80 volt  $V_{DS}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

## Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics @  $T_j = 25^\circ\text{C}$ , Post Total Dose Irradiation ⑤⑥**

Symbol	Parameter	100 kRads (Si) <sup>1</sup>		Up to 300k - 1000 kRads (Si) <sup>2</sup>		Units	Test Conditions
		Min.	Max.	Min.	Max.		
$\text{BV}_{\text{DSS}}$	Drain-to-Source Breakdown Voltage	100	—	100	—	V	$\text{V}_{\text{GS}} = 0\text{V}$ , $\text{I}_D = 1.0\text{mA}$
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	2.0	4.0	1.25	4.5	V	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$ , $\text{I}_D = 1.0\text{mA}$
$\text{I}_{\text{GSS}}$	Gate-to-Source Leakage Forward	—	100	—	100	nA	$\text{V}_{\text{GS}} = 20\text{V}$
$\text{I}_{\text{GSS}}$	Gate-to-Source Leakage Reverse	—	-100	—	-100	nA	$\text{V}_{\text{GS}} = -20\text{V}$
$\text{I}_{\text{DSS}}$	Zero Gate Voltage Drain Current	—	25	—	25	$\mu\text{A}$	$\text{V}_{\text{DS}} = 80\text{V}$ , $\text{V}_{\text{GS}} = 0\text{V}$
$\text{R}_{\text{DS(on)}}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.18	—	0.24	$\Omega$	$\text{V}_{\text{GS}} = 12\text{V}$ , $\text{I}_{\text{D2}} = 5.0\text{A}$
$\text{R}_{\text{DS(on)}}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.18	—	0.24	$\Omega$	$\text{V}_{\text{GS}} = 12\text{V}$ , $\text{I}_{\text{D2}} = 5.0\text{A}$
$\text{V}_{\text{SD}}$	Diode Forward Voltage ④	—	1.5	—	1.5	V	$\text{V}_{\text{GS}} = 0\text{V}$ , $\text{I}_S = 8.0\text{A}$

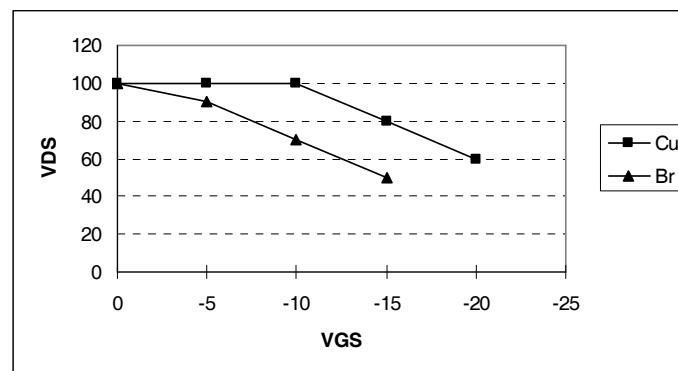
1. Part numbers IRHF7130 (JANSR2N7261)

2. Part numbers IRHF3130 (JANSF2N7261) and IRHF5130(JANSG2N7261), IRHF8130 (JANSH2N7261)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Typical Single Event Effect Safe Operating Area**

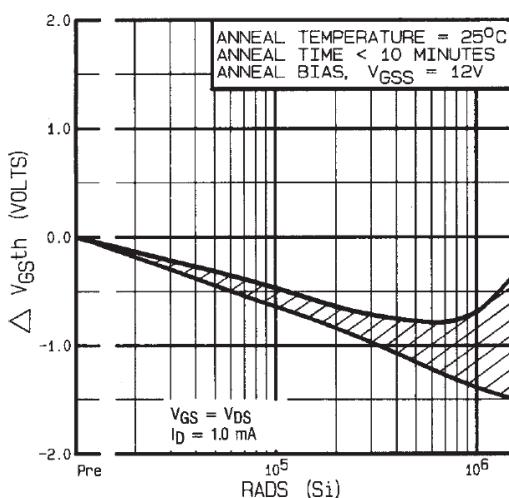
Ion	LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range ( $\mu\text{m}$ )	V <sub>DS</sub> (V)				
				@ V <sub>GS</sub> = 0V	@ V <sub>GS</sub> = -5V	@ V <sub>GS</sub> = -10V	@ V <sub>GS</sub> = -15V	@ V <sub>GS</sub> = -20V
Cu	28	285	43	100	100	100	80	60
Br	36.8	305	39	100	90	70	50	—



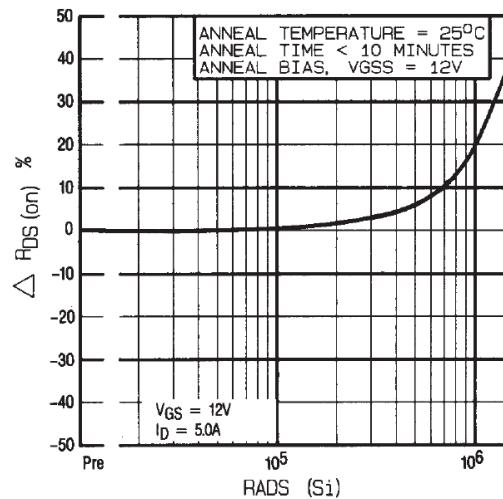
**Fig a.** Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

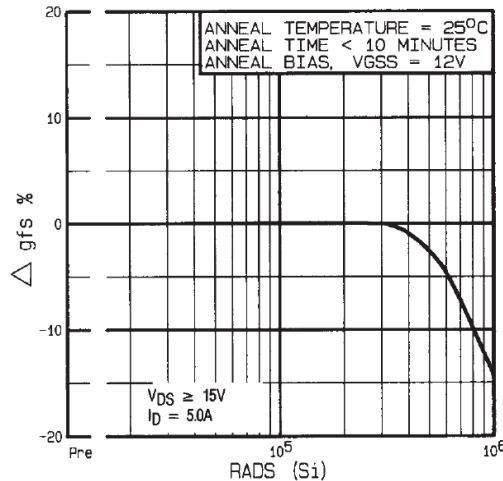
**Pre-Irradiation**



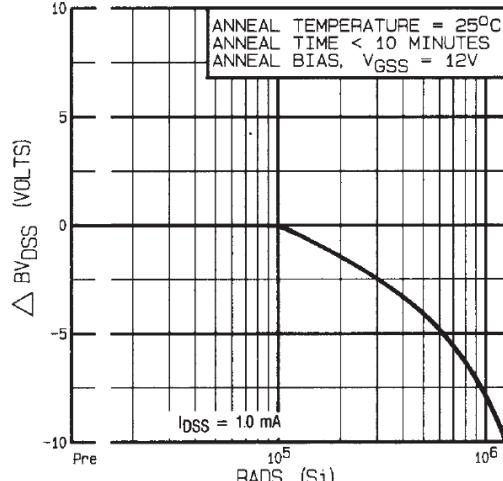
**Fig 1.** Typical Response of Gate Threshold Voltage Vs. Total Dose Exposure



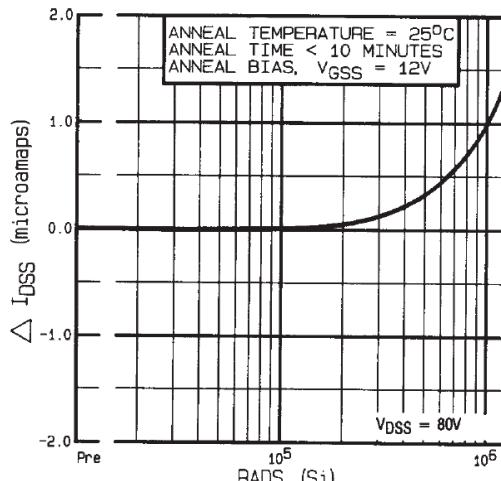
**Fig 2.** Typical Response of On-State Resistance Vs. Total Dose Exposure



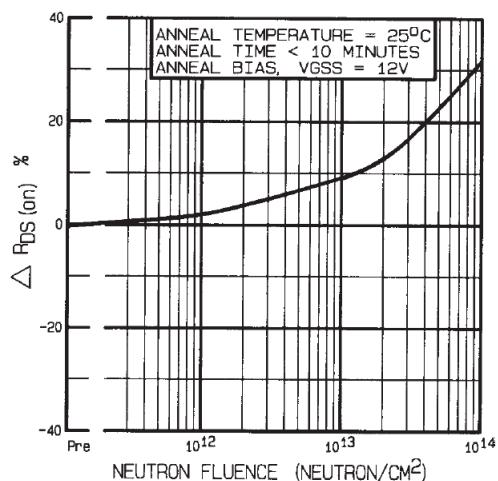
**Fig 3.** Typical Response of Transconductance Vs. Total Dose Exposure



**Fig 4.** Typical Response of Drain to Source Breakdown Vs. Total Dose Exposure

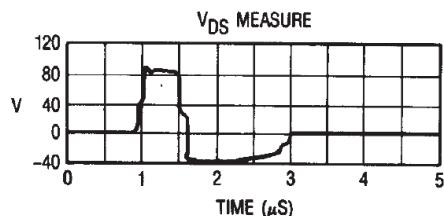


**Fig 5.** Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

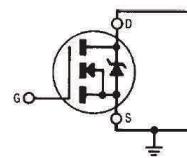


**Fig 6.** Typical On-State Resistance Vs. Neutron Fluence Level

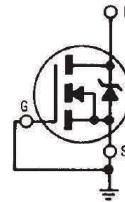
**Pre-Irradiation**



**Fig 7.** Typical Transient Response of Rad Hard HEXFET During  $1 \times 10^{12}$  Rad (Si)/Sec Exposure

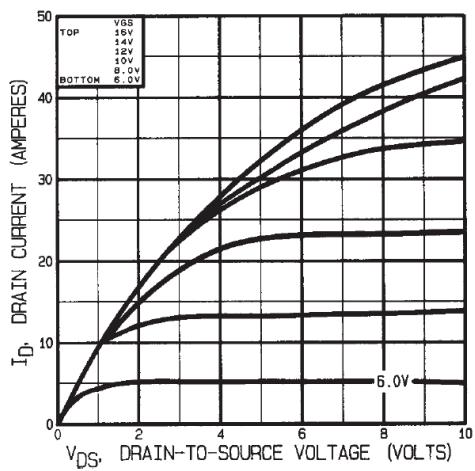


**Fig 8a.** Gate Stress of  $V_{GSS}$  Equals 12 Volts During Radiation

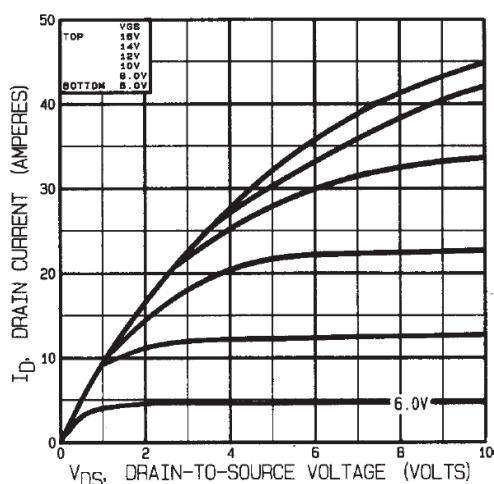


**Fig 8b.**  $V_{DSS}$  Stress Equals 80% of  $B_{V_{DSS}}$  During Radiation

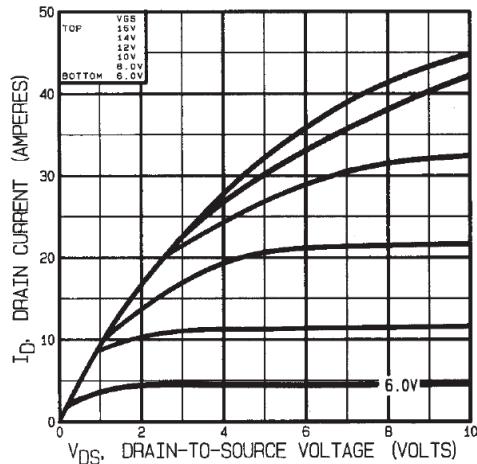
Note: Bias Conditions during radiation:  $V_{GS} = 12$  Vdc,  $V_{DS} = 0$  Vdc, Fig-9,10,11,12



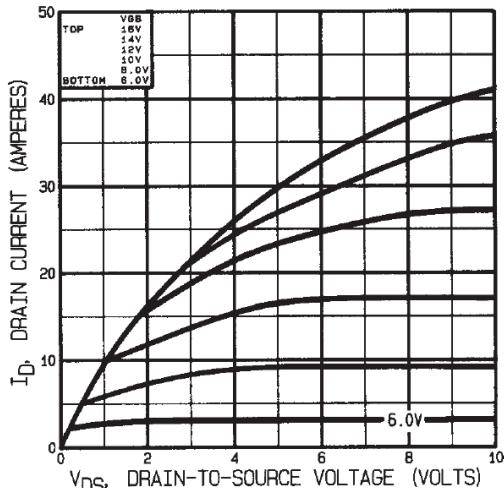
**Fig 9.** Typical Output Characteristics Pre-Irradiation



**Fig 10.** Typical Output Characteristics Post-Irradiation 100K Rads (Si)



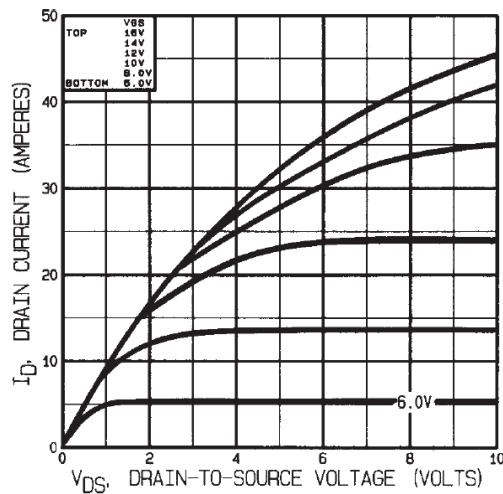
**Fig 11.** Typical Output Characteristics Post-Irradiation 300K Rads (Si)



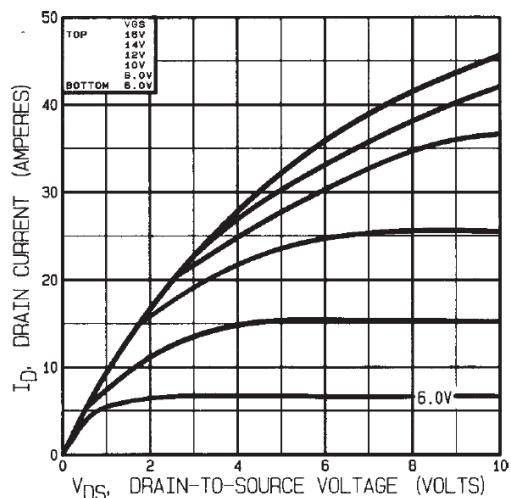
**Fig 12.** Typical Output Characteristics Post-Irradiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation:  $V_{GS} = 0$  Vdc,  $V_{DS} = 80$  Vdc Fig 13,14, 15,16

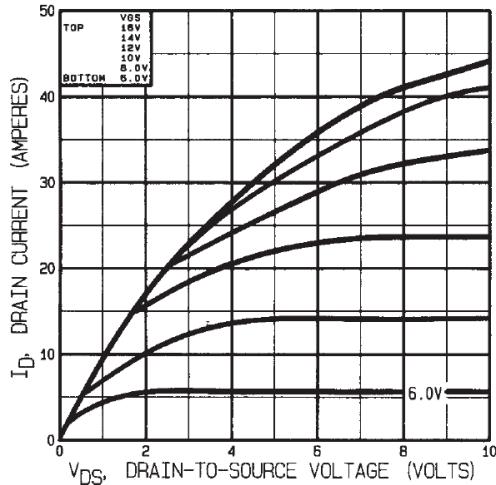
**Pre-Irradiation**



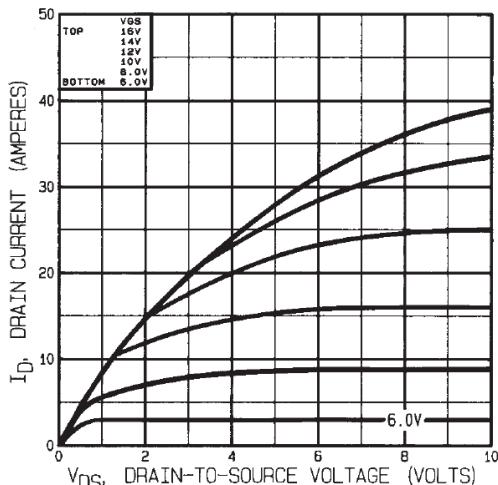
**Fig 13.** Typical Output Characteristics  
Pre-Irradiation



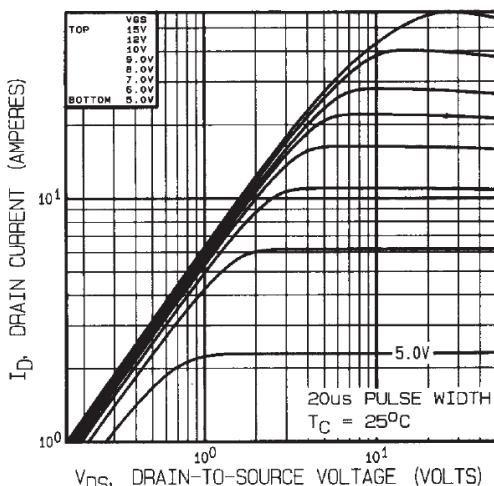
**Fig 14.** Typical Output Characteristics  
Post-Irradiation 100K Rads (Si)



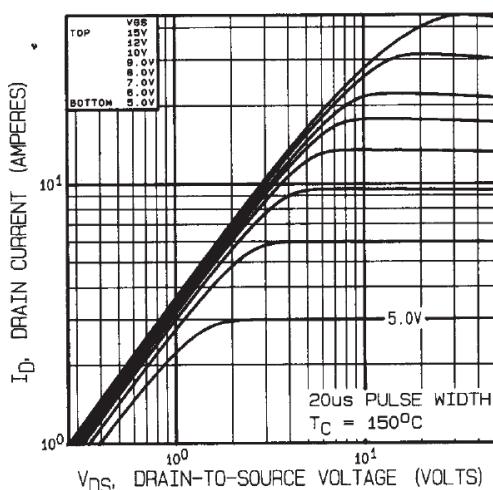
**Fig 15.** Typical Output Characteristics  
Post-Irradiation 300K Rads (Si)



**Fig 16.** Typical Output Characteristics  
Post-Irradiation 1 Mega Rads (Si)

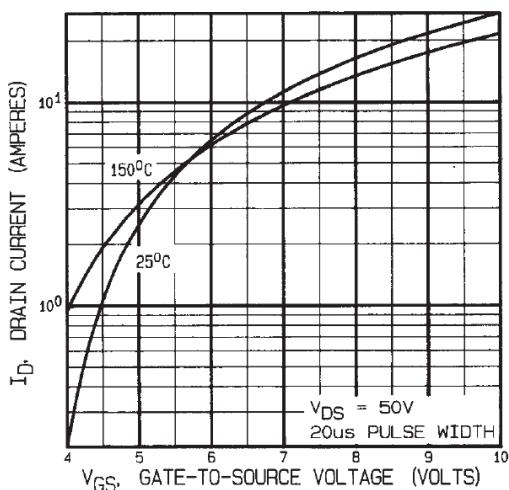


**Fig 17.** Typical Output Characteristics

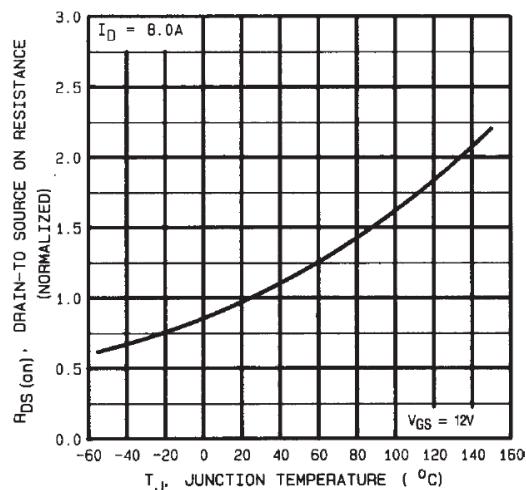


**Fig 18.** Typical Output Characteristics

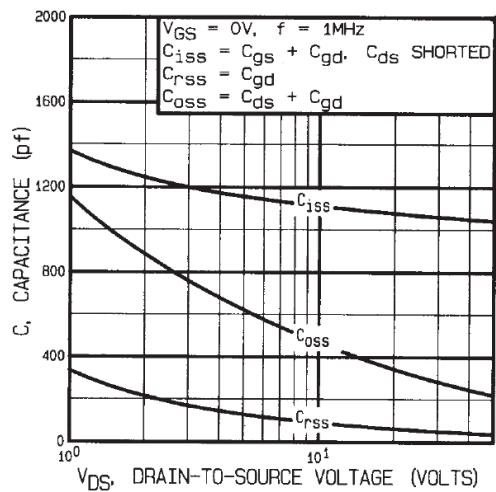
**Pre-Irradiation**



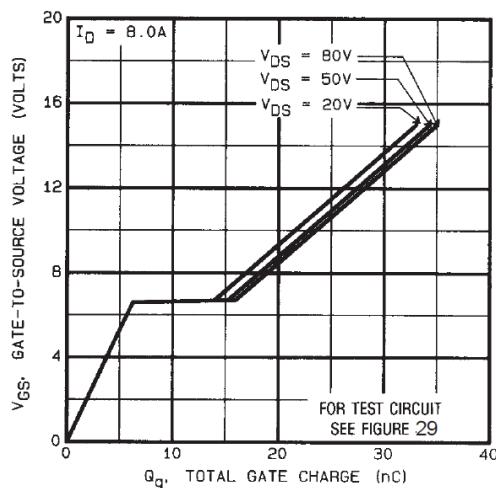
**Fig 19.** Typical Transfer Characteristics



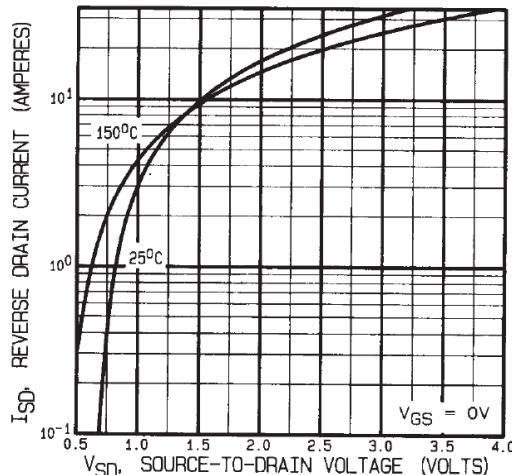
**Fig 20.** Normalized On-Resistance Vs. Temperature



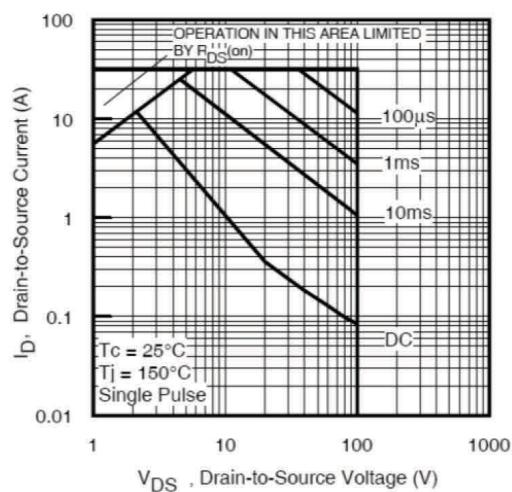
**Fig 21.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 22.** Typical Gate Charge Vs. Gate-to-Source Voltage

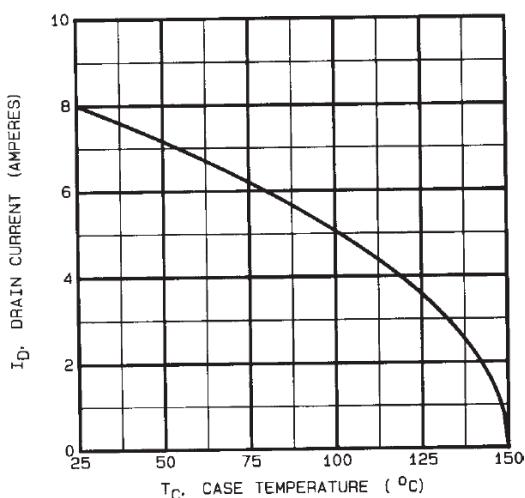


**Fig 23.** Typical Source-Drain Diode Forward Voltage

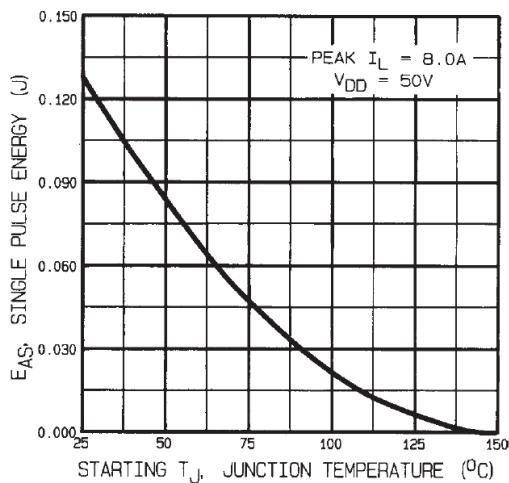


**Fig 24.** Maximum Safe Operating Area

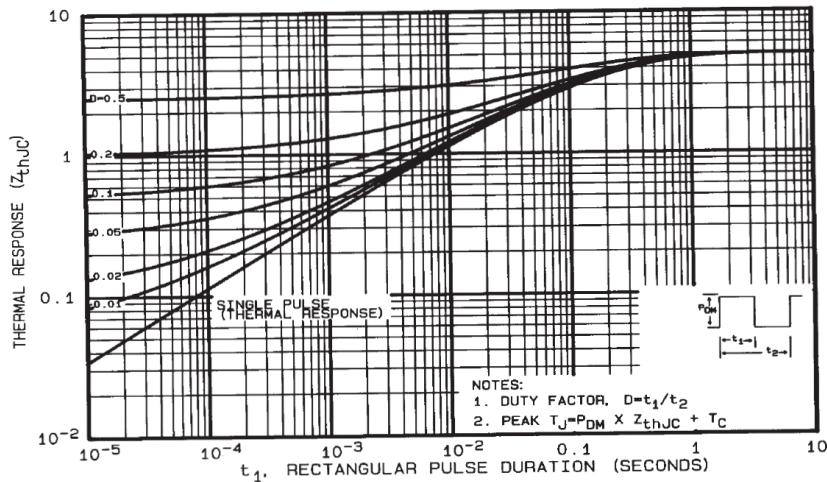
**Pre-Irradiation**



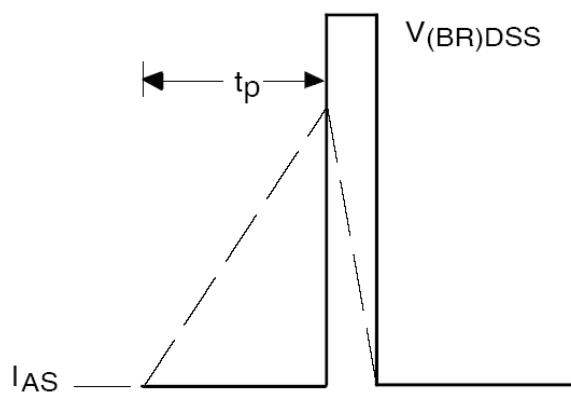
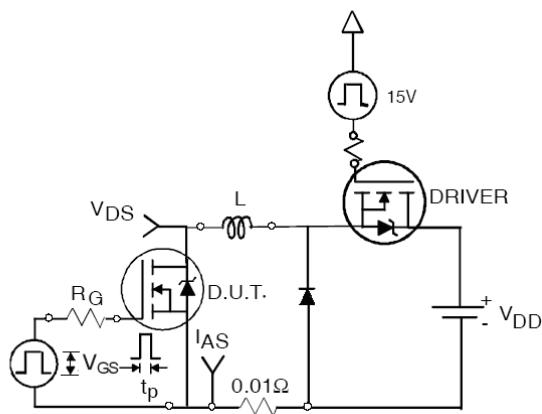
**Fig 25.** Maximum Drain Current Vs.  
Case Temperature



**Fig 26.** Maximum Avalanche Energy  
Vs. Drain Current

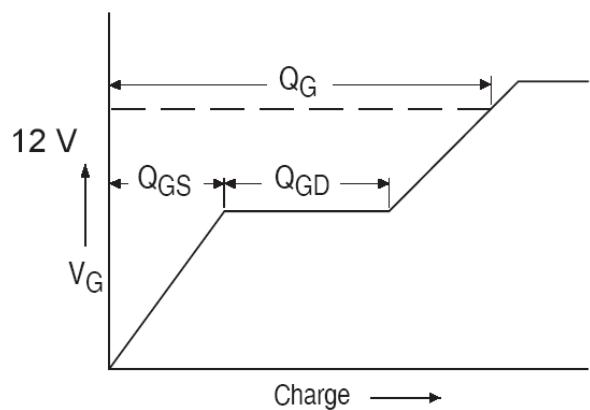


**Fig 27.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

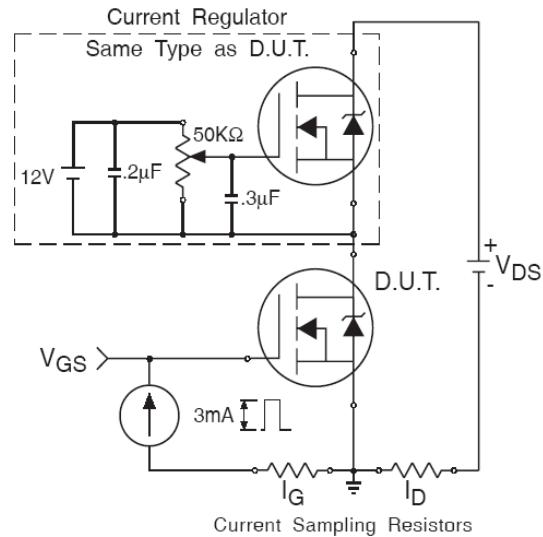


**Fig 28a.** Unclamped Inductive Test Circuit

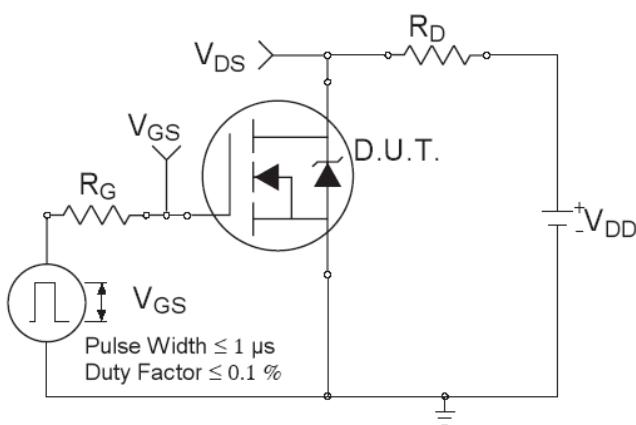
**Fig 28b.** Unclamped Inductive Waveforms



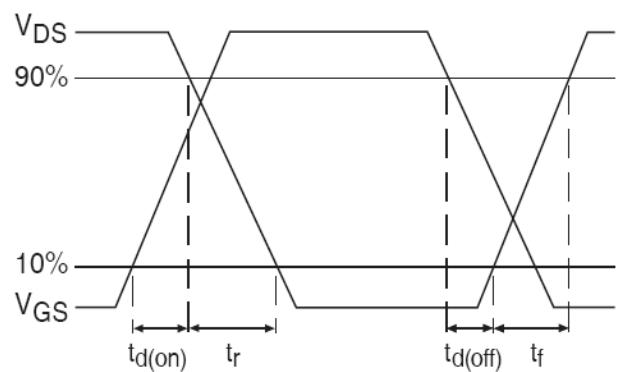
**Fig 29a.** Gate Charge Waveform



**Fig 29b.** Gate Charge Test Circuit

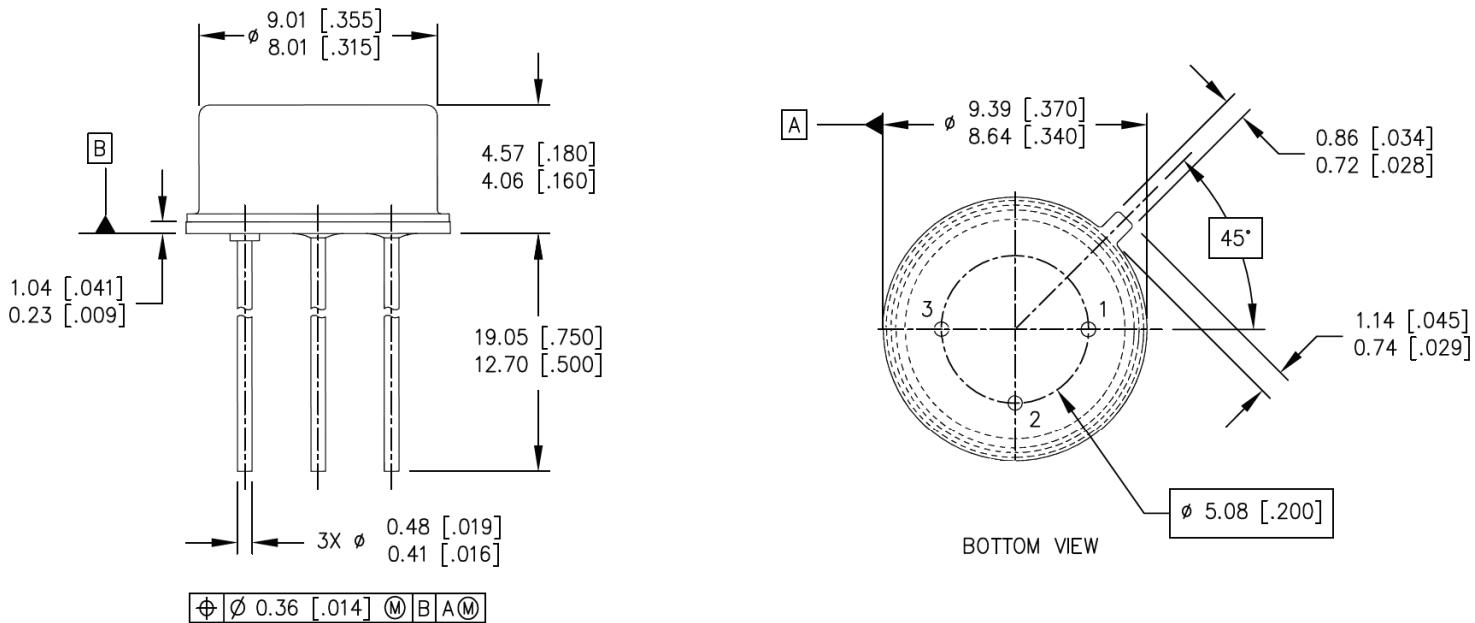


**Fig 30a.** Switching Time Test Circuit



**Fig 30b.** Switching Time Waveforms

### Case Outline and Dimensions - TO-205AF (TO-39)



### **IMPORTANT NOTICE**

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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