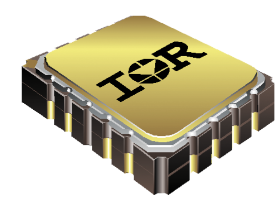
# IRHE57133SE
# JANSR2N7500U5

## RADIATION HARDENED POWER MOSFET SURFACE MOUNT (LCC-18)

**130V, N CHANNEL**
**REF: MIL-PRF-19500/707**
**R5 TECHNOLOGY**

### Product Summary

| Part Number | Radiation Level | RDS(on) | $I_D$ | QPL Part Number |
|---|---|---|---|---|
| IRHE57133SE | 100 kRads(Si) | 0.13Ω | 9.0A | JANSR2N7500U5 |



LCC-18

### Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm2)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retail all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

### Features

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

### Absolute Maximum Ratings — Pre-Irradiation

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $I_{D1}$ @ $V_{GS}$ = 12V, $T_C$ = 25°C | Continuous Drain Current | 9.0 | |
| $I_{D2}$ @ $V_{GS}$ = 12V, $T_C$ = 100°C | Continuous Drain Current | 6.0 | A |
| $I_{DM}$ @$T_C$ = 25°C | Pulsed Drain Current ① | 36 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 25 | W |
| | Linear Derating Factor | 0.2 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 56 | mJ |
| $I_{AR}$ | Avalanche Current ① | 9.0 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 2.5 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 6.6 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 150 | °C |
| | Package Mounting Surface Temperature | 300 (for 5s) | |
| | Weight | 0.42 (Typical) | g |

For Footnotes, refer to the page 2

Pre-Irradiation

## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 130 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.16 | —— | V/°C | Reference to 25°C, $I_D$ = 1.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | —— | 0.13 | Ω | $V_{GS}$ = 12V, $I_{D2}$ = 6.0A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.5 | —— | 4.5 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.0mA |
| Gfs | Forward Transconductance | 5.0 | —— | —— | S | $V_{DS}$ = 15V, $I_{D2}$ = 6.0A ④ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | —— | —— | 10 | µA | $V_{DS}$ = 104V, $V_{GS}$ = 0V |
| | | —— | —— | 25 | | $V_{DS}$ = 104V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | —— | —— | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Leakage Reverse | —— | —— | -100 | | $V_{GS}$ = -20V |
| $Q_G$ | Total Gate Charge | —— | —— | 48 | nC | $I_{D1}$ = 9.0A |
| $Q_{GS}$ | Gate-to-Source Charge | —— | —— | 16 | | $V_{DS}$ = 65V |
| $Q_{GD}$ | Gate-to-Drain ('Miller') Charge | —— | —— | 18 | | $V_{GS}$ = 12V |
| $t_{d(on)}$ | Turn-On Delay Time | —— | —— | 25 | ns | $V_{DD}$ = 65V |
| tr | Rise Time | —— | —— | 100 | | $I_{D1}$ = 9.0A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | —— | 35 | | $R_G$ = 7.5Ω |
| $t_f$ | Fall Time | —— | —— | 40 | | $V_{GS}$ = 12V |
| Ls +$L_D$ | Total Inductance | —— | 6.1 | —— | nH | Measured from the center of drain pad to center of source pad |
| $C_{iss}$ | Input Capacitance | —— | 1020 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 306 | —— | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 22 | —— | | $f$ = 1.0MHz |

## Source-Drain Diode Ratings and Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 9.0 | A | |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | —— | —— | 36 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.5 | V | $T_J$ = 25°C, $I_S$ = 9.0A, $V_{GS}$ = 0V④ |
| $t_{rr}$ | Reverse Recovery Time | —— | —— | 250 | ns | $T_J$ = 25°C, $I_F$ = 9.0A, $V_{DD}$ ≤ 25V |
| $Q_{rr}$ | Reverse Recovery Charge | —— | —— | 1.5 | µC | di/dt = 100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

## Thermal Resistance

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | —— | —— | 5.0 | °C/W |
| $R_{\theta J\text{-}PCB}$ | Junction-to-PC Board | —— | 19 | —— | |

**Footnotes:**

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② $V_{DD}$ = 50V, starting $T_J$ = 25°C, L = 1.4mH, Peak $I_L$ = 9.0A, $V_{GS}$ = 12V

③ $I_{SD}$ ≤ 9.0A, di/dt ≤ 270A/µs, $V_{DD}$ ≤ 130V, $T_J$ ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ Total Dose Irradiation with $V_{GS}$ Bias. 12 volt $V_{GS}$ applied and $V_{DS}$ = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ Total Dose Irradiation with $V_{DS}$ Bias. 104 volt $V_{DS}$ applied and $V_{GS}$ = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

## Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

### Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

| Symbol | Parameter | 100 kRads (Si)[1] | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 130 | —— | V | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | 4.5 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.0mA |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | —— | 100 | nA | $V_{GS}$ = 20V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | —— | -100 | nA | $V_{GS}$ = -20V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | —— | 10 | µA | $V_{DS}$ = 104V, $V_{GS}$ = 0V |
| $R_{DS(on)}$ | Static Drain-to-Source ④ On-State Resistance (TO-3) | —— | 0.111 | Ω | $V_{GS}$ = 12V, $I_{D2}$ = 6.0A |
| $R_{DS(on)}$ | Static Drain-to-Source ④ On-State Resistance (LCC-18) | —— | 0.13 | Ω | $V_{GS}$ = 12V, $I_{D2}$ = 6.0A |
| $V_{SD}$ | Diode Forward Voltage ④ | —— | 1.5 | V | $V_{GS}$ = 0V, $I_S$ = 9.0A |

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

### Table 2. Typical Single Event Effect Safe Operating Area

| LET (MeV/(mg/cm²)) | Energy (MeV) | Range (µm) | VDS (V) | | | | |
|---|---|---|---|---|---|---|---|
| | | | @ VGS = 0V | @ VGS = -5V | @ VGS = -10V | @ VGS = -15V | @ VGS = -20V |
| 38 ± 5% | 300 ± 7.5% | 38 ± 7.5% | 130 | 130 | 130 | 130 | 130 |
| 61 ± 5% | 330 ±7. 5% | 31 ± 10% | 130 | 130 | 130 | 100 | 50 |
| 84 ± 5% | 350 ± 10% | 28 ± 7.5% | 130 | 120 | 30 | —— | —— |

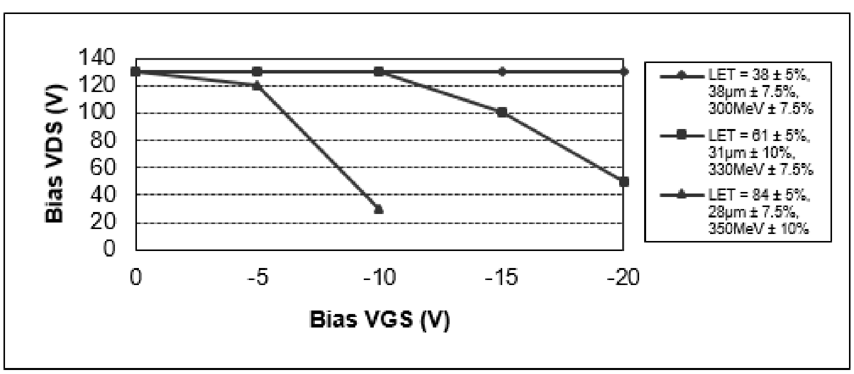



**Fig a.** Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2

**Pre-Irradiation**

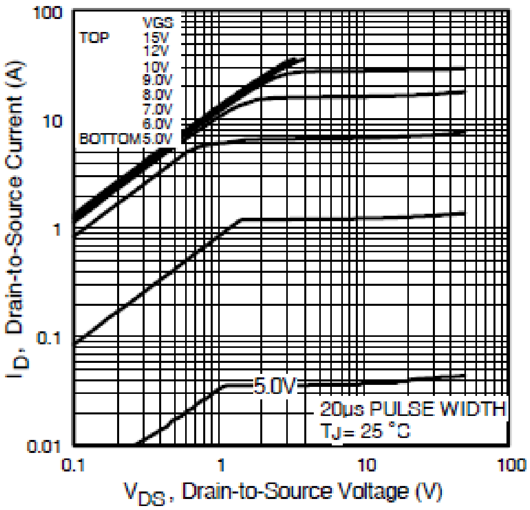



**Fig 1.** Typical Output Characteristics

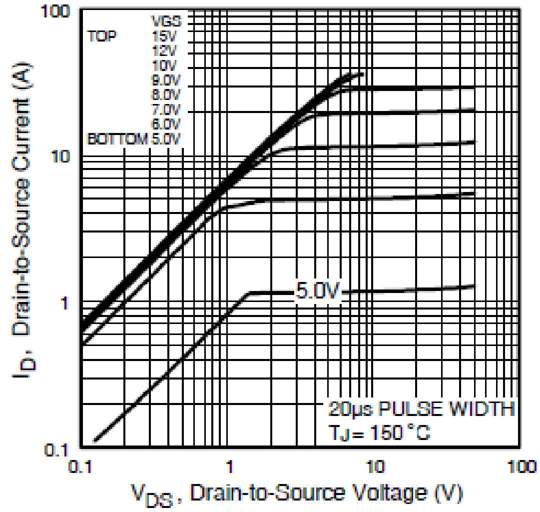



**Fig 2.** Typical Output Characteristics

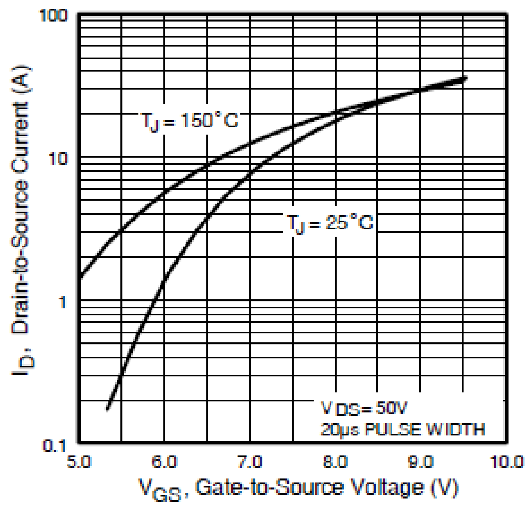



**Fig 3.** Typical Transfer Characteristics

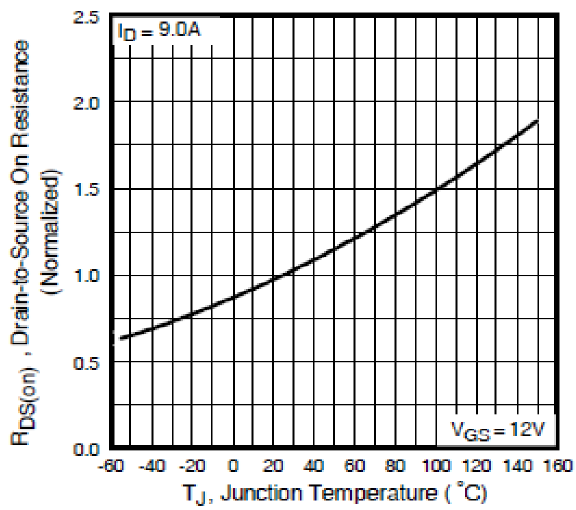



**Fig 4.** Normalized On-Resistance Vs. Temperature

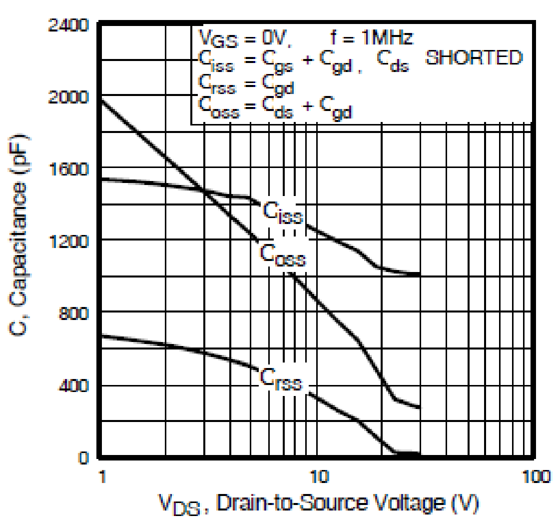



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

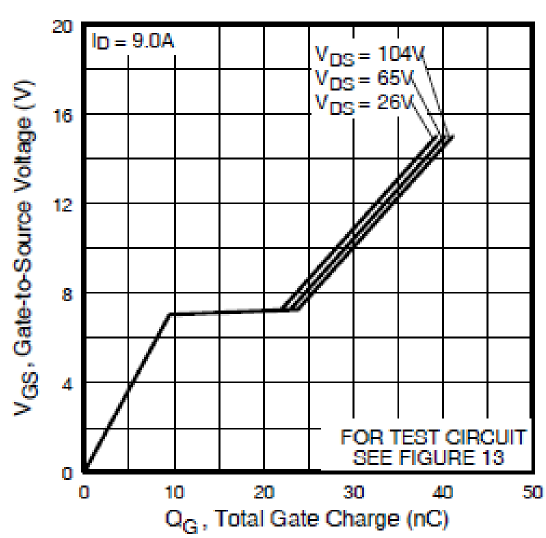



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

**Pre-Irradiation**

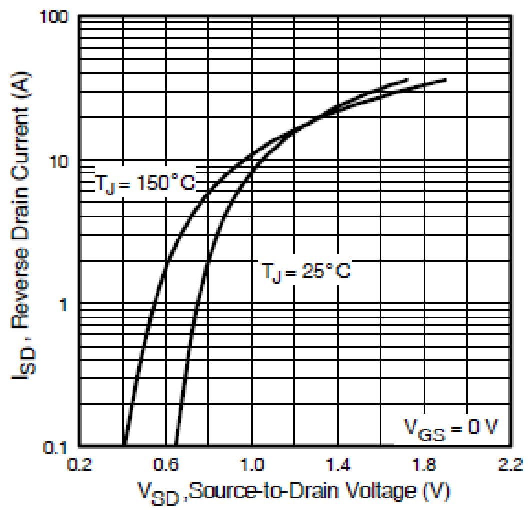



**Fig 7.** Typical Source-Drain Diode Forward Voltage

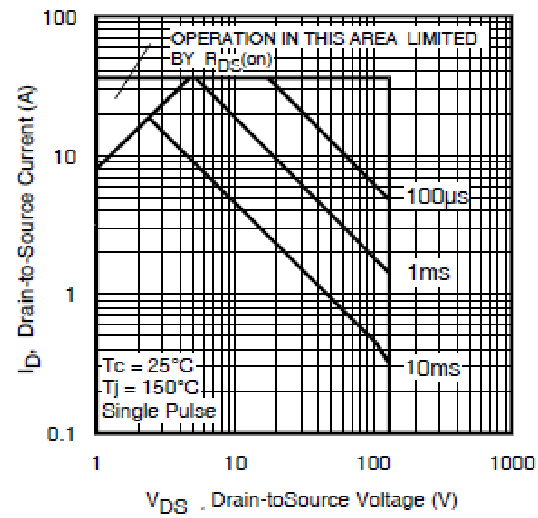



**Fig 8.** Maximum Safe Operating Area

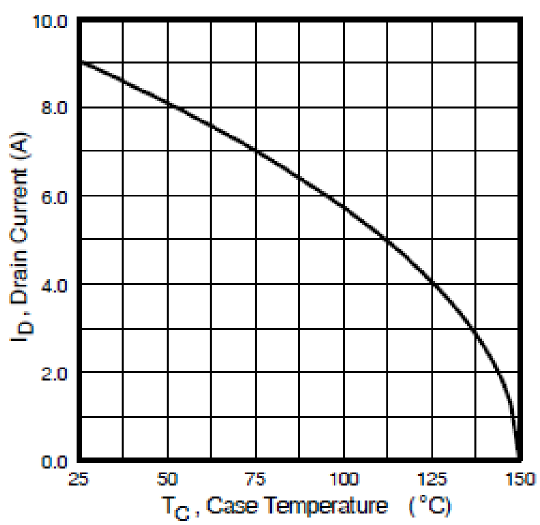



**Fig 9.** Maximum Drain Current Vs. Case Temperature

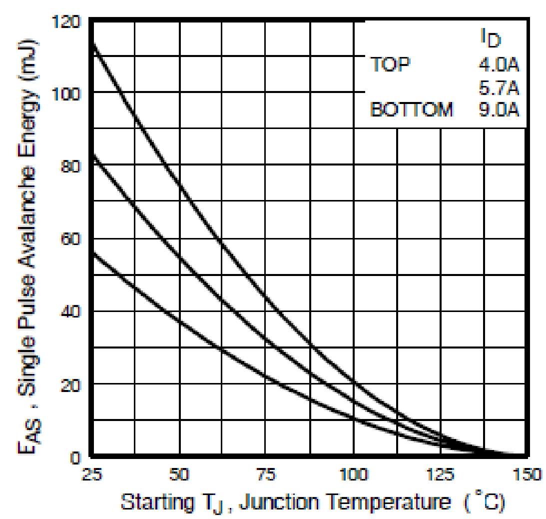



**Fig 10.** Maximum Avalanche Energy Vs. Drain Current

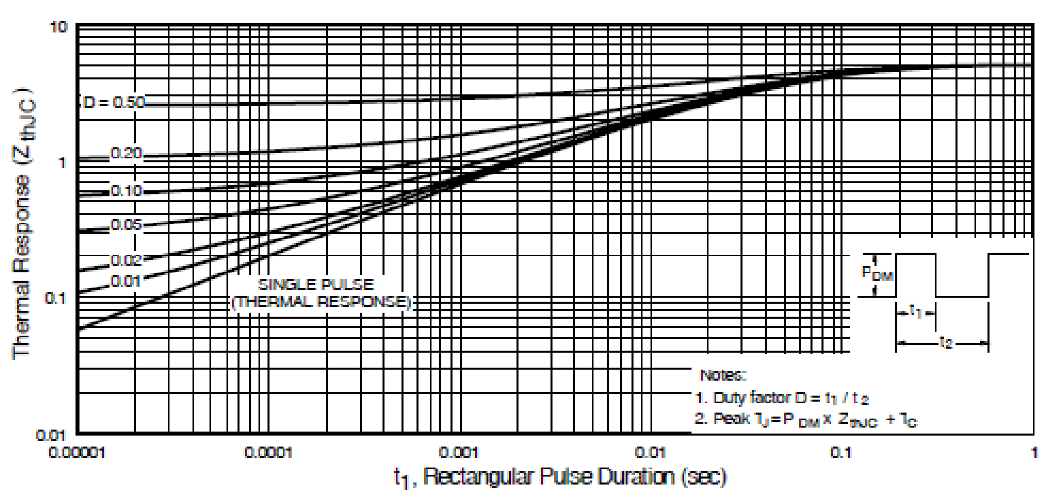



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

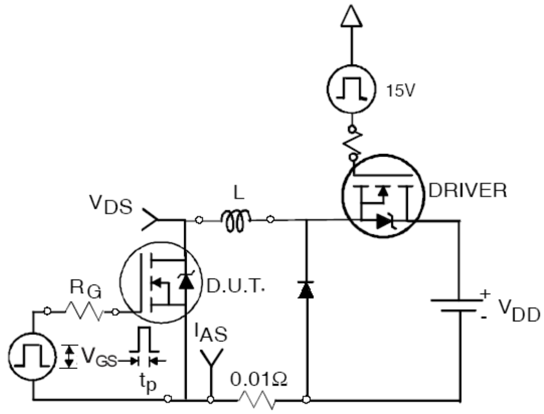



**Fig 12a.** Unclamped Inductive Test Circuit

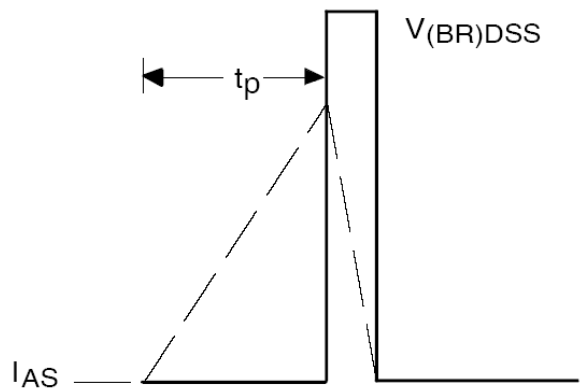



**Fig 12b.** Unclamped Inductive Waveforms

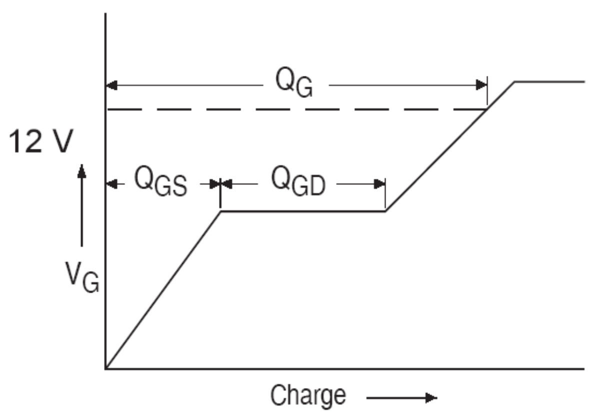



**Fig 13a.** Gate Charge Waveform

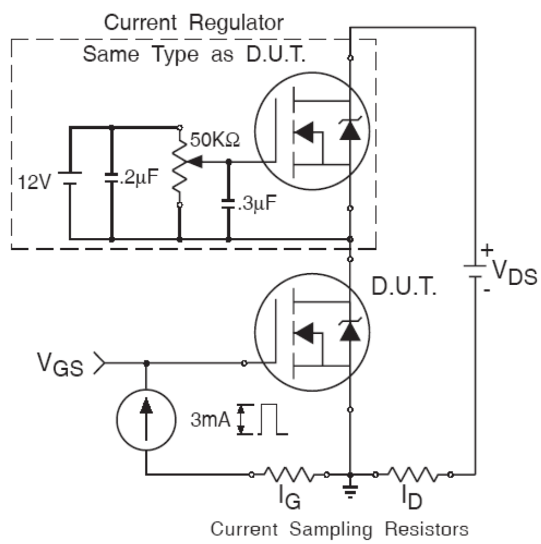



**Fig 13b.** Gate Charge Test Circuit

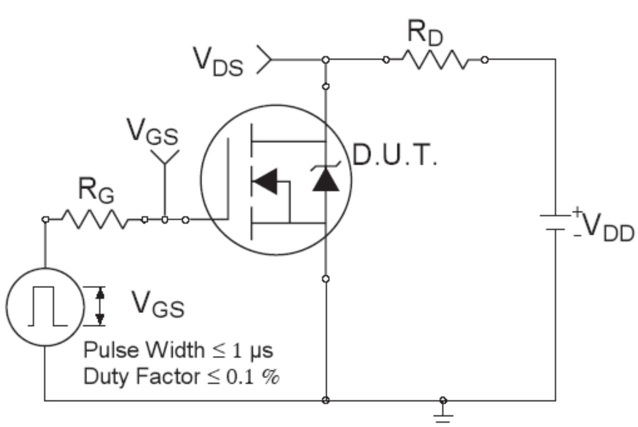



**Fig 14a.** Switching Time Test Circuit

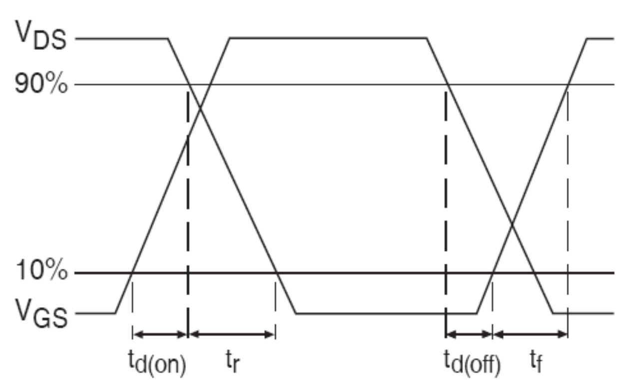
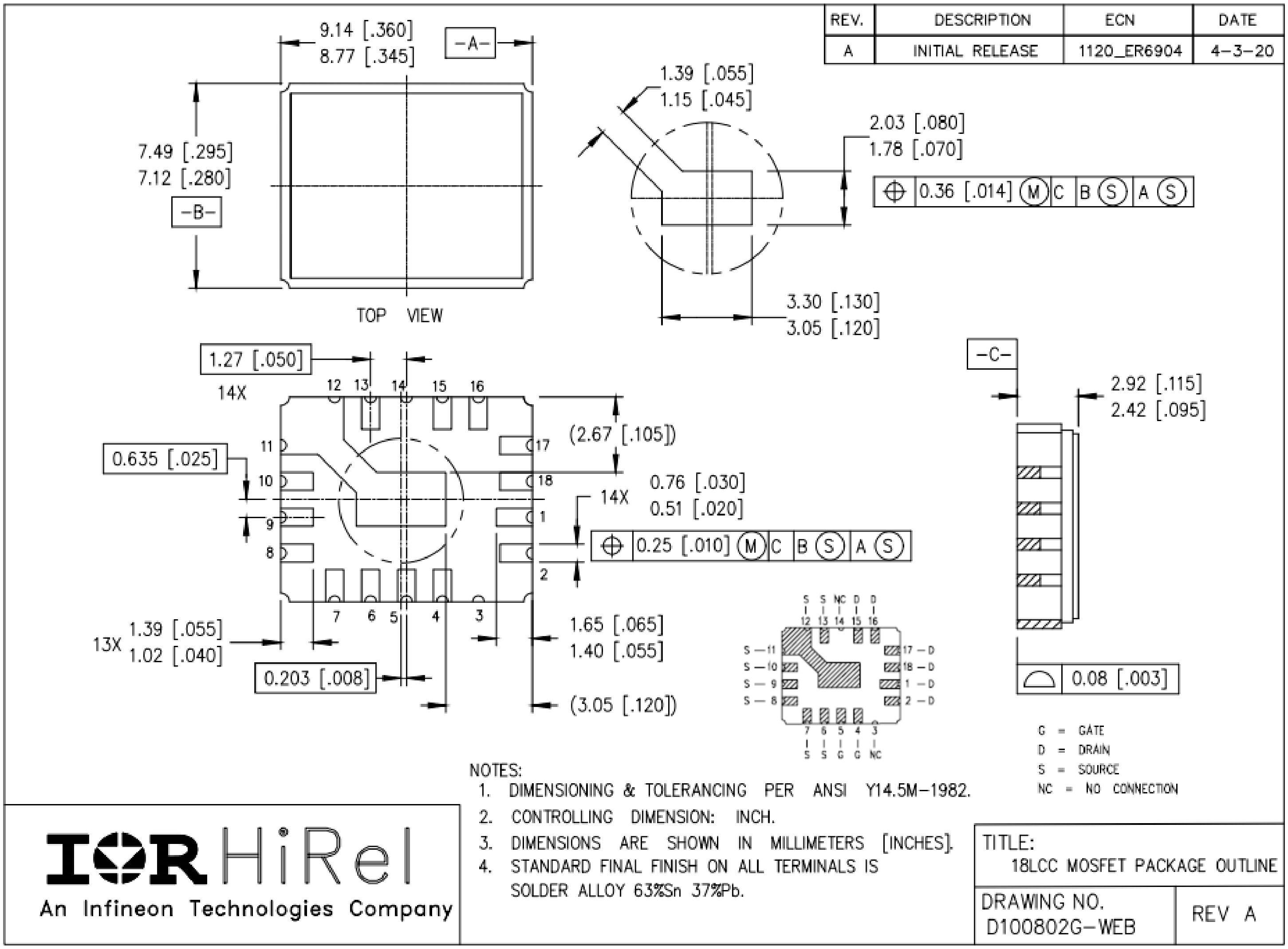



**Fig 14b.** Switching Time Waveforms

**Note: For the most updated package outline, please see the website: [LCC-18]**

## Case Outline and Dimensions — LCC-18

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