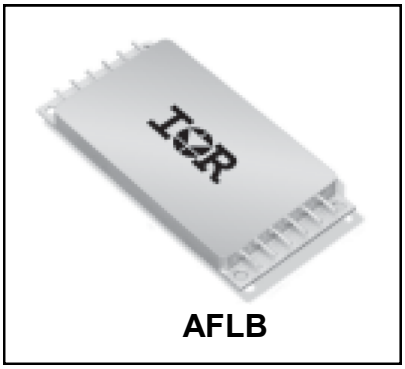
AFLB2805S

(120W, 28Vin, 5Vout)

HYBRID HIGH-RELIABILITY DC-DC CONVERTER



AFLB

Description

The AFLB family is the new generation series of high power DC/DC converters with improved efficiency and higher output current capabilities in addition to the features provided by the well proven AFL family.

This series incorporates an active clamp forward topology with synchronous rectification and IR-Hirel proprietary magnetic pulse feedback technology providing optimum dynamic line and load regulation response.

High power density with no derating over the full military temperature range. For applications requiring output power higher than 120W, multiple converters can be operated in parallel. The internal current sharing circuits assure equal current distribution among the paralleled converters. Multiple converters can be synchronized to a system clock in the 525kHz range or to the synchronization output of one converter. Under-voltage lockout, primary and secondary referenced inhibit, soft-start and load fault protection are provided on all models.

These converters are hermetically packaged in two enclosure variations, utilizing Copper-Zirconium core pins to minimize resistive DC losses. Three lead styles are available, each fabricated with International Rectifier's rugged ceramic lead-to-package seal assuring long term hermeticity in the most harsh environments.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are fabricated utilizing DSCC qualified processes. For available screening options refer to device screening table in the data sheet. Variations in electrical, mechanical and screening can be accommodated. Contact IR-Hirel San Jose for special requirements.

Features

- 16V To 40V Input Range
- High Power Density - up to 84 W/in3
- Up To 120W Output Power
- Parallel Operation with Power Sharing
- High Efficiency - to 91%
- Full Military Temperature Range
- Continuous Short Circuit and Overload Protection
- Primary and Secondary Referenced Inhibit Functions
- Line Rejection > 40dB - DC to 50 kHz
- External Synchronization Port
- Fault Tolerant Design
- Low Profile (0.380") Seam Welded Package
- Ceramic Feed thru CuZr Core Pins

Specifications

Absolute Maximum Ratings	
Input voltage	-0.5V_{DC} to +50V_{DC}
Operating case temperature	-55°C to +125°C
Lead temperature	300°C for 10 seconds
Storage case temperature	-65°C to +135°C

Static Characteristics -55°C ≤ T_{CASE} ≤ +125°C, V_{IN} = 28V_{DC} ±5%, C_L = 0 unless otherwise specified

Parameter	Group A Subgroups	Test Conditions	Min	Nom	Max	Unit
Input voltage		Note 6	16	28	40	V
Output voltage	1, 2, 3	100% Load Note 6	4.95	5.0	5.05	V
Output current	1, 2, 3	V_{IN} = 16, 28, 40 Volts Note 6			24	A
Under-Voltage Release Lock-out Hysteresis	1, 2, 3	50% Load	 14.9 13.9 0.60	 15.3 14.3 1.0	 15.9 14.9 1.4	V
Output power		V_{IN} = 16, 28, 40 Volts Note 6			120	W
Maximum capacitive load		Note 1, 14			10	mF
Output voltage temperature coefficient		100% Load Note 1, 6	-0.015	0.007	+0.015	%/°C
Output voltage regulation Line Load	1, 2, 3	 V_{IN} = 16, 28, 40 Volts No Load, 50% Load, 100% Load	 -0.4 -1.0	 0.08 -0.5	 +0.4 +1.0	%
Output ripple voltage	1, 2, 3	V_{IN} = 16, 28, 40 Volts 100% Load, Note 13		10	30	mVpp
Input current No Load Inhibit 1 Inhibit 2	1, 2, 3	 Pin 4 Shorted to Pin 2 Pin 12 Shorted to Pin 8		 80 4.3 14	 130 5.5 20	mA
Input ripple current	1, 2, 3	100% Load Notes 13, 15		20	60	mApp
Current limit point	1, 2, 3	As a percentage of full rated load V_{OUT} = 90% V_{NOM} Note 5	110	120	125	%
Load fault power dissipation Overload or short circuit	1, 2, 3	Notes 5, 11		28	33	W
Efficiency	1 2 3	100% Load	88 86 88	89.5 87.3 90.8		%
Enable inputs (Inhibit function) Converter off Sink current Converter on Sink current	1, 2, 3	 Logical Low on Pin 4 or Pin 12 Note 1 Logical High on Pin 4 or Pin 12 Notes 1, 9	 -0.5 - 2.0 -	 - 46 - 46	 0.8 100 50 100	 V µA V µA

For Notes to Static Characteristics, refer to page 3

Static Characteristics (Continued) -55°C < T_{CASE} ≤ +125°C, V_{IN} = 28V_{DC} ±5%, C_L = 0 unless otherwise specified.

Parameter	Group A Subgroups	Test Conditions	Min	Nom	Max	Unit
Switching frequency	1, 2, 3	50% Load Sync Input (Pin 6) open	500	525	550	kHz
Synchronization input Frequency range Pulse amplitude, Hi Pulse amplitude, Lo Pulse amplitude, Hi - Lo Pulse fall time Pulse duty cycle	1, 2, 3	50% Load Note 1, 12	 450 2.0 -0.5 2.0 20		 650 10 0.8 5.5 100 80	 kHz V V V ns %
Isolation	1	Input to Output or Any Pin to Case (except Pin 3). Test @ 500V_{DC}	100			MΩ
Device weight		Slight Variations with Case Style		80	85	g
MTBF		MIL-HDBK-217F, SF @ T_C = 55°C MIL-HDBK-217F, AIF @ T_C = 70°C	320 100			kHrs

Dynamic Characteristics -55°C ≤ T_{CASE} ≤ +125°C, V_{IN} = 28V_{DC} ±5%, C_L = 0 unless otherwise specified.

Parameter	Group A Subgroups	Test Conditions	Min	Nom	Max	Unit
Line rejection	4, 5, 6	100% Load DC to 50kHz Note 1	40	50		dB
Load transient response Amplitude Recovery	4, 5, 6	Load steps 50% ⇔ 100% and 10% ⇔ 50% Notes 2, 8	 ±450	 ±120 80	 ±450 200	 mV µs
Line transient response Amplitude Recovery	4, 5, 6	Line steps 16V ⇔ 40V 50% Load Notes 1, 2, 3	 -500	 ±120	 500 200	 mV µs
Turn-on characteristics Overshoot Rise time Delay	4, 5, 6	Load = No load and 100% load. Enable 1, 2 on. (Pins 4, 12 high or open) Notes 2, 4	 1.5 4	 50 3 6	 250 5 9	 mV ms ms

Notes to Specifications

1. Parameters not 100% tested but are guaranteed to the limits specified in the table.
2. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±5% of its steady state value at 50% load
3. Step transition time ≥ 100µs.
4. Turn-on delay is measured with an input voltage rise time of between 100V and 500V per millisecond.
5. Load in constant current mode, calculated worst case with measured parameters just before the trip-point.
6. Parameter verified as part of another test.
7. All electrical tests are performed with the remote sense leads connected to the output leads at the load.
8. Load transient transition time ≥ 10µs.
9. Enable inputs internally pulled high. Nominal open circuit voltage ≈ 5.2V_{DC}.
10. Subgroups 1, 2 and 3 are static tests. Subgroups 4, 5 and 6 are dynamic tests. Subgroups 1, 4: +25ºC, subgroups 2, 5: +125ºC, subgroups 3 and 6 are done at -55ºC.
11. Overload and Short Circuit conditions are defined as the load required to cause output voltage to drop to 90% and 5% respectively of nominal.
12. Operation at higher switching frequencies reduces efficiency slightly and might increase the minimum operational input voltage.
13. Guaranteed for a DC to 20MHz bandwidth. Tested with a 20kHz to 10MHz bandwidth.
14. Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit will cause erratic turn-on behavior.
15. Measurement is done with an inductance in series of 900nH ±10% that represents a typical line inductance.

Typical performance characteristics

Unless otherwise specified, Temperature = 25°C, Input voltage = 28V.

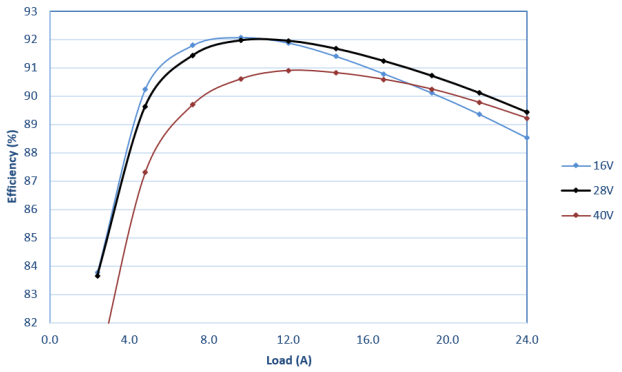


Figure 1: Efficiency vs Load.

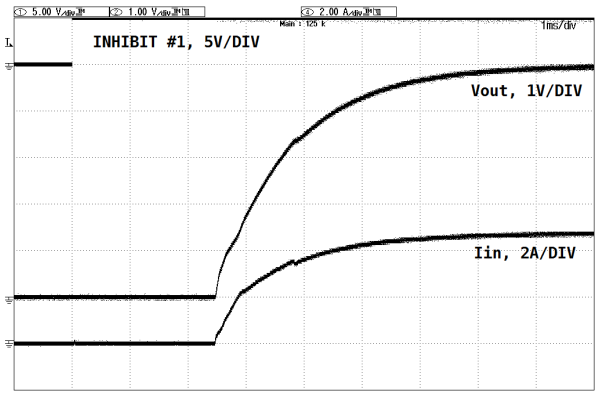


Figure 2: Turn on at full load, CCM, 1 ms/div.

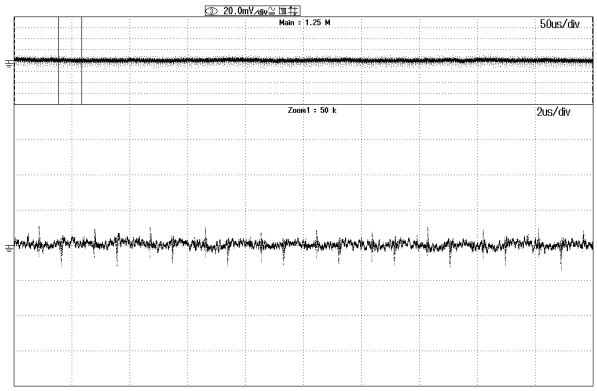


Figure 3: Output voltage ripple at full load, 20mV/div, 20 MHz BW, 50 us/div and 2 us/div.

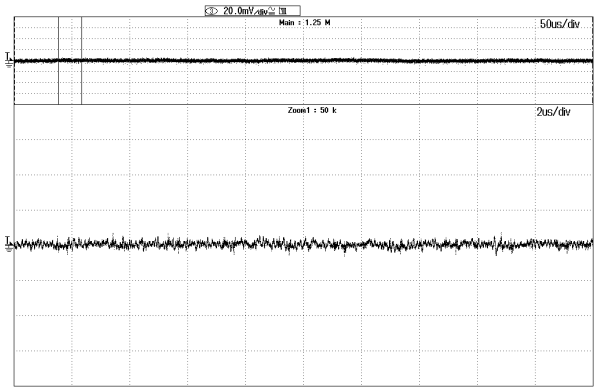


Figure 4: Output voltage ripple at no load, 20mV/div, 20 MHz BW, 50 us/div and 2 us/div.

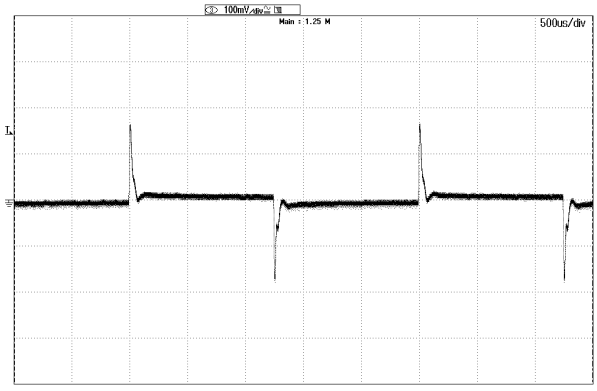


Figure 5: Step load 10%-50%, 100 mV/div and 500 us/div.

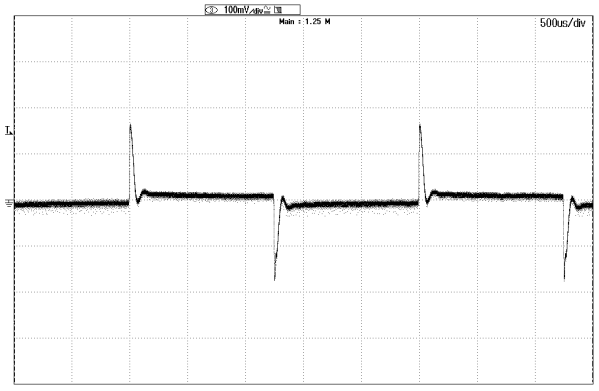
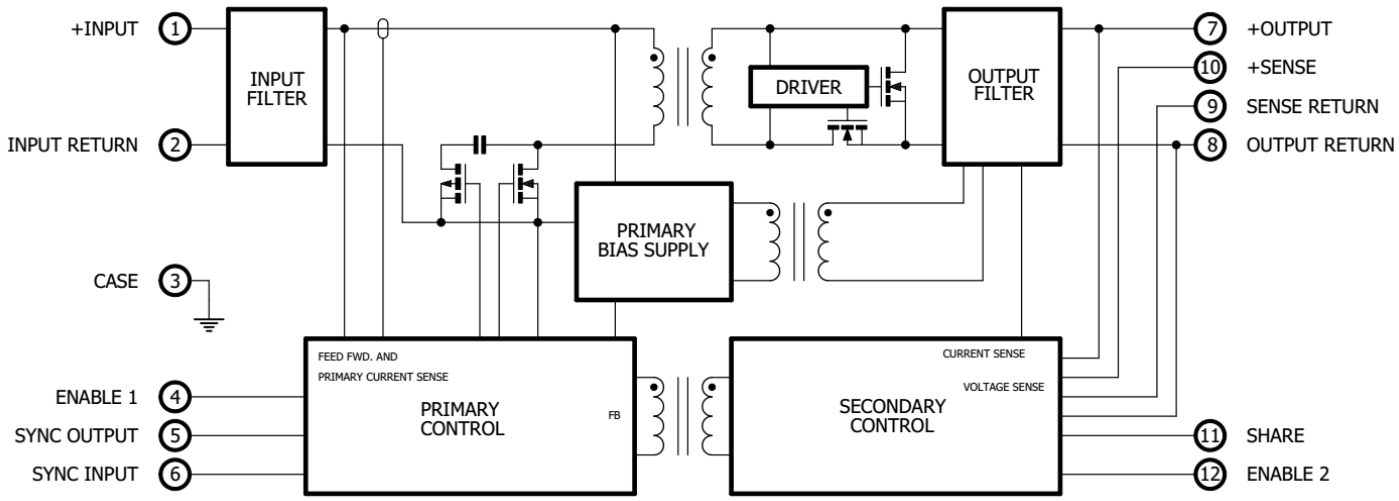


Figure 6: Step load 50%-100%, 100 mV/div and 500 us/div.

Functional block diagram (Single Output Models)

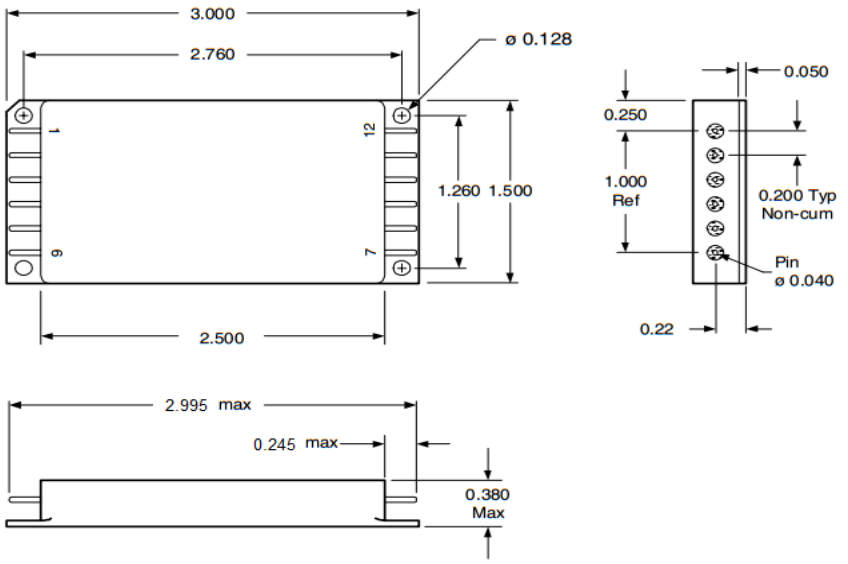


Pin Designation

Pin #	Designation
1	+ Input
2	Input Return
3	Case Ground
4	Enable 1
5	Sync. Output
6	Sync. Input
7	+ Output
8	Output Return
9	Return Sense
10	+ Sense
11	Share
12	Enable 2

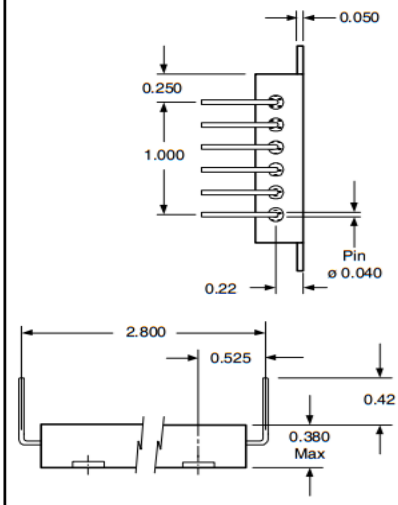
Mechanical Outline

Case X

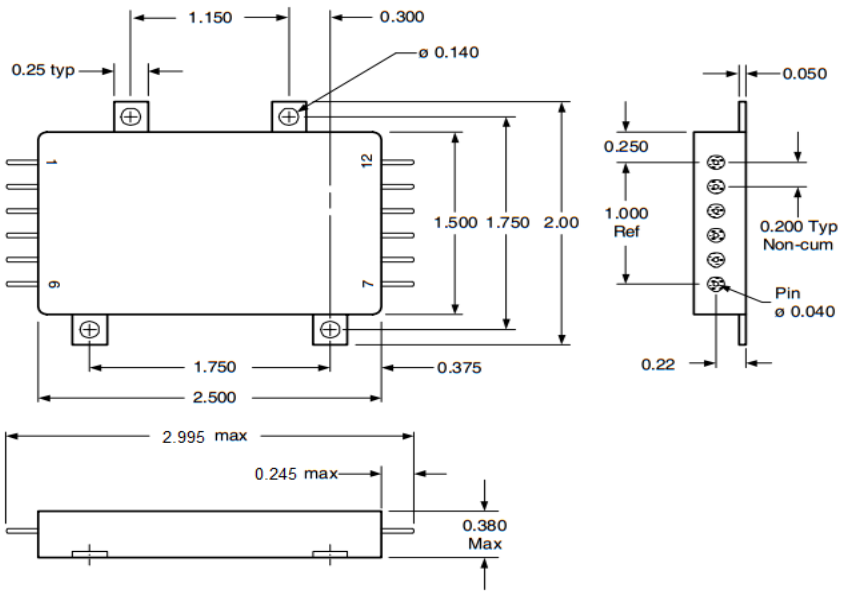


Case W

Pin Variation of Case Y

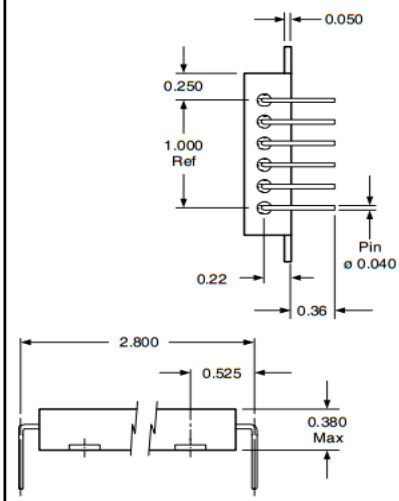


Case Y



Case Z

Pin Variation of Case Y



Tolerances, unless otherwise specified: .XX = ±0.010
.XXX = ±0.005

BERYLLIA WARNING: These converters are hermetically sealed; however they contain BeO substrates and should not be ground or subjected to any other operations including exposure to acids, which may produce Beryllium dust or fumes containing Beryllium.

Device Screening

Requirement	MIL-STD-883 Method	ES	CH
Temperature Range	—	-55°C to +125°C	-55°C to +125°C
Element Evaluation	MIL-PRF-38534	N/A	Class H
Non-Destructive Bond Pull	2023	N/A	N/A
Internal Visual	2017	Yes	Yes
Temperature Cycle	1010	Cond B	Cond C
Constant Acceleration	2001, Y1 Axis	500 Gs	3000 Gs
PIND	2020	N/A	N/A
Burn-In	1015	48hrs @ 125°C	160 hrs @ 125°C
Final Electrical (Group A)	MIL-PRF-38534 & Specification	25°C①	-55°C, +25°C, +125°C
PDA	MIL-PRF-38534	N/A	10%
Seal, Fine and Gross	1014	Cond A, C	Cond A,C
Radiographic	2012	N/A	N/A
External Visual	2009	Yes	Yes

Notes:
① Sample tests at low and high temperatures.

Part Numbering

AFLB 28 05 S W /CH

Model

Input Voltage
28 = 28V
50 = 50V
120 = 120V
270 = 270V

Output Voltage
05 = 5V
06R5 = 6.5V

Screening Level
(Please refer to Screening Table)
ES, CH

Case Style
W, X, Y, Z

Output
S = Single
D = Dual

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