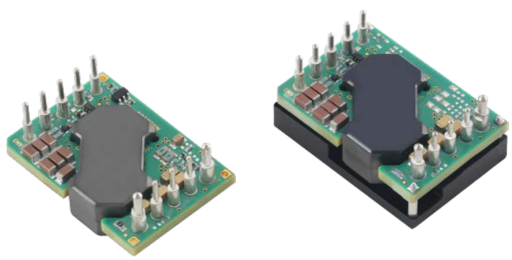
Leading the Advancement of Power Conversion

9-53V Input 12A Output Non-isolated Buck DC-DC Converter



Features

- Industrial sixteenth brick form factor
- Wide input ranges: 9 – 53V
- Wide output range: 3.3 – 36V
- High output power: 12A or 324W
- High efficiency
- Low profile
- Remote sense, output trim, remote On/Off
- Frequency synchronization
- Parallel operation
- Over-temperature protection
- Output over-current / short-circuit protection
- All components meet UL 94V-0

Applications

- Industrial applications
- Telecom, networking equipment
- Point of load power supply

Options

- Baseplate
- Negative / Positive enable logic
- Load current sharing(Parallel) / remote sense
- Power good / tracking
- Pin options

Part Numbering System

NXS	□	□□□	□	012	□	□	□
Series Name	**Input Range**	**Output Preset***	**Enabling Logic**	**Output Rating**	**Pin Options**	**Electrical Option**	**Mechanical Option**
	0: 9−18V **1:** 9−36V **2:** 18−36V **3:** 18−53V **4:** 36−53V **5:** 9−53V	**033:** 3.3V **050:** 5.0V **120:** 12V **150:** 15V **200:** 20V **240:** 24V **360:** 36V	**P:** Positive **N:** Negative	**Unit:** A **012:** 12A or 324Wmax.	**K:** 0.110” **N:** 0.145” **R:** 0.180” **S:** SMT	**5:** Sense & PG **6:** Parallel & PG **7:** Sense & Trk **A:** Parallel & Trk	**5:** Open-frame **6:** Baseplate

***** *For the availability of other preset output voltages, consult with the factory. The output voltage needs to be lower than at least 90% of the input voltage to maintain proper output regulation, see Figure 5.*

Absolute Maximum Ratings

Excessive stresses over these absolute maximum ratings can cause permanent damage to the converter. Operation should be limited to the conditions outlined under the Electrical Specification Section.

Parameter	Min	Max	Unit
Input Voltage (continuous)	-0.3	55	Vdc
ON/OFF, M/S	-0.3	Vin	Vdc
Trk, Trim, I-Share	-0.3	3.6	Vdc
Sync, PG	-0.3	8.8	
Operating Ambient Temperature (See Thermal Considerations section)	-40	105	˚C
Storage Temperature	-55	125	˚C

Electrical Specifications

These specifications are valid over the converter's full range of input voltage and output voltages, resistive load, and temperature unless noted otherwise.

Input Specifications

Parameter		Min	Typical	Max	Unit
Input Voltage		9	-	53	Vdc
Input Current		-	-	25	A
Quiescent Input Current (Vin = 24, Vo = 5.0V)		-	65	80	mA
Standby Input Current (Vin = 24V)		-	1	-	mA
Input Ripple Rejection (120 Hz)		-	30	-	dB
Input Turn-on Voltage Threshold	NXS0/NXS1/NXS5	6.75	7.0	7.25	V
	NXS2/NXS3	17	17.3	17.6	
	NXS4	33.2	33.7	34.2	
Input Turn-off Voltage Threshold	NXS0/NXS1/NXS5	6.25	6.5	6.75	V
	NXS2/NXS3	16.5	16.8	17.1	
	NXS4	32.2	32.7	33.2	

Output Specifications

Parameter		Min	Typical	Max	Unit
Output Voltage Set Point Tolerance (Vin = 12V; full load; Ta = 25°C)		-2.0	-	2.0	%
Output Voltage Set Point Tolerance (over all conditions)		-3	-	3	%
Output Regulation: Line Regulation (full range input voltage, 1/2 full load) Load Regulation(full range load, Vin = 24V) Temperature (Ta = -40°C to 85 °C)		 - - -	 0.3 1.0 0.2	 - - -	%Vo
Output Ripple and Noise Voltage (Peak-to-peak, 5 Hz to 20 MHz bandwidth, Vin = 24V)		-	1.0	-	%Vo
External Load Capacitance (non-ceramic type)		220	-	2,000	µF
Output Current		0	-	12	A
Output Current-limit Trip Point (hiccup mode, Vin=48V)	Vo = 24V	-	20	-	A
	Vo = 36V	-	17	-	

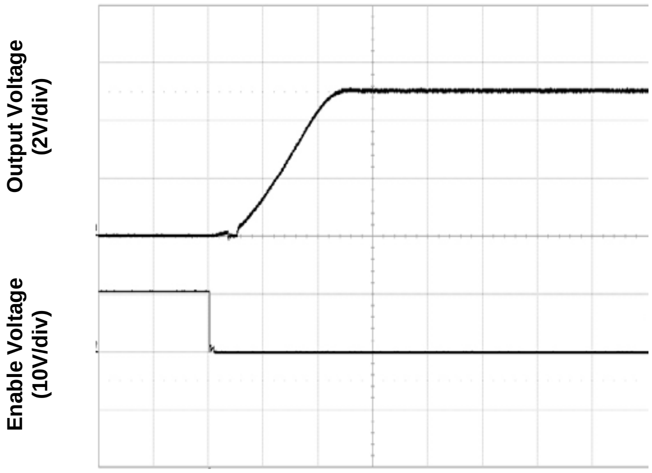
Output Specifications (Continued)

Parameter		Min	Typical	Max	Unit
Efficiency (Vin = 12V; Ta = 25ºC)	Vo = 3.3V, Io = 12A	-	93.0	-	%
	Vo = 5.V, Io = 12A	-	96.0	-	%
	Vo = 9V, Io = 12A	-	97.5	-	%
Efficiency (Vin = 24V; Ta = 25ºC)	Vo = 12V, Io = 12A	-	97.0	-	%
	Vo = 15V, Io = 12A	-	97.3	-	%
	Vo = 20V, Io = 12A	-	98.0	-	%
Efficiency (Vin = 48V; Ta = 25ºC)	Vo = 24V, Io = 12A	-	95.0	-	%
	Vo = 36V, Io = 9A	-	97.5	-	%
Output Ripple Frequency		150	200	300	kHz
Dynamic Response (Vin = 48V; Vo = 24V; Ta = 25°C) Load transient 3A→9A at 0.1A/μs, Co,ext=470μF Peak deviation Settling time (to 10% band of Vo deviation) Load transient 9→3A at 0.1A/μs, Co,ext=470μF Peak deviation Settling time (to 10% band of Vo deviation)		 - - - -	 500 1 500 1	 - - - -	 mV ms mV ms

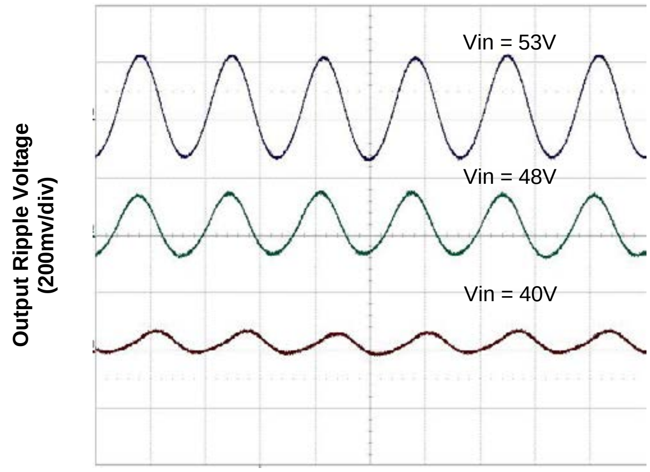
General Specifications

Parameter		Min	Typical	Max	Unit
Remote Enable Logic Low:					
	ION/OFF = 1.0mA	0	-	1.2	V
	VON/OFF = 0.0V	-	-	1.0	mA
Logic High:	ION/OFF = 0.0μA	3.5	-	15	V
	Leakage Current	-	-	50	μA

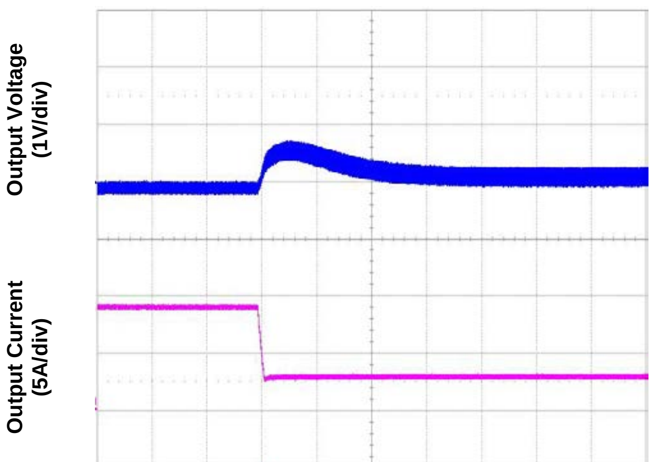
Characteristic Curves



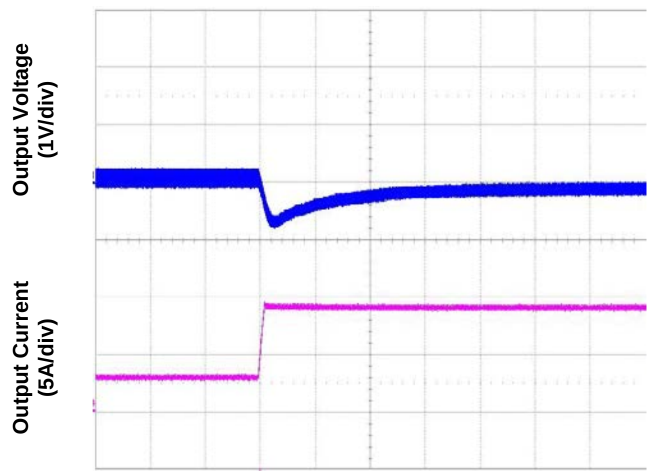
Time – t (5ms/div)
Figure 1. Startup Waveform from ON/OFF Control
(Vin=12V; Vo=5V; Io=0A; Co,ex=470μF)



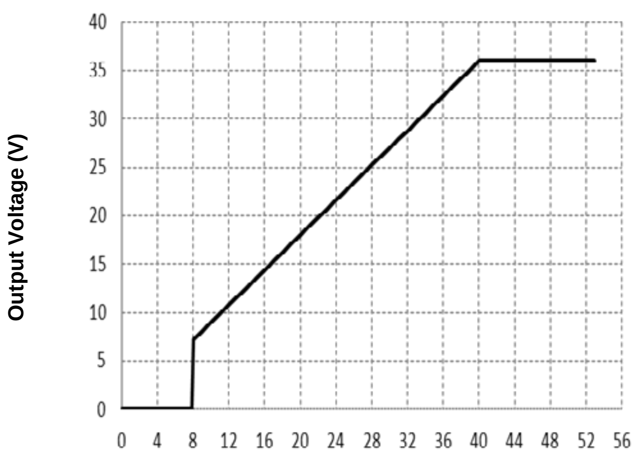
Time – t (2μs/div)
Figure 2. Output Ripple Voltage
(Vo=36V; Io=9A; Co,ex=470μF)



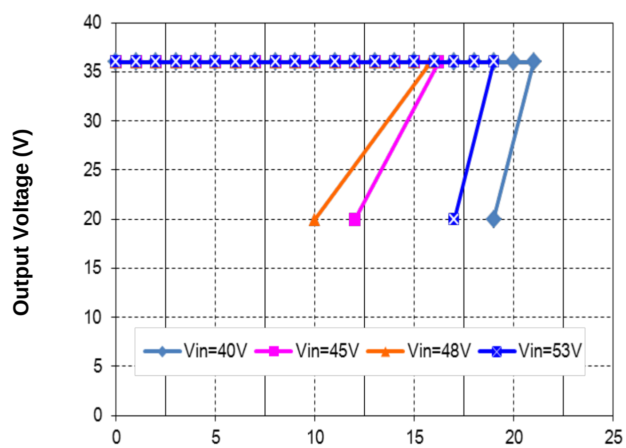
Time – t (500μs/div)
Figure 3. Transient Load Response at Vo=24V
(Vin=48V; Io=9A→3A@0.1A/us; Co,ex=470μF)



Time – t (500μs/div)
Figure 4. Transient Load Response at Vo=24V
(Vin=48V; Io=3A→9A@0.1A/us; Co,ex=470μF)



Input Voltage (V)
Figure 5. Output vs. Input Operating Range



Output Current (A)
Figure 6. Load Regulation
(Vo=36V, no I-share version)

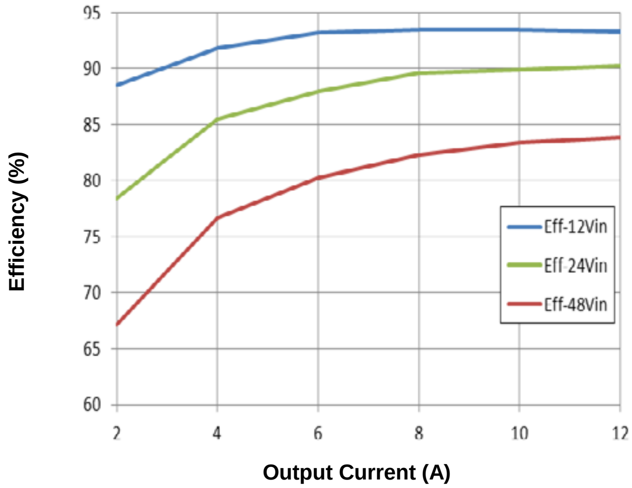


Figure 7. Efficiency Vs. Load Current (Vo=3.3V)

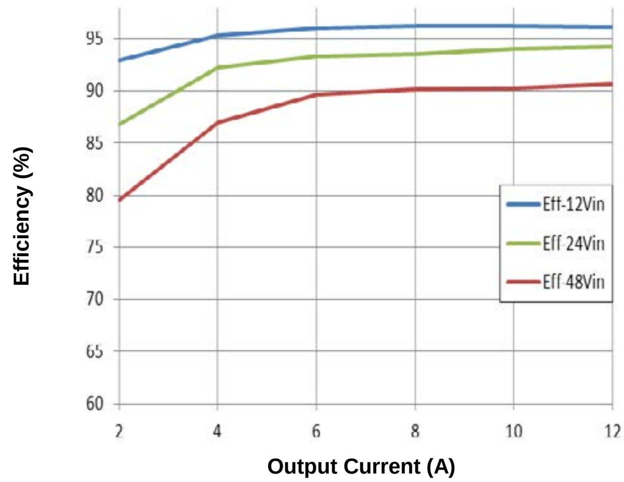


Figure 8. Efficiency Vs. Load Current (Vo=5V)

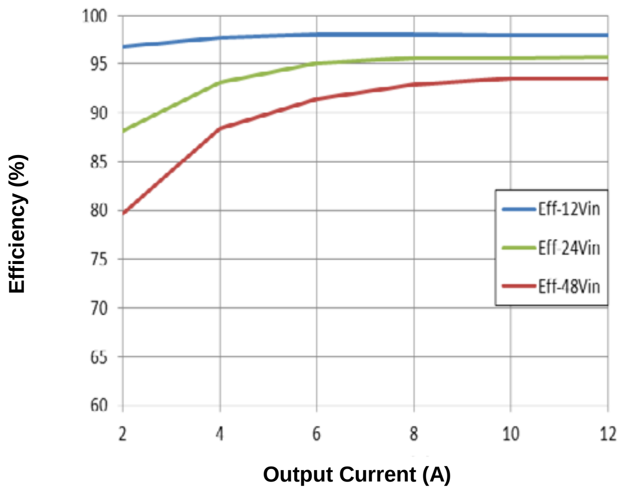


Figure 9. Efficiency Vs. Load Current (Vo=9V)

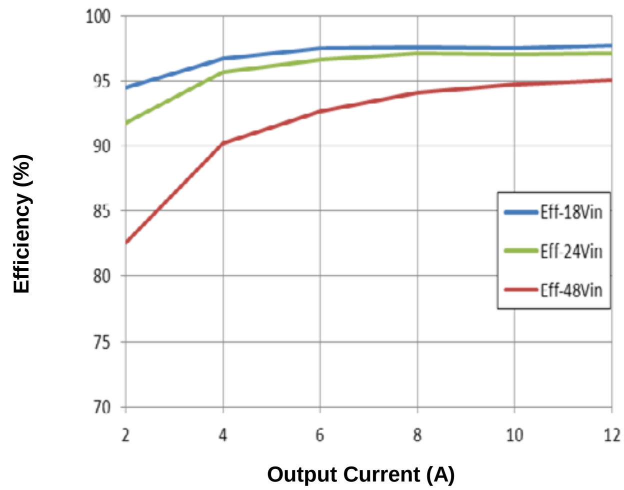


Figure 10. Efficiency Vs. Load Current (Vo=12V)

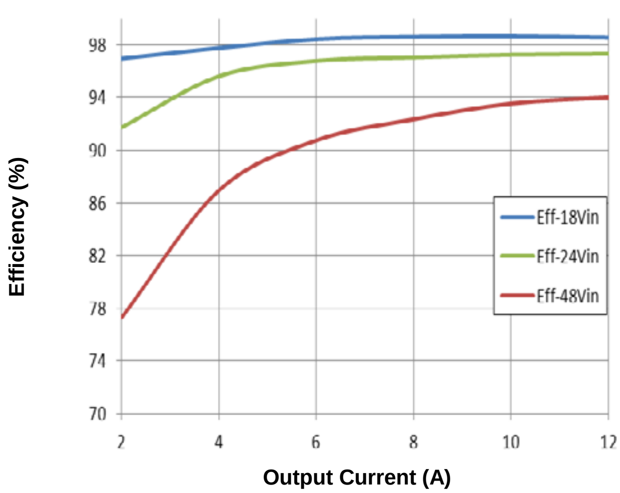


Figure 11. Efficiency Vs. Load Current (Vo=15V)

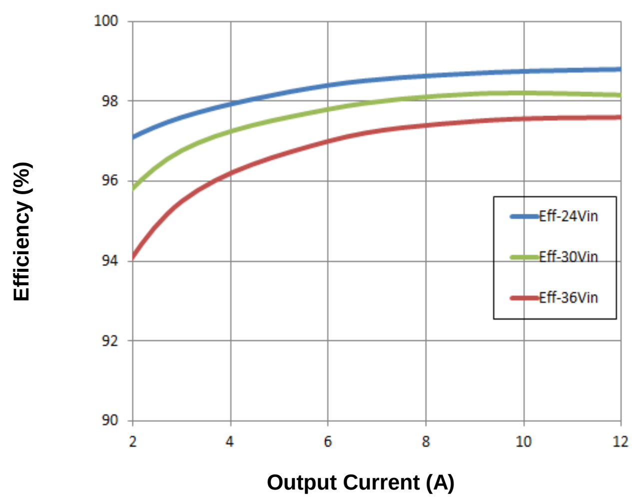


Figure 12. Efficiency Vs. Load Current (Vo=20V)

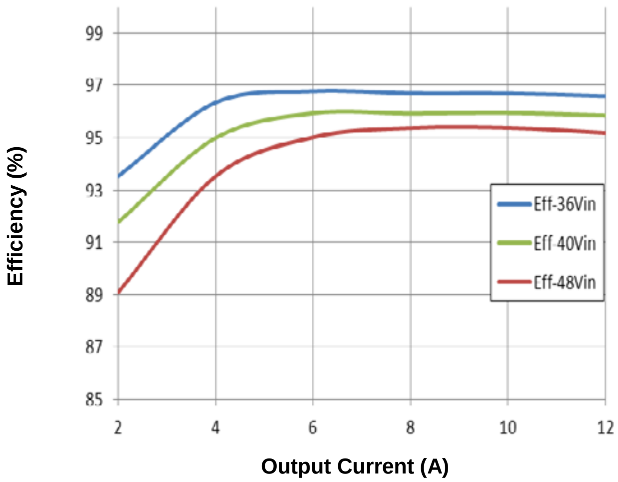


Figure 13. Efficiency Vs. Load Current (Vo=24V)

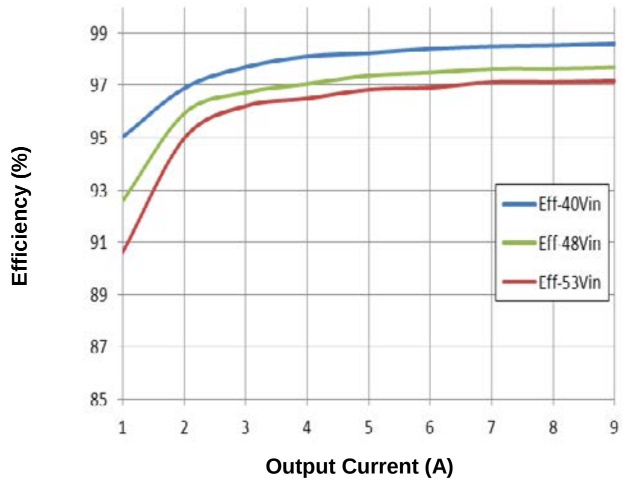


Figure 14. Efficiency Vs. Load Current (Vo=36V)

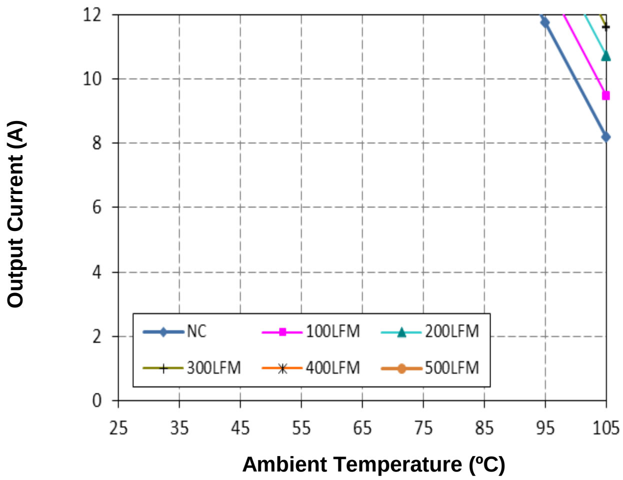


Figure 15a. Derating with Open-frame
(Vin=12V and Vo=3.3V)

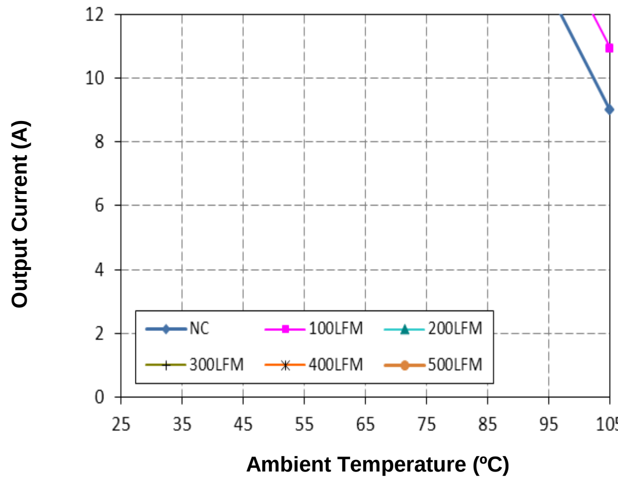


Figure 15b. Derating with Baseplate
(Vin=12V and Vo=3.3V)

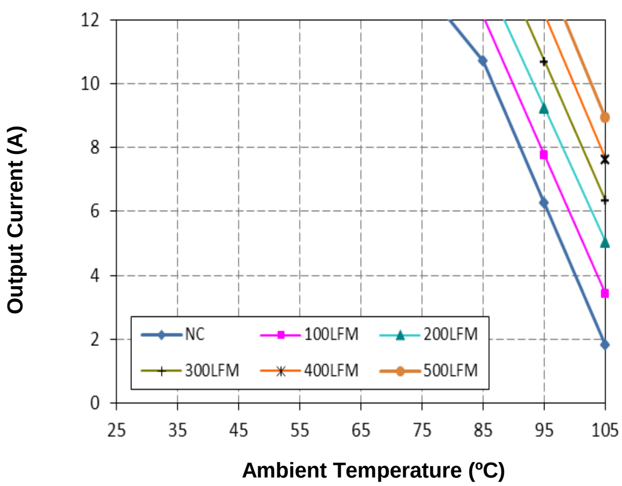


Figure 16a. Derating with Open-frame
(Vin=24V and Vo=3.3V)

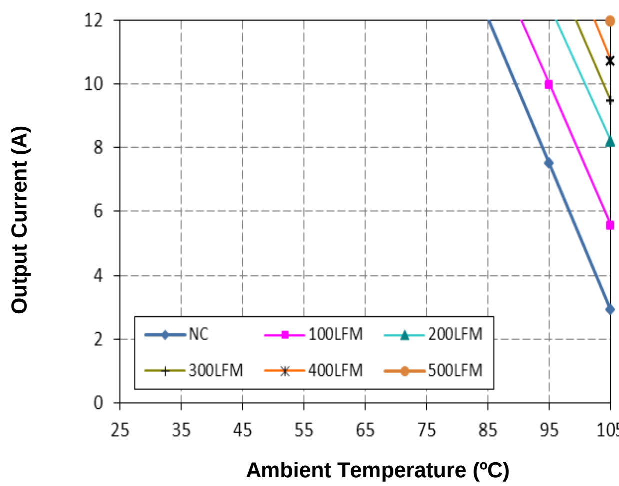


Figure 16b. Derating with Baseplate
(Vin=24V and Vo=3.3V)

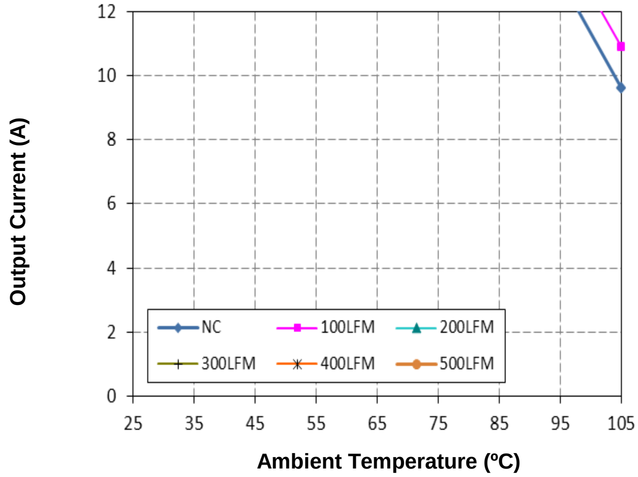


Figure 17a. Derating with Open-frame (Vin=12V and Vo=5V)

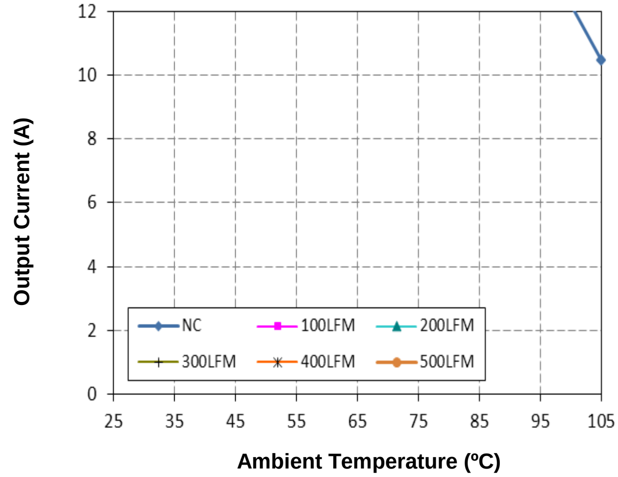


Figure 17b. Derating with Baseplate (Vin=12V and Vo=5V)

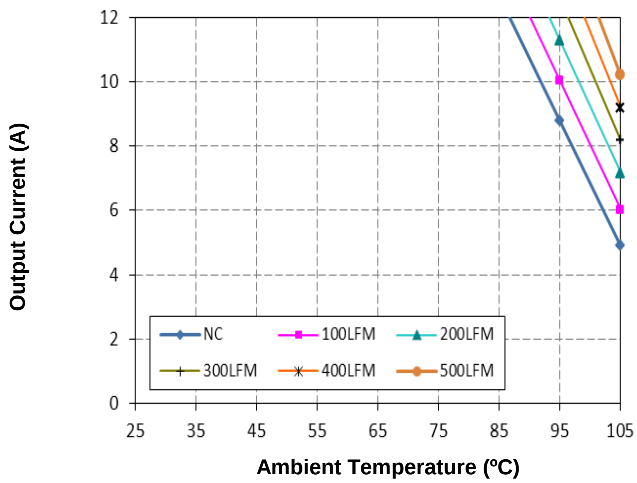


Figure 18a. Derating with Open-frame (Vin=24V and Vo=5V)

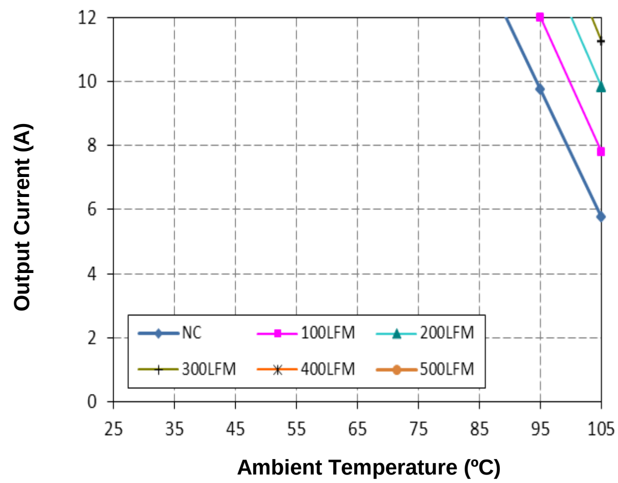


Figure 18b. Derating with Baseplate (Vin=24V and Vo=5V)

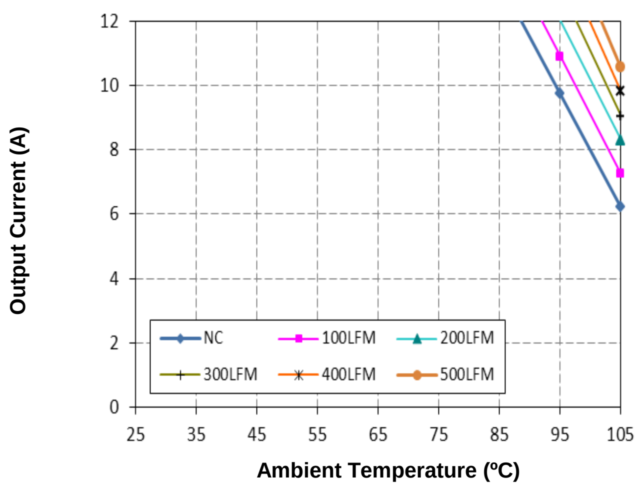


Figure 19a. Derating with Open-frame (Vin=18V and Vo=12V)

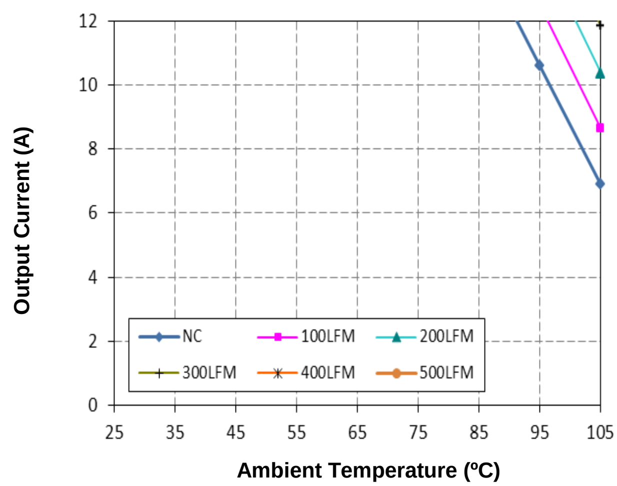


Figure 19b. Derating with Baseplate (Vin=18V and Vo=12V)

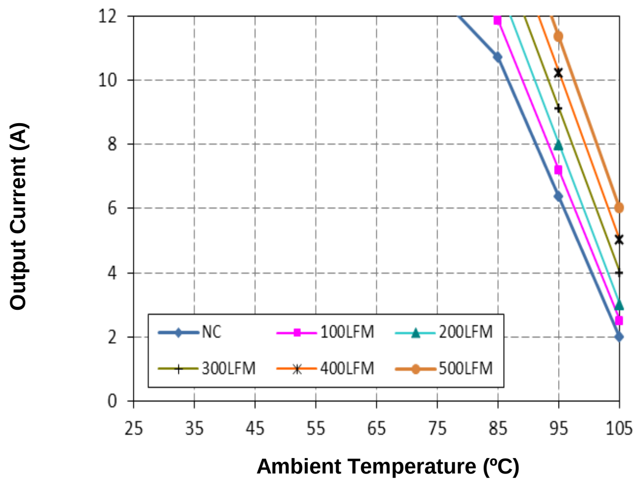


Figure 20a. Derating with Open-frame
(Vin=24V and Vo=12V)

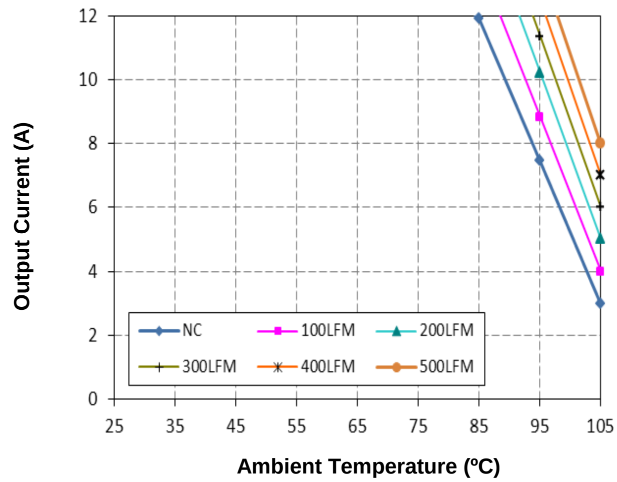


Figure 20b. Derating with Baseplate
(Vin=24V and Vo=12V)

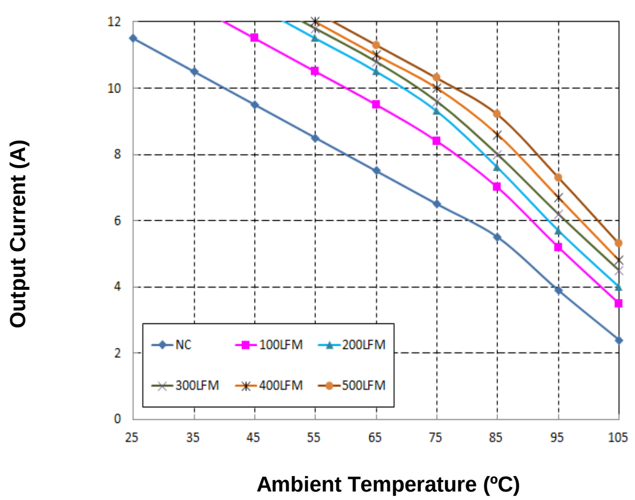


Figure 21a. Derating with Open-frame
(Vin=36V and Vo=20V)

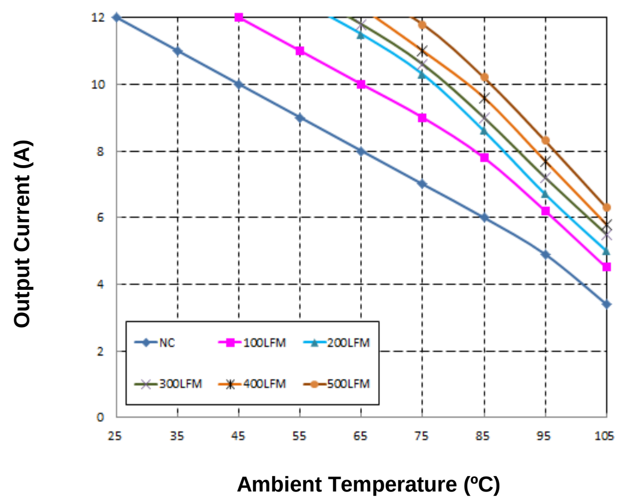


Figure 21b. Derating with Baseplate
(Vin=36V and Vo=20V)

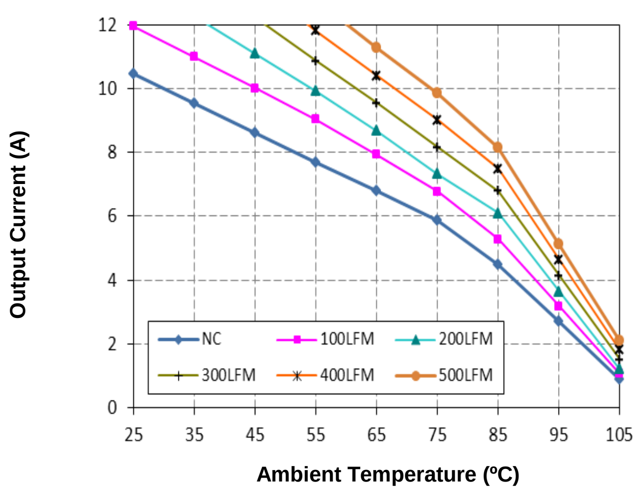


Figure 22a. Derating with Open-frame
(Vin=36V and Vo=24V)

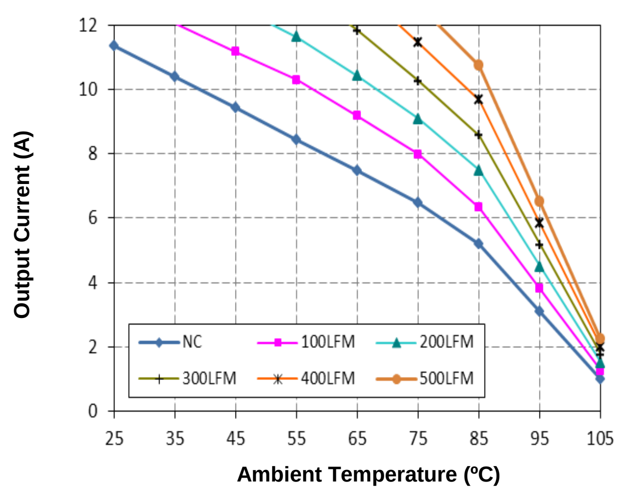


Figure 22b. Derating with Baseplate
(Vin=36V and Vo=24V)

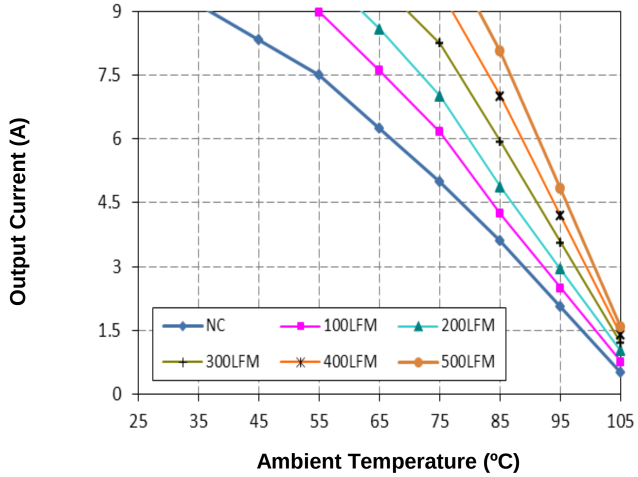


Figure 23a. Derating with Open-frame (Vin=48V and Vo=36V)

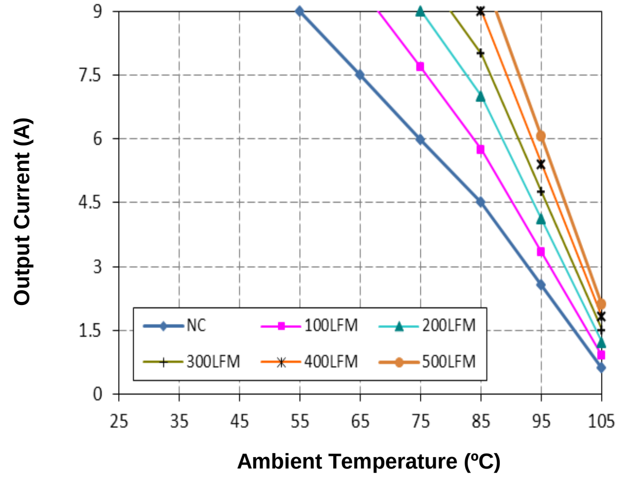


Figure 23b. Derating with Baseplate (Vin=48V and Vo=36V)

Feature Descriptions

Enable Control (ON/OFF)

The converter can be turned on and off by changing the voltage between the ON/OFF pin and Vin(-). The NXS Series of converters are available with factory selectable positive logic and negative logic.

For the negative control logic, the converter is ON when the ON/OFF pin is at a logic low level and OFF when the ON/OFF pin is at a logic high level. For the positive control logic, the converter is ON when the ON/OFF pin is at a logic high level and OFF when the ON/OFF pin is at a logic low level.

With the internal pull-up circuitry, a simple external switch between the ON/OFF pin and Vin(-) can control the converter. A few example circuits for controlling the ON/OFF pin are shown in Figures 24, 25 and 26.

The logic low level is from 0V to 1.2V and the maximum sink current during logic low is 1mA. The external switch must be capable of maintaining a logic-low level while sinking up to this current. The logic high level is from 3.5V to 15V. The converter has an internal pull-up circuit that ensures the ON/OFF pin at a high logic level when the leakage current at ON/OFF pin is no greater than 50μA.

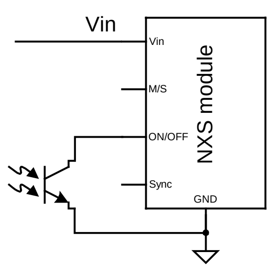


Figure 24. Opto-coupler Enable Circuit

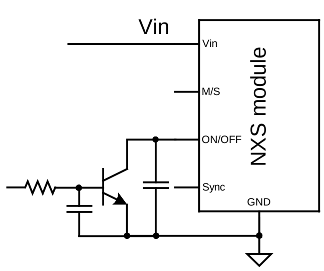


Figure 25. Open Collector Enable Circuit

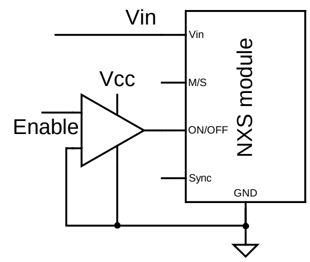


Figure 26. Direct Logic Drive

Output Voltage Adjustment

The output voltage of the NXS converter is preset to a nominal voltage. With trim feature, the output voltage can be adjusted up based on the preset output voltage using an external resistor R_{trim_up} between the TRIM pin (pin 6) and the Vo(-) pin (pin 4).

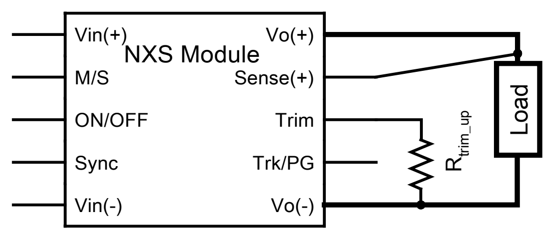


Figure 27. Circuit Configuration for Output Voltage Trim Up

The circuit configuration for trim up is shown in Figure 27. R_{trim_up} should be placed as close as possible to Vo(-) pin.

The trim up resistance R_{trim_up} is determined by below equation:

$$R_{trim\_up} = \frac{21900}{\Delta V_o} - 511 \ (\Omega)$$

Where,

$\Delta V_o = |V_o - V_{onom}|$ — Difference between the preset nominal output voltage and the trimmed output voltage, unit volt.

Power Good and Tracking (optional)

Pin 5 can be either selected to be Power Good (PG) signal output pin or Tracking (Trk) input pin.

If selected to be a PG pin, Pin 5 will be an open-drain signal to indicate whether the output is within regulation limits. When the output is out of regulation limits, Pin 5 will pull to low (<0.1V). These conditions include:

- Regulation is out of limits;
- Module is in soft-start process;
- Module is in under-voltage status;
- Fault conditions (OCP, SCP and OTP) are detected.

When the output is within the regulation limits, Pin 5 will be released as open-drain status.

If selected to be a Trk pin, Pin 5 will be an input pin for tracking voltage signal. The tracking feature makes the startup ramp up waveform to track the voltage waveform at Pin 5 proportionally. The tracking function can be configured for either ratio-metric tracking or simultaneous tracking. The tracking voltage signal at the Trk pin should start from 0V and final voltage value should be greater than 0.6V and lower than 3.6V.

If ratio-metric tracking configuration is implemented, the two (or multiple) NXS converter outputs ramp up and reach the regulation points at the same time. Figure 28 shows the circuit configuration of ratio-metric tracking and Figure 29 shows the ratio-metric tracking waveforms.

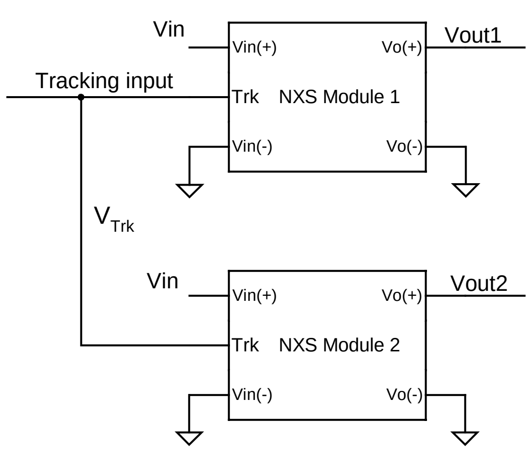


Figure 28. Circuit Configuration for Ratio-metric Tracking

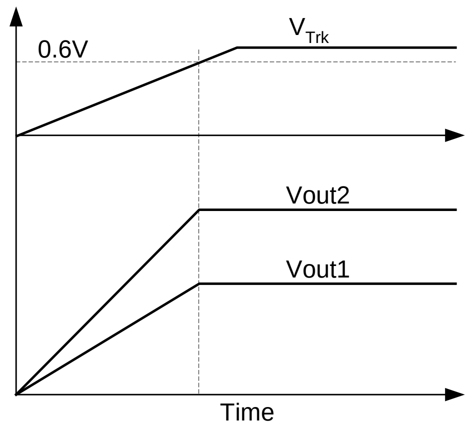


Figure 29. Ratio-metric Tracking Waveforms

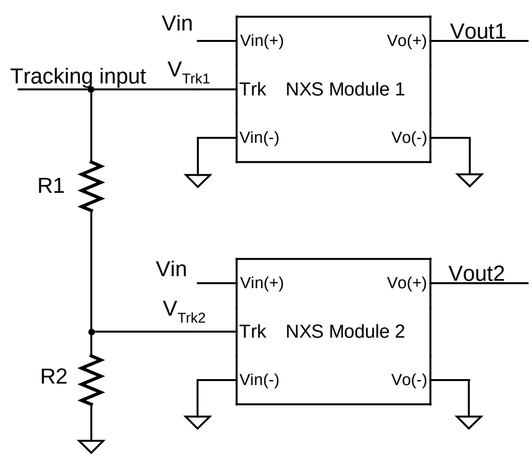


Figure 30. Circuit Configuration for Simultaneous Tracking

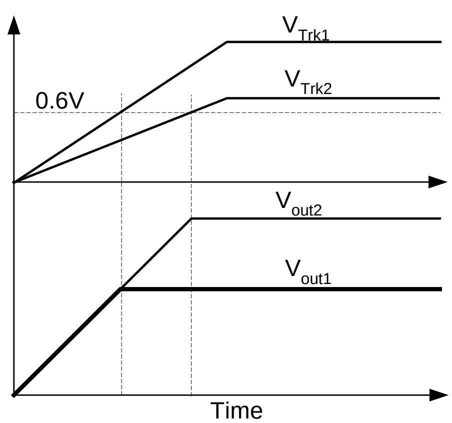


Figure 31. Simultaneous Tracking Waveforms

The Simultaneous tracking allows the two NXS converter outputs ramp up with the same slew rate until each output reaches its own regulation point. The tracking voltage signal is directly input to the NXS converter with lower output. Two resistors, R1 and R2, form a voltage divider to generate the tracking signal for the NXS converter with higher output voltage. The resistor values satisfy below equation:

$$\frac{R_1}{R_2} = \left(\frac{V_{out2}}{V_{out1}}\right) - 1$$

Circuit configuration of the simultaneous tracking is shown in Figure 30. Simultaneous tracking waveforms are shown in Figure 31.

The PG/Trk option can be configured to implement sequential startup. Figure 32 shows the circuit configuration. The PG/Trk pin of NXS module 1 is selected as PG output and that of NXS module 2 is selected as Trk input.

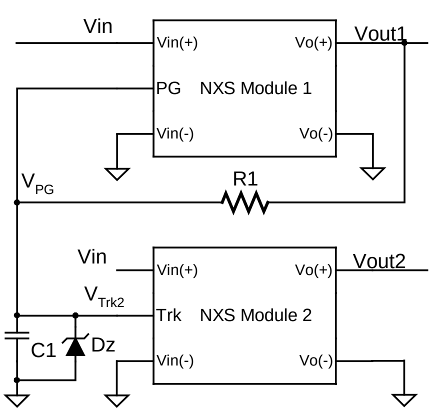


Figure 32. Circuit Configuration for Sequential Startup

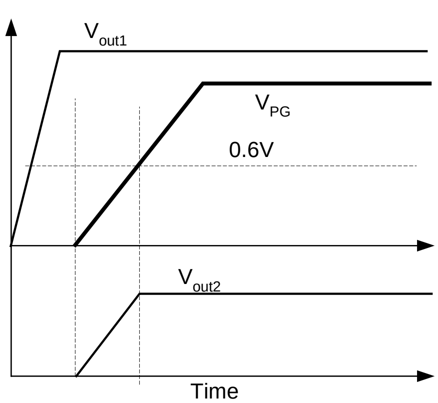


Figure 33. Sequential Startup Waveforms

Voltage V_{PG} will be held low during the startup process of module 1. When the startup process is completed, capacitor C1 will be released to be charged by Vout1 after module 1 declares power good status. With the ramping up of V_{PG}, Module 2 will start and track the charging voltage signal V_{PG} until its output Vout2 reaches the regulation point. Figure 33 shows the sequential startup waveforms.

Frequency Synchronization

Pin A (Sync) and Pin B (M/S) of NXS module are used for frequency synchronization. The NXS module can be set as either master mode or slave mode.

To set the module as master mode, Pin B (M/S) is connected to input Vin. In master mode the Sync pin emits a stream of pulses with 50% duty cycle at the same frequency as its PWM switching frequency. The amplitude of the pulse stream is 8V (typical).

In slave mode, the Sync pin is an input pin to accept a synchronization clock signal. The slave NXS module can synchronize the clock in phase or with 180° phase shift. To set the NXS module to synchronize the clock in phase, the M/S pin is connected to GND. To set the NXS module to synchronize the clock with 180° phase shift, the M/S pin is left open.

When an external synchronization clock signal is used, the NXS converter should be set as slave mode. The external synchronization clock should have frequency within 210kHz-390kHz, 50% duty ratio with amplitude greater than 2V and less than 8V. The maximum slew rate of the clock signal should be limited to 10V/μs. It is recommended that connect the Sync pin to the external clock signal via 5kΩ resistor.

Remote Sense (optional)

The remote sense feature is optional versus the load share feature. The remote sense feature makes the tight regulation at a load point possible. When the remote sense feature is selected, the Sense(+) pin (pin 7) should be connected to the positive point where the regulation is desired. The output return trace should be designed as strong as possible to reduce voltage drop at heavy load. Note that use of remote sense generally will lead to a higher output voltage at the power module output terminals.

The traces connecting Sense(+) pin should not carry significant current for good load point voltage regulation accuracy.

When remote sense is not used, the Sense(+) pin should be connected to the Vo(+) terminals. If the Sense(+) pin is left floating, the converter may deliver an output voltage slightly higher than the specified output voltage.

Load share (Parallel operation) (optional)

If Load share feature is selected, Pin 7 is used to synchronize the startup and shutdown of the load sharing NXS modules. Droop load current sharing technique is used in the NXS module to allow multiple NXS modules operating in parallel to share the load current while keeping the regulation accuracy within 10%. The circuit configuration for NXS modules to operate in load sharing is shown in Figure 34. If Tracking feature is selected, all the Trk pins should be connected together to apply the same tracking signal. The ON/OFF pins should be connected together as well to use the same enable signal.

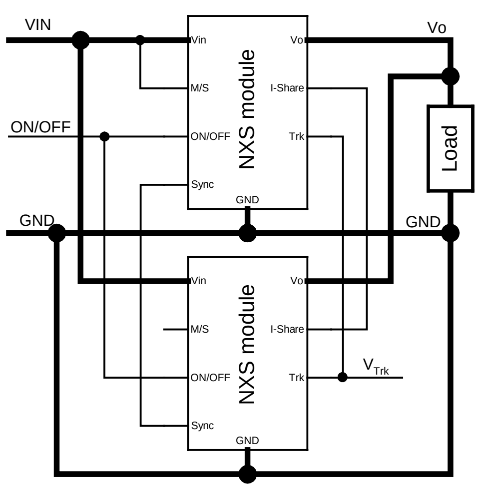


Figure 34. Circuit Configuration for Active Load Sharing

Note that if the I-Share option is selected, the trim pins should be left open.

It is recommended that the input and output power traces for the NXS converters are arranged in symmetrical way and all the converters see even airflow.

Input Under-Voltage Lockout

This feature prevents the converter from turning on until the input voltage reaches 8.0V (typical), and turns the converter off when the input voltage drops down to 7.0V (typical).

Output Over-Current and Short Circuit Protection

As a standard feature, the converter shuts off when the load current exceeds the current limit. If the over-current or short circuit condition persists, the converter will operate in a hiccup mode (repeatedly trying to restart) until the over-current condition is cleared.

Thermal Shutdown

The converter has a temperature limit to prevent the converter running into over temperature thermal condition. The converter shuts off when the over temperature condition is sensed. The converter will resume operation after it cools down. To ensure the long term reliability, Thermal monitoring points specified in Figure 35 should be kept lower than 125°C. If the NXS module is with base plate, the base plate temperature should be kept lower than 110°C.

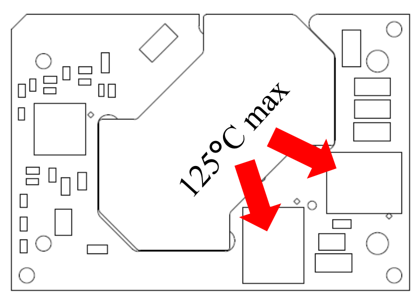


Figure 35. Thermal Monitoring Points

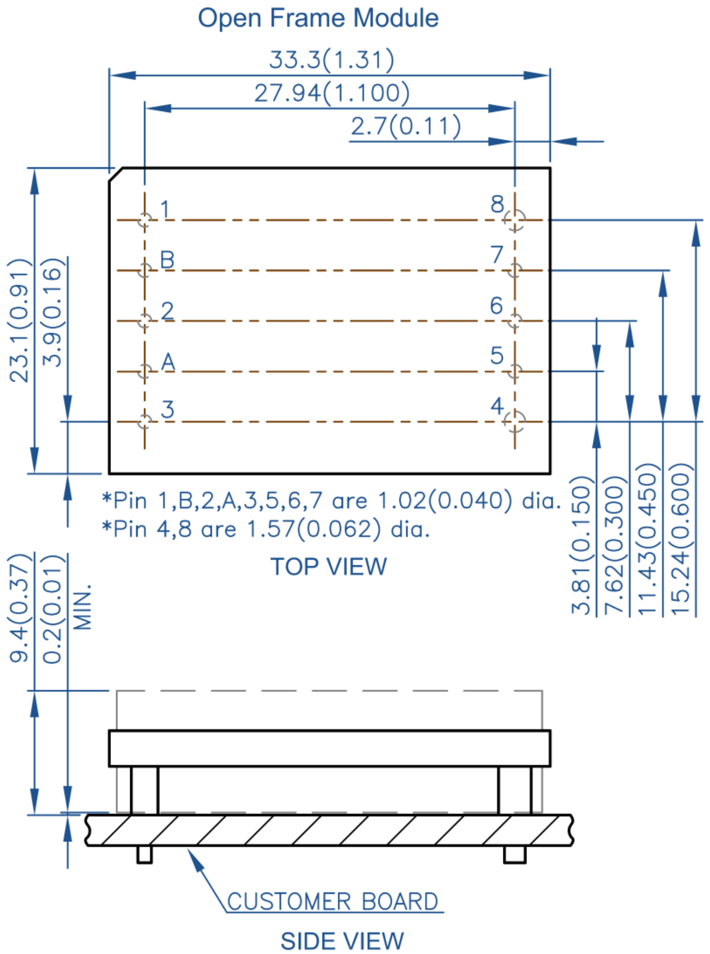
Design Considerations

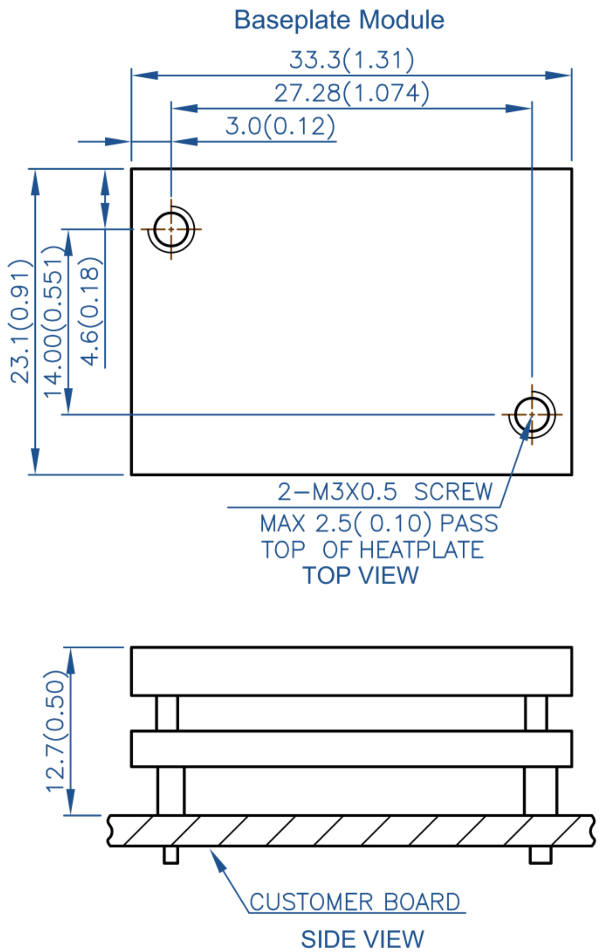
The stability of DC/DC converter will be compromised if the source impedance is high, especially in inductive impedance. It's desirable to keep the input source AC impedance as low as possible. To reduce switching frequency ripple current getting into the input circuit (especially the ground/return conductor), it is desirable to place some low ESR capacitors at the input. Due to the existence of some inductance (such as the trace inductance, connector inductance, etc.) in the input circuit, possible oscillation may occur at the input of the converter. Because the relatively high input current of low input voltage power system, it may not be practical or economical to have separate damping or soft start circuit in front of POL converters. We recommend using a combination of ceramic capacitors and Tantalum/Polymer capacitors at the input, so the relatively higher ERS of Tantalum/Polymer capacitors can help to damp the possible oscillation.

The converter is designed to be stable without additional output capacitors. To further reduce the output voltage ripple and improve the transient response, additional output capacitors are often used in applications. When additional output capacitors are used, a combination of ceramic capacitors and tantalum/polymer capacitors shall be used to provide good filtering while assuring the stability of the converter.

Mechanical Drawing

- Through hole module



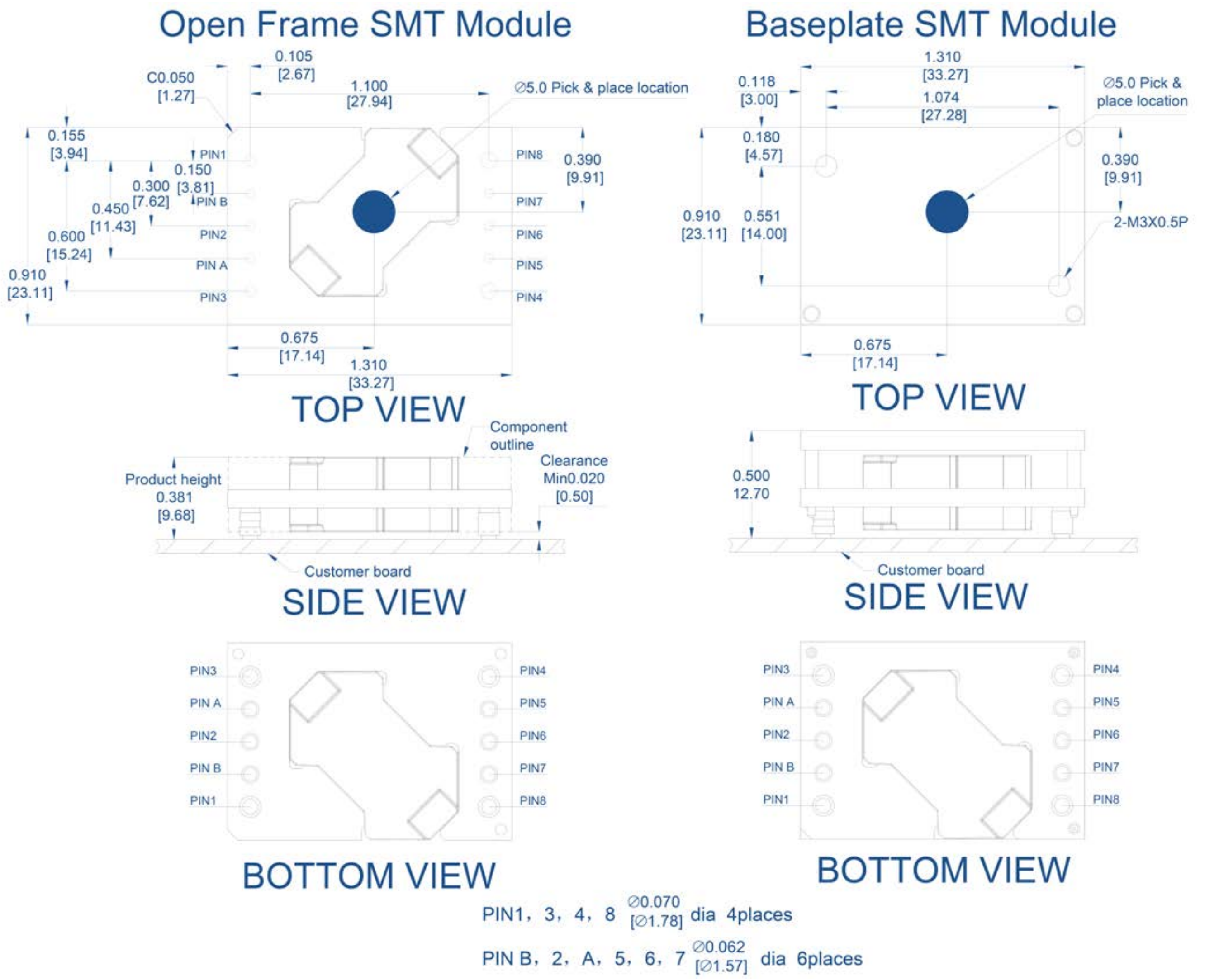


Pin	Name	Function
1	Vin(+)	Positive input voltage
B	M/S	Master/Slave
2	ON/OFF	Remote control
A	SYNC	Switching frequency synchronization
3	Vin(-)	Negative input voltage
4	Vout(-)	Negative output voltage
5	Trk/PG	Tracking or Power good (optional)
6	TRIM	Output voltage adjustment
7	SENSE(+)/I-Share	Positive remote sense or Current share (optional)
8	Vout(+)	Positive output voltage

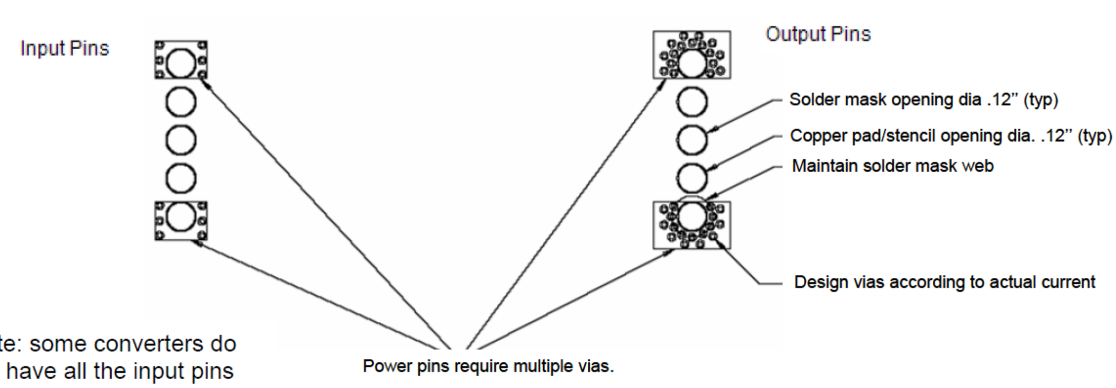
Notes

1) All dimensions in mm (inches)
   Tolerances: .x ± .5 (.xx ± 0.02)
   .xx ± .25 (.xxx ± 0.010)
2) Input and function pins are 1.02mm (0.040") dia. with +/- 0.10mm (0.004") tolerance; the recommended diameter of the receiving hole is 1.42mm (0.056'').
3) Output pins are 1.57 mm (0.062") dia. with +/- 0.10mm (0.004") tolerance; the recommended diameter of the receiving hole is 1.98mm (0.078'').
4) SMT pins are at the same locations of the through-hole pins. The recommended diameter for pad/stencil opening and solder mask opening for SMT pins is 3mm (0.12")
5) All pins are coated with 90%/10% solder, Gold, or Matte Tin finish with Nickel under plating.
6) Weight: 16 g open frame converter
   25 g baseplate converter
7) Workmanship meets or exceeds IPC-A-610 Class II
8) Baseplate flatness tolerance is 0.10mm (0.004") TIR for surface
9) Torque applied to screw should not exceed 6in-lb. (0.7 Nm).
10) If M3 screws are used to attach a heatsink to the baseplate, the screw length from the top surface of baseplate going down should not exceed 2.5mm (0.10") max.

- SMT module

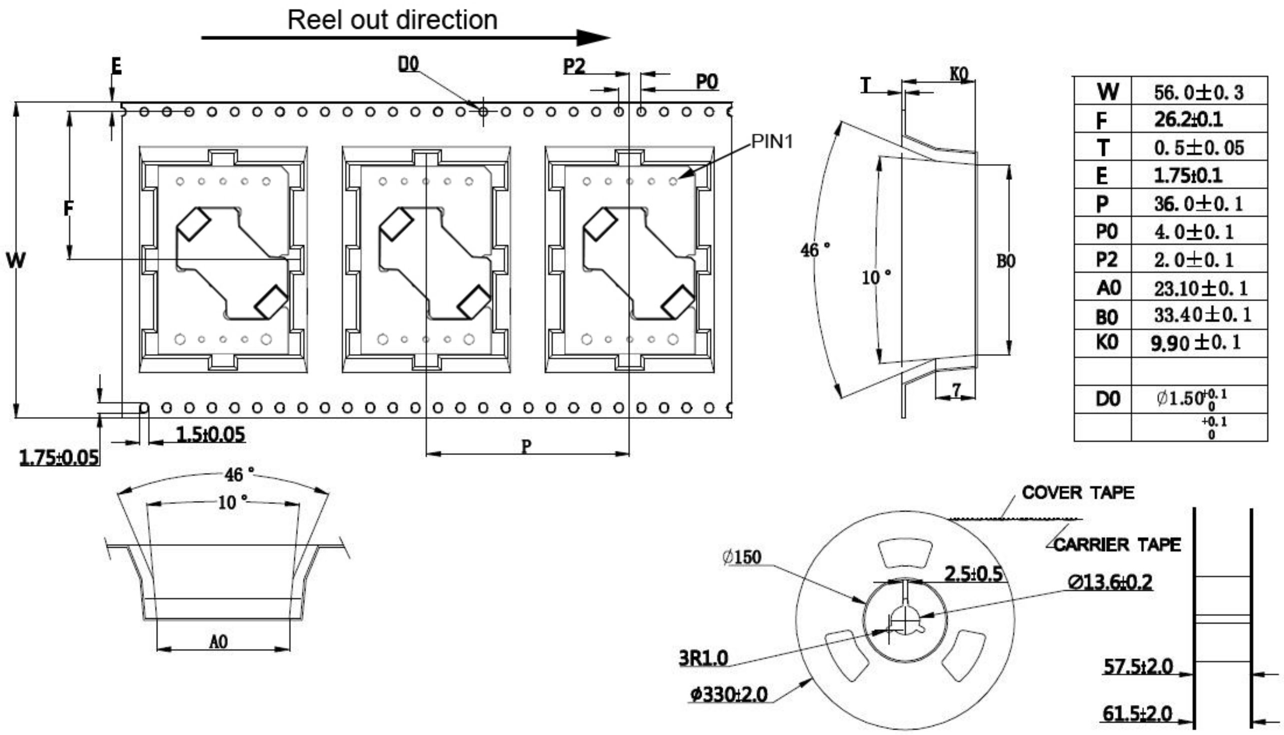


Recommended pad layout for SMT module:



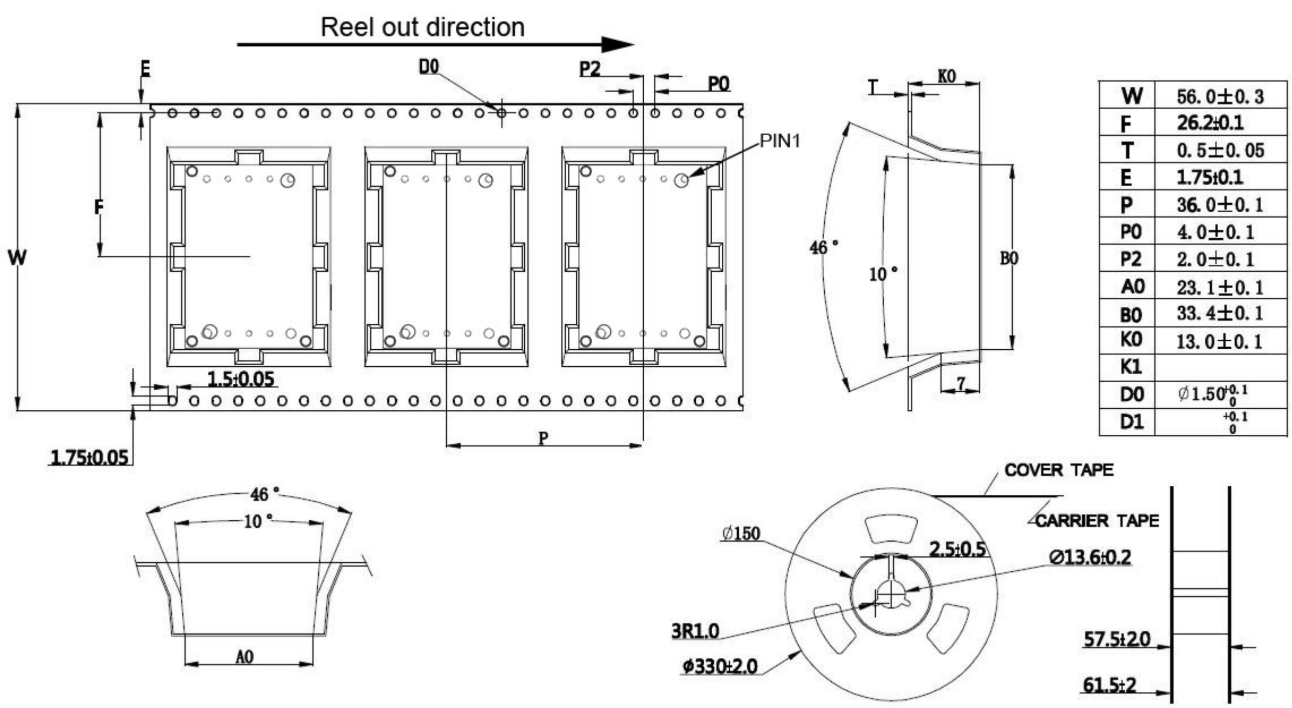
Note: some converters do not have all the input pins shown.

- Tape & Reel for SMT open frame module



W	56.0±0.3
F	26.2±0.1
T	0.5±0.05
E	1.75±0.1
P	36.0±0.1
P0	4.0±0.1
P2	2.0±0.1
A0	23.10±0.1
B0	33.40±0.1
K0	9.90±0.1
D0	$\varnothing 1.50^{+0.1}_{0}$
	$^{+0.1}_{0}$

- Tape & Reel for SMT base plate module



W	56.0±0.3
F	26.2±0.1
T	0.5±0.05
E	1.75±0.1
P	36.0±0.1
P0	4.0±0.1
P2	2.0±0.1
A0	23.1±0.1
B0	33.4±0.1
K0	13.0±0.1
K1	
D0	$\varnothing 1.50^{+0.1}_{0}$
D1	$^{+0.1}_{0}$